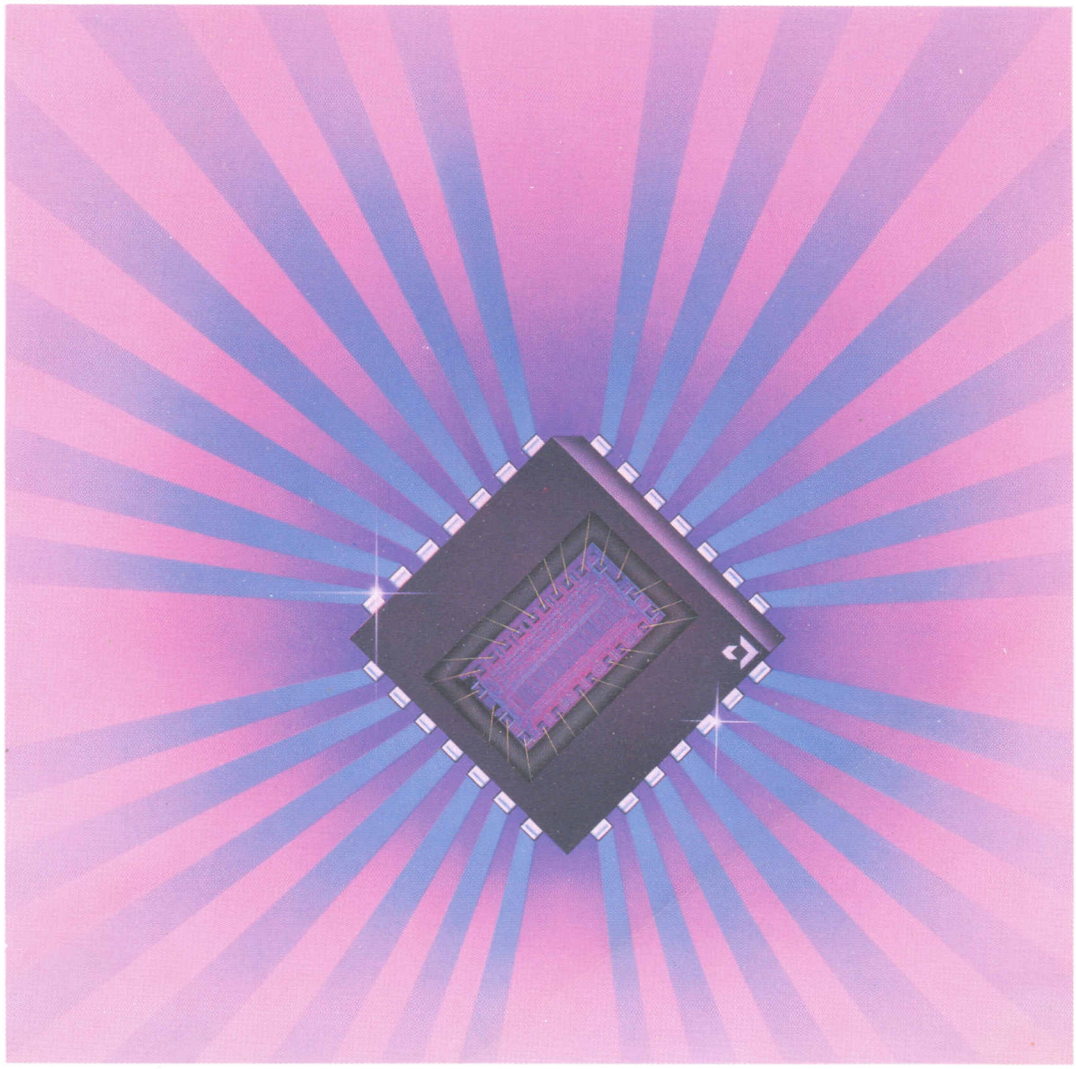
PAL® Device Data Book and Design Guide

1993

Advanced
Micro
Devices



Family	Part Number	Standard Packages	Technology	Features	t_{PD} ns	I_{CC} mA	Page
UNIVERSAL PAL DEVICES							
16V8	PALCE16V8H-5	20S, J	EE CMOS	GAL® Device Equivalent	5	125	2-58
	PALCE16V8H-7	20P, J			7.5	115	
	PALCE16V8H-10	20P, S, J			10	115	
	PALCE16V8Q-10				10	55	
	PALCE16V8H-15				15	90	
	PALCE16V8Q-15	20P, J			15	55	
	PALCE16V8H-25	20P, S, J			25	90	
	PALCE16V8Q-25	20P, J			25	55	
	PALCE16V8Z-15	20P, J		Zero-Power	15	0.015	2-104
	PALCE16V8Z-25				25	0.015	
	PALLV16V8Z-25	20P, J		3.3 V Zero-Power	25	0.015	2-124
	PALLV16V8Z-30				30	0.015	
	PALLV16V8-10	20P, J		3.3 V	10	115	2-79
	PALCE16V8HD-15	24P, 28J		High-Drive	15	115	2-135
20V8	PALCE20V8H-5	24S, 28J		GAL Device Equivalent	5	125	2-214
	PALCE20V8H-7	24P, 28J			7.5	115	
	PALCE20V8H-10				10	115	
	PALCE20V8Q-10	24P, S, 28J			10	55	
	PALCE20V8H-15	24P, 28J			15	90	
	PALCE20V8Q-15				15	55	
	PALCE20V8H-25				25	90	
	PALCE20V8Q-25				25	55	
22V10	PAL22V10-7	24P, 28J	TTL	Varied Term Distribution	7.5	220	2-266
	PAL22V10-10				10	180	
	PAL22V10-15				15	180	
	AmPAL22V10A				25	180	
	PALCE22V10H-5	28J	EE CMOS	Varied Term Distribution	5	115	2-294
	PALCE22V10H-7	24P, S, 28J			7.5	115	
	PALCE22V10H-10				10	120	
	PALCE22V10Q-10	24P, 28J			10	55	
	PALCE22V10H-15	24P, S, 28J			15	90	
	PALCE22V10Q-15	24P, 28J			15	55	
	PALCE22V10H-25	24P, S, 28J			25	90	
	PALCE22V10Q-25	24P, 28J			25	55	
	PALCE22V10Z-15	24P, S, 28J		Zero Power	15	0.015	2-320
	PALCE22V10Z-25				25	0.015	
	PALLV22V10Z-25	24P, S, 28J		3.3 V Zero-Power	25	0.015	2-331
24V10	PALCE24V10H-15	28P, J		28-Pin GAL-Type	15	115	2-345
	PALCE24V10H-25				25	115	
26V12	PALCE26V12H-15	28P, J		Advanced 22V10 Macrocell	15	105	2-360
	PALCE26V12H-20				20	105	
29M16	PALCE29M16H-25	24P, 28J		Advanced Macrocell	25	100	2-377
ASYNCHRONOUS PAL DEVICES							
610	PALCE610H-15	24P, 28J	EE CMOS	J-K F/Fs,	15	90	2-432
	PALCE610H-25			Prog. CLK	25	90	
20RA10	PALCE20RA10H-20	24P, 28J		Prog. CLK	20	100	2-236
29MA16	PALCE29MA16H-25	24P, 28J		Prog. CLK, Advanced Macrocell	25	100	2-399

Bold part numbers indicate preliminary.

Family	Part Number	Standard Packages	Technology	t_{PD} ns	I_{CC} mA	Page
STANDARD PAL DEVICES						
16R8	PAL16L8-4 PAL16R8-4 PAL16R6-4 PAL16R4-4	28J	TTL	4.5	210	2–3
	PAL16L8-5 PAL16R8-5 PAL16R6-5 PAL16R4-5	20P, J		5	210	
	PAL16L8-7 PAL16R8-7 PAL16R6-7 PAL16R4-7	20P, J, D		7.5	180	
	PAL16L8D/2 PAL16R8D/2 PAL16R6D/2 PAL16R4D/2	20P, J		10	180	
	PAL16L8B PAL16R8B PAL16R6B PAL16R4B	20N, J, NL		15	180	
	PAL16L8B-2 PAL16R8B-2 PAL16R6B-2 PAL16R4B-2			25	90	
	PAL16L8A PAL16R8A PAL16R6A PAL16R4A			25	180	
	PAL16L8B-4 PAL16R8B-4 PAL16R6B-4 PAL16R4B-4			35	55	
20R8	PAL20L8-5 PAL20R8-5 PAL20R6-5 PAL20R4-5	24P, 28J		5	210	2–121
	PAL20L8-7 PAL20R8-7 PAL20R6-7 PAL20R4-7	24P, 28J, 24D		7.5	210	
	PAL20L8-10/2 PAL20R8-10/2 PAL20R6-10/2 PAL20R4-10/2	24P, 28J		10	210	
	PAL20L8B PAL20R8B PAL20R6B PAL20R4B	24NS, 28NL, 24JS		15	210	
	PAL20L8B-2 PAL20R8B-2 PAL20R6B-2 PAL20R4B-2			25	105	
	PAL20L8A PAL20R8A PAL20R6A PAL20R4A			25	210	
18P8	AmPAL18P8B AmPAL18P8AL AmPAL18P8A AmPAL18P8L	20P, J		15 25 25 35	180 90 180 90	2-155
22P10	AmPAL22P10B AmPAL22P10AL AmPAL22P10A	24P, 28J		15 25 25	180 90 180	2-249

PAL® Device Data Book and Design Guide

1993

ADVANCED MICRO DEVICES



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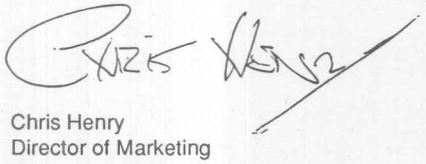
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Your fast time-to-market needs can now be met better than ever with PAL® devices from Advanced Micro Devices, Inc. This new data book provides you with a truly diverse selection of low-power and high-performance CMOS solutions in addition to the highest performing bipolar products in the industry. A number of Application Notes have also been included in order to make this data book a valuable design guide as well.

For your high-density PLD requirements, please contact an AMD representative for our latest printing of the MACH® 1 and 2 or MACH 3 and 4 Family Data Books.

Thanks for selecting AMD. Remember, our partnership helps you gain and keep the competitive edge. We're not your competition.



Chris Henry
Director of Marketing
Programmable Logic


IMPORTANT
NOTES

Chapter 1 **Introduction** **1-1**
Product Overview 1-3
Selecting the Correct CMOS PLD 1-10
Commercial PLDs for Industrial Applications 1-22

Chapter 2 **PAL Device Data Sheets** **2-1**
16R8 PAL16R8 Family 2-3
PAL16R8-4 Com'l Series 2-16
PAL16L8-4/5
PAL16R8-4/5
PAL16R6-4/5
PAL16R4-4/5
PAL16R8-7 Com'l Series 2-18
PAL16L8-7
PAL16R8-7
PAL16R6-7
PAL16R4-7
PAL16R8D/2 Com'l Series 2-20
PAL16L8D/2
PAL16R8D/2
PAL16R6D/2
PAL16R4D/2
PAL16R8B Com'l Series 2-22
PAL16L8B
PAL16R8B
PAL16R6B
PAL16R4B
PAL16R8B-2 Com'l Series 2-24
PAL16L8B-2
PAL16R8B-2
PAL16R6B-2
PAL16R4B-2
PAL16R8A Com'l Series 2-26
PAL16L8A
PAL16R8A
PAL16R6A
PAL16R4A
PAL16R8B-4 Com'l Series 2-28
PAL16L8B-4
PAL16R8B-4
PAL16R6B-4
PAL16R4B-4
PAL16R8-10/12 Mil Series 2-30
PAL16L8-10/12
PAL16R8-10/12
PAL16R6-10/12
PAL16R4-10/12

PAL16R4B
PAL16R8B-2 Mil Series 2-34
PAL16L8B-2
PAL16R8B-2
PAL16R6B-2
PAL16R4B-2
PAL16R8A Mil Series 2-36
PAL16L8A
PAL16R8A
PAL16R6A
PAL16R4A
PAL16R8B-4 Mil Series 2-38
PAL16L8B-4
PAL16R8B-4
PAL16R6B-4
PAL16R4B-4

16V8 PALCE16V8 Family 2-48
PALCE16V8H-5 Com'l 2-58
PALCE16V8H-7 Com'l 2-60
PALCE16V8H-10 Com'l 2-62
PALCE16V8Q-10 Com'l 2-64
PALCE16V8H-15/25 Q-15/25 Com'l 2-66
PALCE16V8H-15 Mil 2-68
PALCE16V8H-20/25 Mil 2-70
PALLV16V8-10 Com'l 2-79
PALCE16V8Z Family 2-95
PALCE16V8Z-15 Com'l, IND 2-104
PALCE16V8Z-25 Com'l, IND 2-106
PALLV16V8Z Family 2-115
PALLV16V8Z-25 IND 2-124
PALLV16V8Z-30 IND 2-126
PALCE16V8HD-15 Com'l 2-135

18P8 AmPAL18P8B/AL/A/L Com'l 2-155

20R8 PAL20R8 Family 2-165
PAL20R8-5 Com'l Series 2-178
PAL20L8-5
PAL20R8-5
PAL20R6-5
PAL20R4-5
PAL20R8-7 Com'l Series 2-180
PAL20L8-7
PAL20R8-7
PAL20R6-7
PAL20R4-7
PAL20R8-10/2 Com'l Series 2-182
PAL20L8-10/2
PAL20R8-10/2
PAL20R6-10/2
PAL20R4-10/2

PAL20R8B Com'l Series 2-184
PAL20L8B
PAL20R8B
PAL20R6B
PAL20R4B
PAL20R8B-2 Com'l Series 2-186
PAL20L8B-2
PAL20R8B-2
PAL20R6B-2
PAL20R4B-2
PAL20R8A Com'l Series 2-188
PAL20L8A
PAL20R8A
PAL20R6A
PAL20R4A
PAL20R8-10/12 Mil Series 2-190
PAL20L8-10/12
PAL20R8-10/12
PAL20R6-10/12
PAL20R4-10/12
PAL20R8-15 Mil Series 2-192
PAL20L8-15
PAL20R8-15
PAL20R6-15
PAL20R4-15
PAL20R8B-2 Mil Series 2-194
PAL20L8B-2
PAL20R8B-2
PAL20R6B-2
PAL20R4B-2
PAL20R8A Mil Series 2-196
PAL20L8A
PAL20R8A
PAL20R6A
PAL20R4A

20V8 PALCE20V8 Family 2-204
PALCE20V8H-5 Com'l 2-214
PALCE20V8H-7 Com'l 2-216
PALCE20V8H-10 Com'l 2-218
PALCE20V8Q-10 Com'l 2-220
PALCE20V8H-15/25 Q-15/25 Com'l 2-222
PALCE20V8H-15 Mil 2-224
PALCE20V8H-20/25 Mil 2-226

20RA10 PALCE20RA10H-20 Com'l, IND 2-236

22P10 AmPAL22P10B/AL/A Com'l 2-249

22V10 PAL22V10 Family, AmPAL22V10/A 2-258
PAL22V10-7 Com'l 2-266
PAL22V10-10 Com'l 2-268
PAL22V10-15 Com'l 2-270
AmPAL22V10A Com'l 2-272
PAL22V10-12 Mil 2-274
PAL22V10-20 Mil 2-276
AmPAL22V10/A Mil 2-278

PALCE22V10 Family ... 2-286
PALCE22V10H-5 Com'l ... 2-294
PALCE22V10H-7 Com'l ... 2-296
PALCE22V10H-10 Com'l ... 2-298
PALCE22V10Q-10 Com'l ... 2-300
PALCE22V10H-15/25 Q-15/25 Com'l ... 2-302
PALCE22V10H-15/20/25/30 Mil ... 2-304
PALCE22V10Z Family ... 2-313
PALCE22V10Z-15 IND ... 2-320
PALCE22V10Z-25 Com'l, IND ... 2-322
PALLV22V10Z-25 IND ... 2-331

24V10 PALCE24V10H-15/25 Com'l ... 2-345

26V12 PALCE26V12H-15/20 Com'l ... 2-360

29M16 PALCE29M16H-25 Com'l ... 2-377

29MA16 PALCE29MA16H-25 Com'l ... 2-399

610 PALCE610 Family ... 2-424
PALCE610H-15/25 Com'l ... 2-432
PALCE610H-20 Mil ... 2-434

Chapter 3 MACH Devices ... 3-1

MACH 1 and 2 Device Families ... 3-3
MACH110-12/15/20 ... 3-7
MACH120-15/20 ... 3-9
MACH130-15/20 ... 3-11
MACH210A-10, MACH210-12/15/20, MACH210AQ-15/20 ... 3-13
MACHLV210A-15/20 ... 3-15
MACH220-12/15/20 ... 3-17
MACH230-15/20 ... 3-19
MACH215-12/15/20 ... 3-21
MACH 3 and 4 Device Families ... 3-23
MACH435-15/20, Q-25 ... 3-27
MACH355-15/20 ... 3-29
MACH445-15/20 ... 3-31
MACH465-15/20 ... 3-33

Chapter 4 General Information ... 4-1

Inside AMD's CMOS PLD Technology ... 4-3
Military PAL Devices ... 4-43
Military ProPAL Devices ... 4-52
Electrical Characteristic Definitions ... 4-54
f_{MAX} Parameters ... 4-57
Physical Dimensions ... 4-58

Chapter 5 **Design and Testability** **5-1**
Basic Design with PLDs 5-3
PLD Design Basics 5-8
PLD Design Methodology 5-16
Combinatorial Logic Design 5-27
Registered Logic Design 5-40
State Machine Design 5-60
Testability 5-73
Ground Bounce 5-92
Metastability 5-95
Latchup 5-97
Converting Bipolar PLD Designs to CMOS 5-100
High-Speed-Board Design Techniques 5-107
Minimizing Power Consumption with Zero-Power PLDs 5-135
Designing with the PALCE16V8HD 5-138

Chapter 6 **Appendices** **6-1**
Logic Reference Guide 6-3
Signal Polarity 6-25
Glossary 6-30
Worldwide Application Support 6-37


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PAL
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CHAPTER

1 INTRODUCTION

Product Overview 1-3
Selecting the Correct CMOS PLD 1-10
Commercial PLDs for Industrial Applications 1-22


IMPORTANT
NOTES

PRODUCT OVERVIEW



Advanced
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Devices

Advanced Micro Devices offers the industry's widest variety of Programmable Logic Devices (PLDs), implemented in a variety of technologies. In this section, we will briefly discuss the device families, and look at the various architecture, speed, and power options. More specific device information can be found in the individual data sheets. Discussions on some of the special architectural features of many of the devices can also be found in their respective data sheets.

There are six basic PLD areas addressed by Advanced Micro Devices' PLDs:

- High-speed PAL® devices
- Universal PAL devices
- Industry-standard PAL devices
- Low-power PAL devices
- Asynchronous PAL Devices
- High-density PLDs

The largest application area is that covered by the Programmable Array Logic (PAL) devices. There is a wide variety of PAL devices, ranging from simple devices that address general logic design problems to more sophisticated devices that deal with more complex problems.

The area of high-density PLDs is addressed by the MACH® devices which provide a PLD with thousands of gates and very high performance. The Macro Array CMOS High-density (MACH) devices are described briefly Chapter 3. Further information on AMD's MACH product line may be found by obtaining the MACH 1 and 2 Family Data Book (14051) and the MACH 3 and 4 Family Data Book (17466). MACH design assistance is available by obtaining the MACH Technical Briefs Manual (15972) and the MACH Devices Applications Handbook (17020). Development Assistance is available through the FusionPLD^{SM} Partners Catalog (15585).

HIGH-SPEED PAL DEVICES

AMD offers the fastest PAL devices on the market today. We were the first to introduce the PAL device in 1978 and have been the first to market with volumes on all successive generations. As the market leader in the PLD arena, we fully expect to introduce even faster devices in the future.

Currently, we have the bipolar TTL PAL16R8 family of 20-pin devices in 5-ns speed grade and the PAL20R8 family of 24-pin devices, also in 5-ns speed grade, available in volume production. For extra performance we also have the 16R8 family at 4.5 ns, when packaged with the high-performance 28-pin PLCC pinout. These families include, both registered (16R4, 16R6, 16R8, 20R4, 20R6, 20R8) and combinational devices (16L8, 20L8). They are used in a wide variety of applications where performance and space are critical, often replacing SSI/MSI logic circuits. For applications where the absolute fastest devices are not needed, other speed grades are offered at a lower cost and/or lower power consumption.

AMD's Electronically Erasable (EE) CMOS process also provides high-speed universal PAL devices. The PALCE16V8, PALCE20V8, and PALCE22V10 have a 5-ns version; most other EE CMOS devices have a 7.5- or 10-ns t_{PD}, while using half or even a quarter of the power required by their bipolar equivalents.

Table 1-1 High-Speed PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PAL16L8	20	6	10	—	—	8	—	7	-4	4.5	125	210
PAL16R8	20	—	8	8	8	—	—	8	-5	5	117	210
PAL16R6	20	2	8	6	6	2	—	7–8				
PAL16R4	20	4	8	4	4	4	—	7–8				
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	H-5	5	142.8	125
PAL20L8	24	6	14	—	—	8	—	7	-5	5	117	210
PAL20R8	24	—	12	8	8	—	—	8				
PAL20R6	24	2	12	6	6	2	—	7–8				
PAL20R4	24	4	12	4	4	4	—	7–8				
PALCE20V8	24	0–8	12–14	8–0	—	—	8	7–8	H-5	5	142.8	125
PALCE24V10	28	0–10	14–16	10–0	—	—	10	7–8	H-15	15	45.5	115
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	H-5	5	142.8	115
PAL22V10	24	0–10	12	10–0	—	—	10	8–16	-7	7.5	91	220
PALCE610	24	0–16	4	16–0	—	—	16	8	H-15	15	45.5	90

f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback.

UNIVERSAL PAL DEVICES

Have your design needs included a non-standard mix of inputs and outputs or choosing a variable number of combinatorial/registered/latched inputs and/or outputs for the given application? How about stocking only one or two PLDs to reduce your inventory costs?

The solution to your problem is AMD's family of universal PAL devices. We pioneered the concept of user-programmable output logic macrocells with the PAL22V10. With this macrocell, you can configure an output for combinatorial or registered operation and active-low or active-high polarity. This is what makes the PAL22V10 universal, for it can substitute for virtually all of the standard 24-pin PAL devices on the market. The PALCE26V12 is a 28-pin version which provides more inputs and outputs for those designs that don't quite fit into a PAL22V10.

But we did not stop there. A second new feature pioneered with the PAL22V10 is variable product term distribution; the 10 outputs on this device are arranged in pairs with 16, 14, 12, 10 or eight product terms on each output. With up to 16 product terms, the PAL22V10 can implement far more complex logic functions than can be supported by other 24-pin devices. No wonder the PAL22V10 is the most popular PAL device on the market today. And now both faster (7.5 ns, 91 MHz) and reprogrammable low-power CMOS (7.5 ns at 130 mA; 15 ns at 55 mA) versions are available from AMD.

The PALCE16V8 and PALCE20V8 are EE CMOS universal devices that have the additional capability of directly taking the designs of standard 20- and 24-pin PAL devices, respectively. They provide a cost-effective means of reducing inventory, lowering power, and reducing risk. The PALCE24V10 extends this architecture to 28 pins.

The PALCE610 adds to the basic macrocell by providing 16 I/O macrocells that can be configured with D, T, J-K, or S-R flip-flops.

The PALCE29M16 further enhances the macrocell concept. Its macrocell can be an input or an output macrocell that can be configured three ways: combinatorial, latched or registered. Sixteen of these macrocells are available in a 24-pin 300-mil package. And eight of the macrocells can be buried, allowing the connecting pins to be used as dedicated inputs. The PALCE29M16 also offers variable product term distribution.

For those applications where registers and latches are not needed, the AmPAL18P8 (20 pins) and AmPAL22P10 (24 pins) are ideal. These PAL devices with programmable polarity can flexibly replace almost all standard 20- and 24-pin combinatorial PAL devices. As a result, they significantly reduce your inventory. They are available in several speed-power grades to meet most application requirements.

Table 1-2 Universal PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	H-5	5	142.8	125
									H-7	7.5	100	115
									Q-10	10	66.7	55
									H-10	10	66.7	115
									Q-15	15	45.5	55
									H-15	15	45.5	90
									Q-25	25	37	55
									H-25	25	37	90
PALCE20V8	24	0–8	12–14	8–0	—	—	8	7–8	H-5	5	142.8	125
									H-7	7.5	100	115
									Q-10	10	66.7	55
									H-10	10	66.7	115
									Q-15	15	45.5	55
									H-15	15	45.5	90
									Q-25	25	37	55
									H-25	25	37	90
PALCE24V10	28	0–10	14–16	10–0	—	—	10	7–8	H-15	15	45.5	90
									H-25	25	37	90
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	H-5	5	142.8	115
									H-7	7.5	100	115
									Q-10	10	83.3	55
									H-10	10	83.3	120
									Q-15	15	50	55
									H-15	15	50	90
									Z-15	15	50	0.015
									Q-25	25	33.3	55
									H-25	25	33.3	90
PAL22V10	24	0–10	12	10–0	—	—	10	8–16	-7	7.5	91	220
									-10	10	71	180
									-15	15	50	180
									A	25	28.5	180
PALCE20RA10	24	10	10	—	—	—	10	4	H-20	20	37	90
PALCE26V12	28	0–12	14	12–0	—	—	12	8–16	H-15	15	50	105
									H-20	20	40	105
PALCE610	24	0–16	4	16–0	—	—	16	8	H-15	15	45.5	90
									H-25	25	37	90
PALCE29M16	24	8–16	5	16–8	—	—	16	8–16	H-25	25	28.5	100
AmPAL18P8	20	8	10	—	—	8	—	8	B	15	—	180
									A	25	—	180
									AL	25	—	90
									L	35	—	90
AmPAL22P10	24	10	12	—	—	10	—	8	B	15	—	180
									A	25	—	180
									AL	25	—	90

f_{MAX} is defined as $1/(ts + tco)$ for the external feedback.

INDUSTRY-STANDARD PAL DEVICES

As we have increased speed on the TTL PAL devices, we have also reduced the power consumption on the slower devices by as much as 75 percent. As a result, both the industry-standard 20-pin and 24-pin PAL device families are available in a variety of speed and power grades. This allows the designer to select the optimum performance at the lowest possible cost and power consumption. These 20-pin and 24-pin devices are used in applications where the advantages of reduced package count, such as higher reliability and lower power consumption, improve the overall price-performance of the end-product. Often these benefits are realized by replacing Schottky, ALS, LS and some CMOS SSI/MSI logic circuits with these PAL devices.

Table 1-3 Standard PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PAL16L8	20	6	10	—	—	8	—	7	B	15	—	180
PAL16R8	20	—	8	8	8	—	—	8	B-2	25	25	90
PAL16R6	20	2	8	6	6	2	—	7–8	A	25	25	180
PAL16R4	20	4	8	4	4	4	—	7–8	B-4	35	16	55
PAL20L8	24	6	14	—	—	8	—	7	B	15	—	210
PAL20R8	24	—	12	8	8	—	—	8	B-2	25	25	105
PAL20R6	24	2	12	6	6	2	—	7–8	A	25	25	210
PAL20R4	24	4	12	4	4	4	—	7–8				

f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback.

LOW-POWER PAL DEVICES

AMD is the only major supplier of programmable logic devices to offer a broad line of low-power CMOS devices. And we are the only PLD supplier with such a comprehensive CMOS programmable logic line.

There are two basic types of CMOS PAL devices: those that dissipate essentially no power when in a quiescent state, and faster devices which draw nominal current even when quiescent. Devices are thus classified as "zero-power" or "quarter-power."

Zero-power PAL devices are particularly suited for products that are portable or battery operated. In a standby mode they consume less than 15 µA. Quarter-power CMOS devices can cut system power consumption 50 percent by replacing equivalent CMOS PAL devices. The PALLV16V8 and PALLV22V10 are devices designated to operate at 3.3 V for battery-operated applications.

Table 1-4 Low-Power PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	Q-10	10	66.7	55
									Q-15	15	45.5	55
									Z-15	15	45.5	0.015
									Q-25	25	37	55
									Z-25	25	33.3	0.015
PALLV16V8									-10	10	66.7	90
									Z-25	25	33.3	0.015
									Z-30	30	22	0.015
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	Q-15	15	50	55
									Z-15	15	50	0.015
									Q-25	25	33.3	55
									Z-25	25	33.3	0.015
PALLV22V10									Z-25	25	33.3	0.015

f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback.

ASYNCHRONOUS PAL DEVICES

Currently AMD makes three devices that support asynchronous and bus interface applications.

The PALCE20RA10 is optimized for asynchronous applications. It contains ten D-type flip-flops, driven by a PAL array. Each flip-flop has individually programmable Clock, Reset and Preset product terms. With such features, this device is well suited to replacing glue logic in your system.

The PALCE29MA16 combines some of the advantages of the PALCE29M16 with the advantages of the PALCE20RA10. It has one dedicated Clock/Latch Enable input as well as product terms for each of the 16 macrocells to allow individual clocking, asynchronous Reset and asynchronous Preset. It also features variable product term distribution. To top it off, the PALCE29MA16 is electrically reprogrammable in a plastic 300-mil package.

The PALCE610 is a general purpose PLD. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J-K or S-R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Asynchronous clocking is available since each clock pin controls 8 of the 16 macrocells.

Table 1-5 Asynchronous PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE20RA10	24	10	10	—	—	—	10	4	H-20	20	50	90
PALCE29MA16	24	8–16	5	16–8	—	—	16	4–12	H-25	25	28.5	100
PALCE610	24	0–16	4	16–0	—	—	16	8	H-15 H-25	15 25	45.5 37	90 90

**f_{MAX} is defined as 1/(ts + tco) for the external feedback.*

Selecting the Correct CMOS PLD—An Overview of Advanced Micro Devices' CMOS PLDs

Application Note
by Steve Holte, Applications Engineer

Advanced Micro Devices

INTRODUCTION

The purpose of this application note is to provide a survey of AMD's CMOS PLDs (Programmable Logic Devices). This includes both PAL (Programmable Array Logic) devices and the more general realm of PLDs to which PAL devices belong. With the proliferation of parts the selection of the best PLD for your application may seem difficult. If you are a new PLD user, this overview will guide you through the wide variety of different device architectures, speed, and power grades. This tutorial should increase your understanding of the basic characteristic features that make a device appropriate for a given application.

Figure 1 shows a "CMOS PAL Selection Route Map." This can be used as a convenient model of the discussion throughout this paper. It can also be used as a reference guide when you are selecting a PLD for a particular application.

The Benefits of AMD's CMOS PLDs

Before addressing individual products, it is important to understand why CMOS technology is used in PLDs. There are two universal benefits of AMD's CMOS PLDs: electrical erasability and low power.

Electrical Erasability

Because PLDs are programmable, electrical erasability is probably the most important advantage that CMOS technology can bring. AMD's electrically-erasable CMOS has benefits that make it superior to both UV-erasable CMOS and bipolar technologies. The most important advantage is the ability to erase the device electrically in a matter of seconds as opposed to hours for UV-based technologies, and not at all in the case of bipolar. The chief benefit to the user is a very high quality device. This is realized through the ability to erase and reprogram the device many times at various test points in the factory. In fact, the quality is so good that programming and post-programming functional rejects are virtually non-existent.

A second major benefit of electrical erasability is the ease of reprogramming the device by the user. This saves time when prototyping, and allows for recovery of large volumes of devices that may need to be reprogrammed for a variety of reasons, such as mid-production bug fixes. Erasure takes place automatically by the device programmer, and is completely transparent to the user.

Low Power

The most well-known attribute of CMOS is low power consumption. All PALCE (Programmable Array Logic CMOS Electrically-Erasable) devices are offered in half-power versions; they require at most half the supply current of their first-generation bipolar counterparts. Some devices are also offered in quarter-power versions. This is achieved by taking the latest process technology and designing to favor even lower power over the fastest speed possible.

CMOS uses less current than bipolar because most of the current flow only takes place while the transistors are actually switching. With bipolar, current flows through the transistors all the time. AMD's half- and quarter-power CMOS devices take advantage of this as much as possible. However, in order to achieve high speed it is necessary to operate some transistors on the chip in the linear region. Because this circuitry is essentially always switching, the power consumption does not go to zero as it would in a conventional CMOS device.

Lower power requirements are ideal for applications which have tight power budgets, such as mobile telecommunications. Smaller power supplies also reduce cost and lowers heat dissipation. This results in smaller cooling fans, or perhaps no fan at all. It also allows the system designer to pack everything even tighter since less empty space is needed for air circulation. This can make the circuit board fit in a smaller package, again reducing cost.

Publication# 17402 Rev. A Amendment/0
Issue Date: February 1993

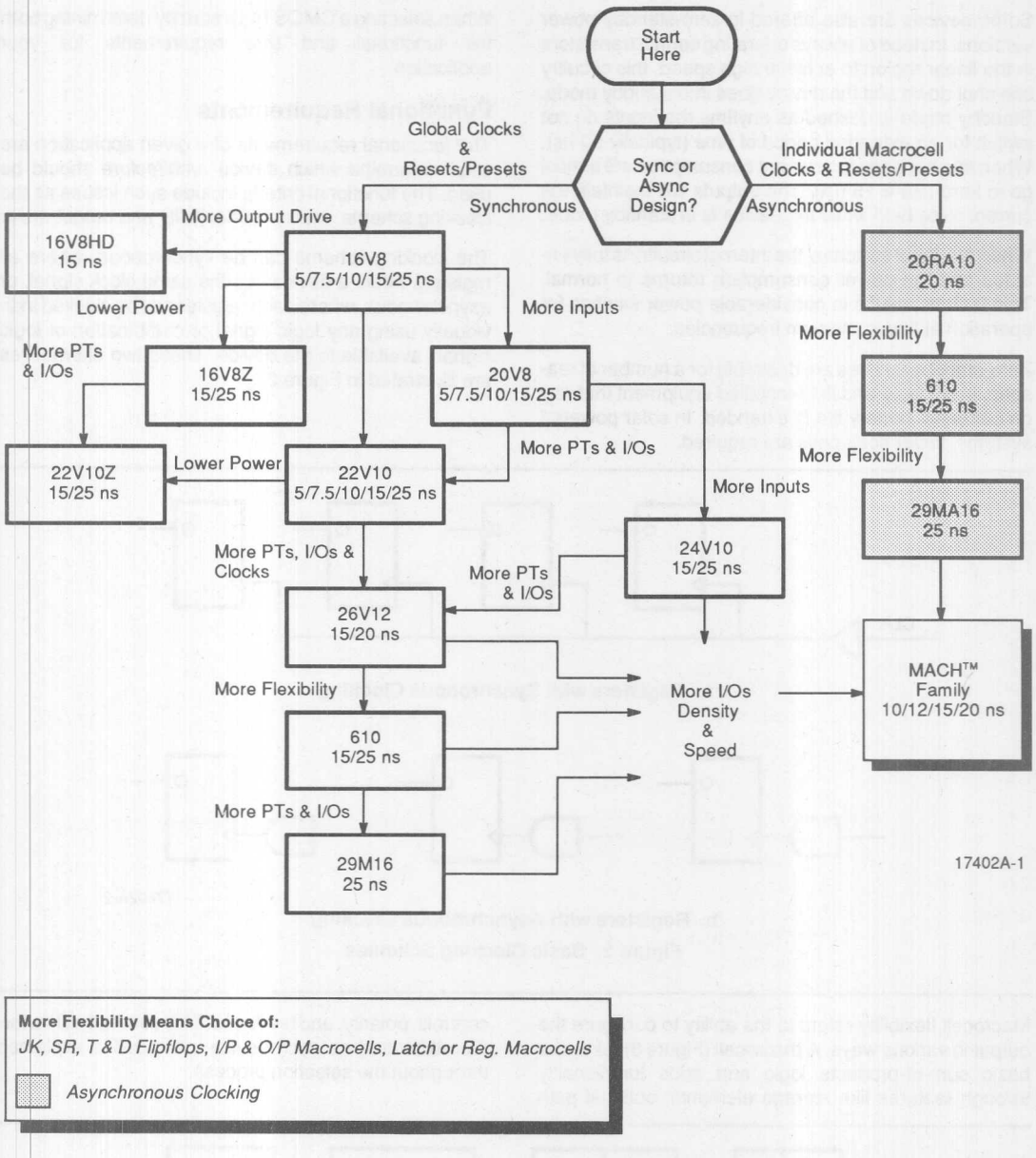


Figure 1. CMOS PAL Selection Route Map

Zero-Power

Some devices are also offered in zero-standby power versions. Instead of *always* operating certain transistors in the linear region to achieve high speed, this circuitry can shut down and the device goes into standby mode. Standby mode is defined as anytime the inputs do not switch for an extended period of time (typically 50 ns). When this happens the current consumption will almost go to zero (I_{CC} < 15 μA). The outputs will maintain the current state held while the device is in standby mode.

When any input switches, the internal circuitry is fully enabled and the power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies.

Zero-standby devices are desirable for a number of reasons. In portable and field-installed equipment that rely on batteries, battery life is extended. In solar powered systems, fewer solar cells are required.

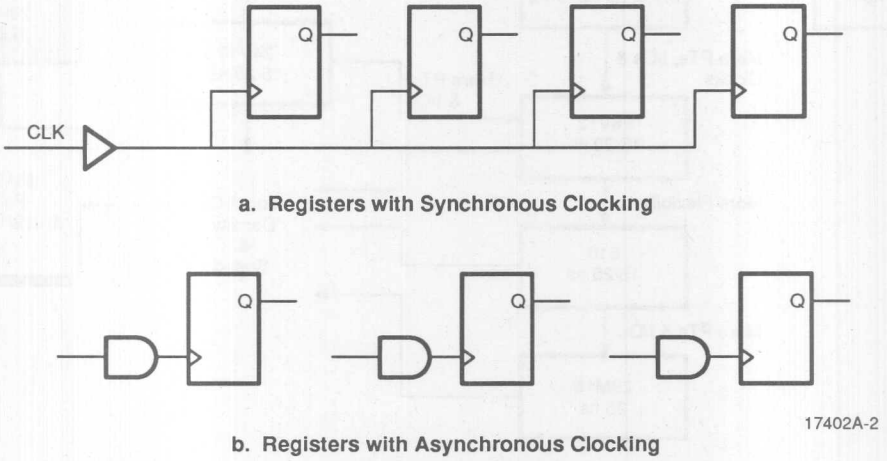
The Selection Process

When selecting a CMOS PLD, start by determining both the functional and size requirements for your application.

Functional Requirements

The functional requirements of a given application are what determine which device *architecture* should be used. The functional criteria include such issues as the clocking scheme, macrocell flexibility and output drive.

The clocking scheme can be synchronous, where all registers within a device use the same clock signal, or asynchronous, where each register can be clocked individually using any logic signal or combination of logic signals available to the device. These two alternatives are illustrated in Figure 2.



a. Registers with Synchronous Clocking

b. Registers with Asynchronous Clocking

Figure 2. Basic Clocking Schemes

Macrocell flexibility refers to the ability to configure the output in various ways. A macrocell (Figure 3) takes the basic sum-of-products logic and adds functionality through features like storage elements, optional path controls, polarity, and feedback. This concept will be further illustrated as each device macrocell is explained throughout the selection process.

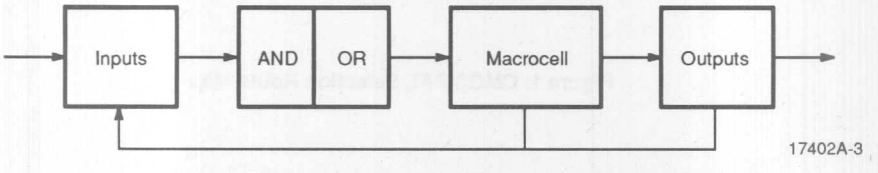


Figure 3. PLD Block Diagram with the Macrocell Included

Size Requirements

The combination of number of inputs and outputs required determines the device *size* that should be used. The number of product terms required to implement a particular design also factor into this decision.

The best approach to selecting the appropriate device is to begin with the simplest and smallest devices and upgrade as necessary to accommodate your application.

Combinatorial and Synchronous Applications

Starting from the top of the flow chart in Figure 1 and taking the path for synchronous designs leads one to those devices best suited for simple state machines, encoders, decoders, muxes, and similar logic applications. For these applications, D-type registered or combinatorial (non-registered) logic is needed. The first choice is the **PALCE16V8, PALCE20V8, or PALCE24V10,** depending on the number of inputs or outputs needed. The macrocells (Figure 4) can be configured to use combinatorial or D-type registered outputs in any combination. The D-type register operates very simply; data presented at the D input of the register will be clocked into the register on the rising edge of the clock signal. The output can be configured as active low- or active high-output depending on the requirements of the downstream devices and the efficiency of the logic.

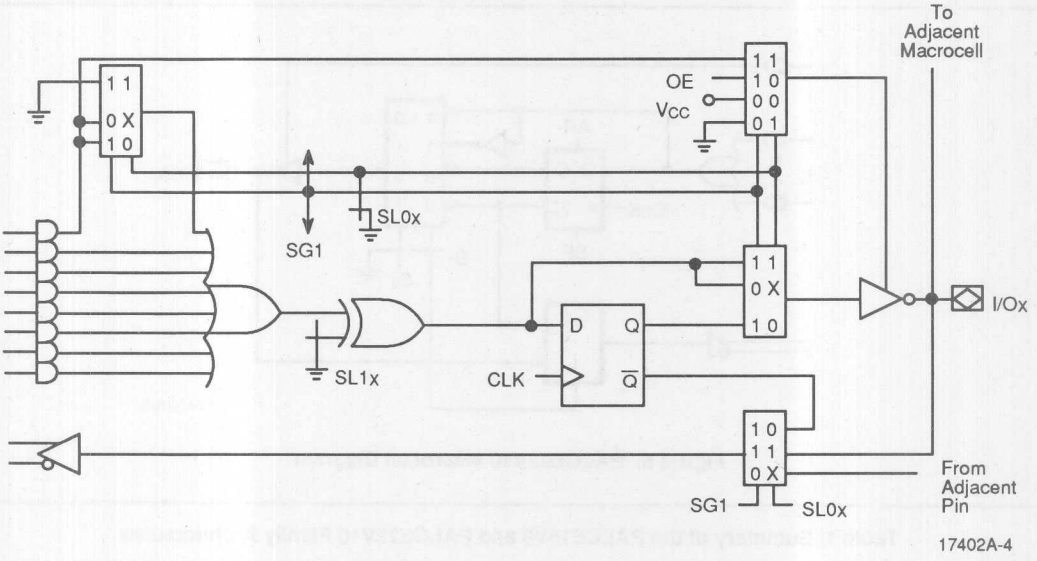


Figure 4. PALCE16V8 Macrocell

More Product Terms and I/O's

If the application requires the features of the PALCE16V8 macrocell, but requires more programmable gate functions, move further down the flowchart. The next device, the **PALCE22V10** (Figure 5) has varied product term distribution. The number of product terms varies among outputs, with up to 16 product terms on some outputs. In addition, it has global synchronous preset and asynchronous reset product terms. These are connected to all macrocells configured as registers, facilitating easy power-up and system reset. This versatility contributes significantly to the 22V10 being the world's most popular PAL architecture. When combined with the PALCE16V8 family, these two device families will likely handle about 80% of PLD applications.

The **PALCE26V12**, a 28-pin version of the 22V10 increases versatility by adding more inputs and outputs, and by adding another global clock. Any macrocell can use one of the two clocks. This allows the logic to be partitioned giving greater design flexibility. In addition, registered outputs can be configured as bidirectional pins on the 26V12.

Since historically most applications in bipolar technology had been done in PAL16R8, PAL20R8, and PAL22V10 families, these types of applications can easily have their power lowered with half-, quarter-, and zero-power versions of the PALCE16V8, PALCE20V8, or PALCE22V10.

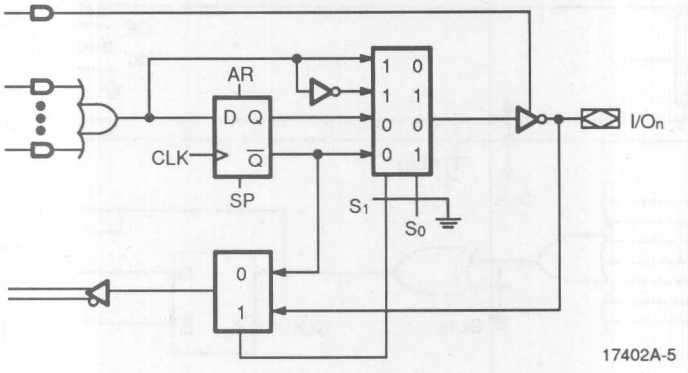


Figure 5. PALCE22V10 Macrocell Diagram

Table 1. Summary of the PALCE16V8 and PALCE22V10 Family Architectures

Device	Macrocell Type	Dedicated Inputs	I/O's	Clocks	Product Terms
PALCE16V8	16V8	8–10	8	1	7–8
PALCE20V8	16V8	10–12	8	1	7–8
PALCE24V10	16V8	14	10	1	7–8
PALCE22V10	22V10	12	10	1	8–16
PALCE26V12	22V10	14	12	2	8–16

Table 2. Summary of the Speed and Power Requirements for the PALCE16V8, PALCE20V8, and PALCE22V10 Families of Devices

Device and Speed Grade	I_{CC}
PALCE16V8H-5	125 mA static
PALCE16V8H-7/-10	115 mA at 25 MHz
PALCE16V8H-15/-25	90 mA at 15 MHz
PALCE16V8Q-15/-25	55 mA at 15 MHz
PALCE16V8Z-25	15 µA in standby mode
PALCE20V8H-5	125 mA static
PALCE20V8H-7/-10	115 mA at 25 MHz
PALCE20V8H-15/-25	90 mA at 15 MHz
PALCE20V8Q-15/-25	55 mA at 15 MHz
PALCE22V10H-5	140 mA at 25 MHz
PALCE22V10H-7	140 mA at 25 MHz
PALCE22V10H-10	120 mA at 25 MHz
PALCE22V10H-15/25	90 mA static
PALCE22V10Q-25	55 mA static
PALCE22V10Z-25	15 µA in standby mode

Bus Applications

For applications that require bus interaction, the **PALCE16V8HD** features 64 mA low-output and 16 mA high-output drive capability. This compares to 24 mA low-output and 3.2 mA high-output drive for other PALCE16V8 devices. The PALCE16V8HD also has some unique macrocell features. Because this device is designed to drive a bus, it can be configured with open-drain outputs. Open-drain (open-collector) configuration is sometimes used in bus applications because it provides controlled V_{OH}, termination, and wire-NOR capability. Because the PALCE16V8HD is designed to take inputs directly from a noisy bus, all inputs have 200 mV input threshold hysteresis to improve noise immunity. The inputs can be configured as direct or latched, making additional buffering devices unnecessary. Additionally, the macrocell can be configured as either a D- or T-type register. The T-type register is more efficient for counter applications because fewer product terms are consumed as hold states.

Complex Functions

For those applications that require D, T, J-K, or S-R register capability, the **PALCE610** (Figure 6) has this flexibility. This device has 16 macrocell outputs and four dedicated inputs. The J-K, S-R, and T registers allow easy implementation of counters and larger state machines.

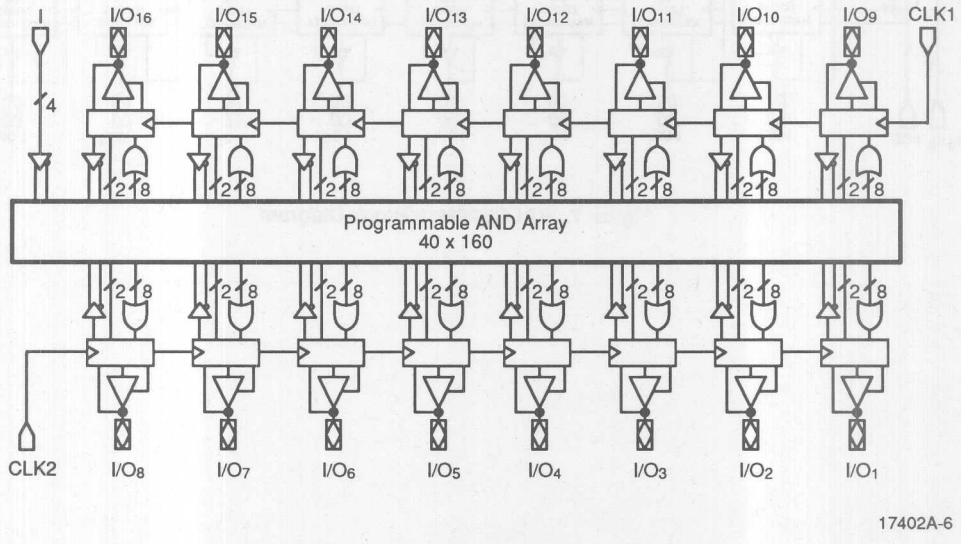


Figure 6. PALCE610 Block Diagram

More Flexibility

Moving down to the bottom of the flow chart reveals a more flexible device than the PALCE610. Applications that make use of embedded, or buried, registers can take advantage of the **PALCE29M16** (Figure 7). Buried register operation is very useful when a state machine uses state bits that do not need to be brought outside the chip. This allows the pin associated with the macrocell to be available as an input. Eight of the 16 macrocells have *dual feedback* capability. This means that these macrocells have two independent feedback paths: one from the register and one from the I/O pin. The other eight macrocells have *single* feedback, where both paths are available but, only one or the other can be used. Since almost every pin is an I/O pin this device has 29 available inputs to the programmable AND array.

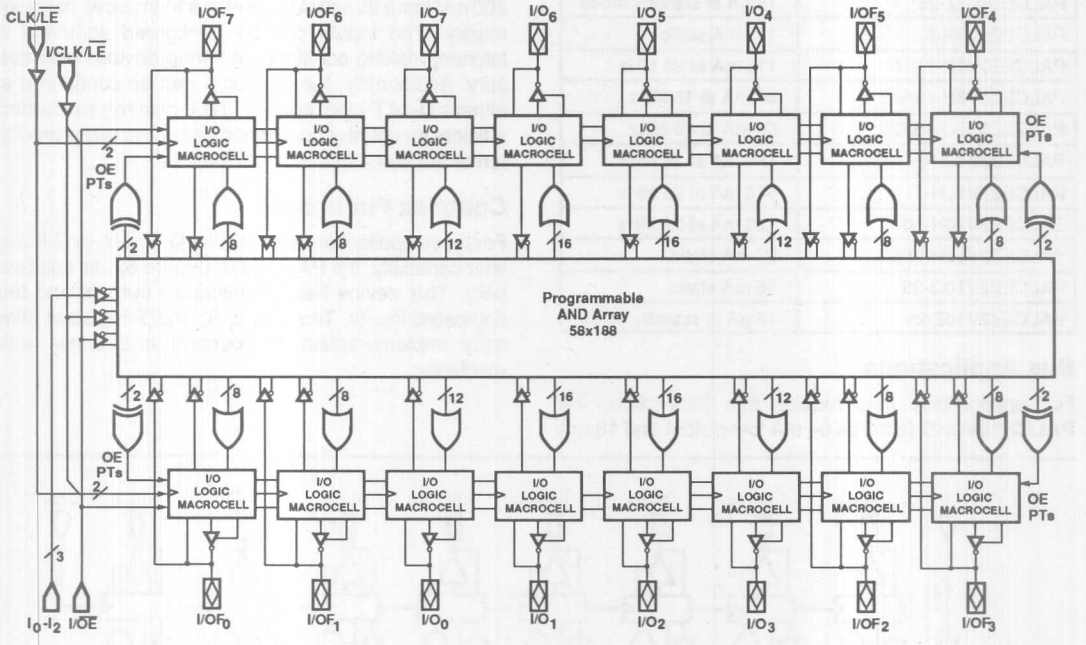


Figure 7. PALCE29M16 Block Diagram

The macrocells (Figure 8) can be configured as latches or registers. Latch operation allows the flip-flop in the macrocell to become transparent while the latch is enabled. When the latch is disabled, the flip-flop will hold the current state. This kind of operation is useful in sample and hold applications. Also, the register or latch may be used with the macrocell input pin for synchronizing signals. The active level of the latch enable, as well as the clock edge (rising or falling) are both programmable.

Like the PALCE22V10, there is varied product term distribution among the macrocells. Also, preload capability is available using a global product term to define the preload condition. Preload capability allows arbitrary states to be loaded directly into the register, making it unnecessary to cycle through long, complex vector sequences to get the device in a particular state. This is normally only performed by the device programmer when it performs functional tests. The preload product term allows preload to be engaged by hand, without the need for supervoltages (voltages above V_{CC} needed to engage preload on most PLDs).

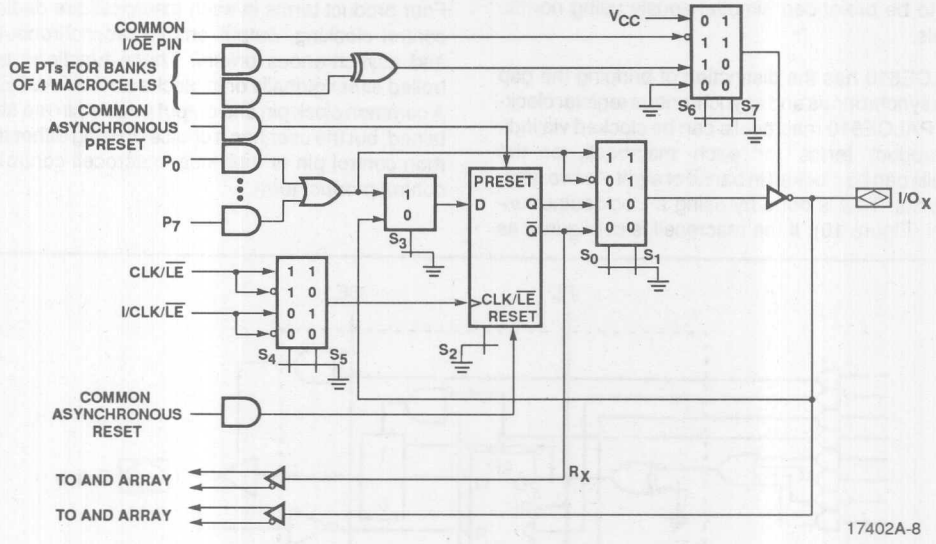


Figure 8. PALCE29M16 Macrocell Diagram

Asynchronous Applications

Starting at the top of the flow chart again, but this time taking the path for asynchronous applications, you will find **PALCE20RA10.** The PALCE20RA10 is the simplest of the asynchronous devices. Each macrocell (Figure 9) is clocked individually using one product term per macrocell. Also, reset, preset, and output enable are controlled individually with one product term each. There is also a global output enable pin which is combined with the product term enable to determine if the output is enabled or disabled.

A dedicated global preload pin allows all registered macrocells to be preloaded simultaneously using normal TTL levels.

The PALCE610 has the distinction of bridging the gap between synchronous and asynchronous register clocking. The PALCE610 macrocells can be clocked via individual product terms for each macrocell, or the macrocells can be clocked in banks of eight via two dedicated clocks. This is done by using a clock/output enable mux (Figure 10). If the macrocell is configured as combinatorial or as a synchronous register, output enable/disable is controlled by a product term. If asynchronous register mode is desired, the same product term is used as a clock and the macrocell is always enabled.

As mentioned above, the PALCE610 can act as a synchronous or asynchronous PAL device. As shown, a special function product term can be steered to control either the output enable or the macrocell clock. In the latter mode, each register can be individually clocked.

If your application requires the basic features of the PALCE29M16, except with individual macrocell control, the **PALCE29MA16** (Figure 11) should be considered. Four product terms in each macrocell are dedicated to control clocking, output enable, asynchronous reset, and asynchronous preset. These functions are controlled either globally or in blocks on the PALCE29M16. A common clock pin and output enable pin are still maintained, but the user has a choice of using either the common control pin or individual macrocell control via the control product term.

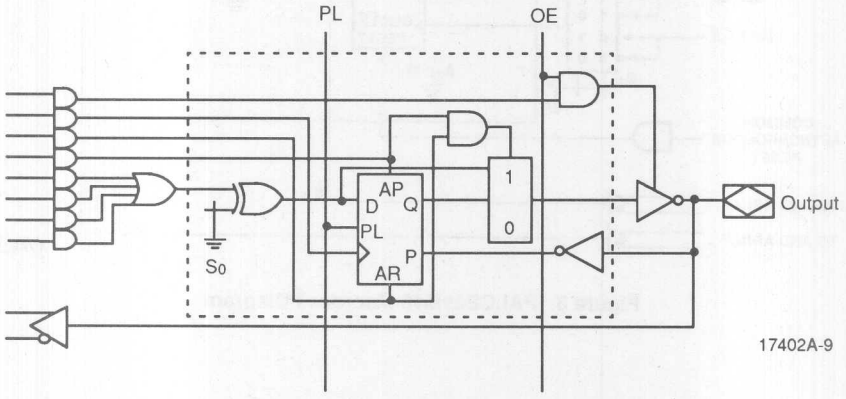


Figure 9. PALCE20RA10 Macrocell Diagram

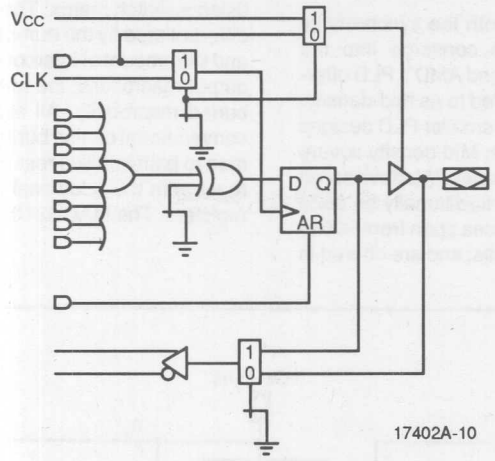


Figure 10. PALCE610 Macrocell (Configured as a D-Register) with the Output Enable/Clock Mux

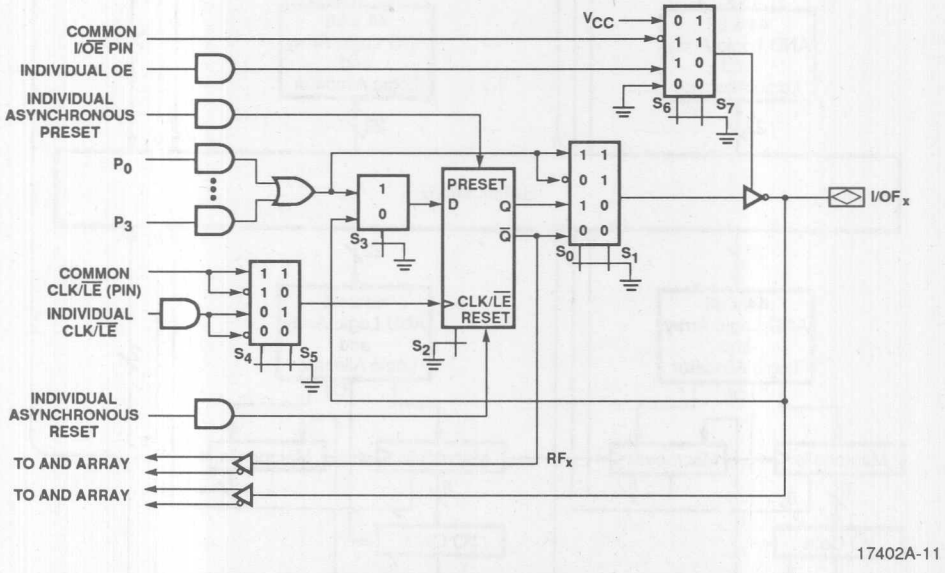


Figure 11. PALCE29MA16 Macrocell

MACH Devices

At the bottom of the flow chart, both the synchronous and asynchronous design paths converge into the MACH Family. MACH devices extend AMD's PLD offerings into the realm of what is referred to as mid-density. Mid-density devices allow multiple smaller PLD designs to be consolidated into one device. Mid-density covers replacement of just a couple of smaller PAL devices, all the way up to designs that would traditionally be done with small gate arrays. These devices span from 900 to 3600 gates, with 32 to 64 macrocells, and are offered in 44- to 84-pin packages.

MACH devices use PAL blocks that are interconnected using a switch matrix. The members of the families are differentiated by the number of pins, macrocells, clocks, and the amount of interconnect. The MACH 1 family has output macrocells; the MACH 2 family has output and buried macrocells. All signals, whether registered or combinatorial can be buried. The basic macrocell, common to both families resembles the PALCE22V10 macrocell with the additional choice of using D- or T-type registers. The MACH210 is illustrated in Figure 12.

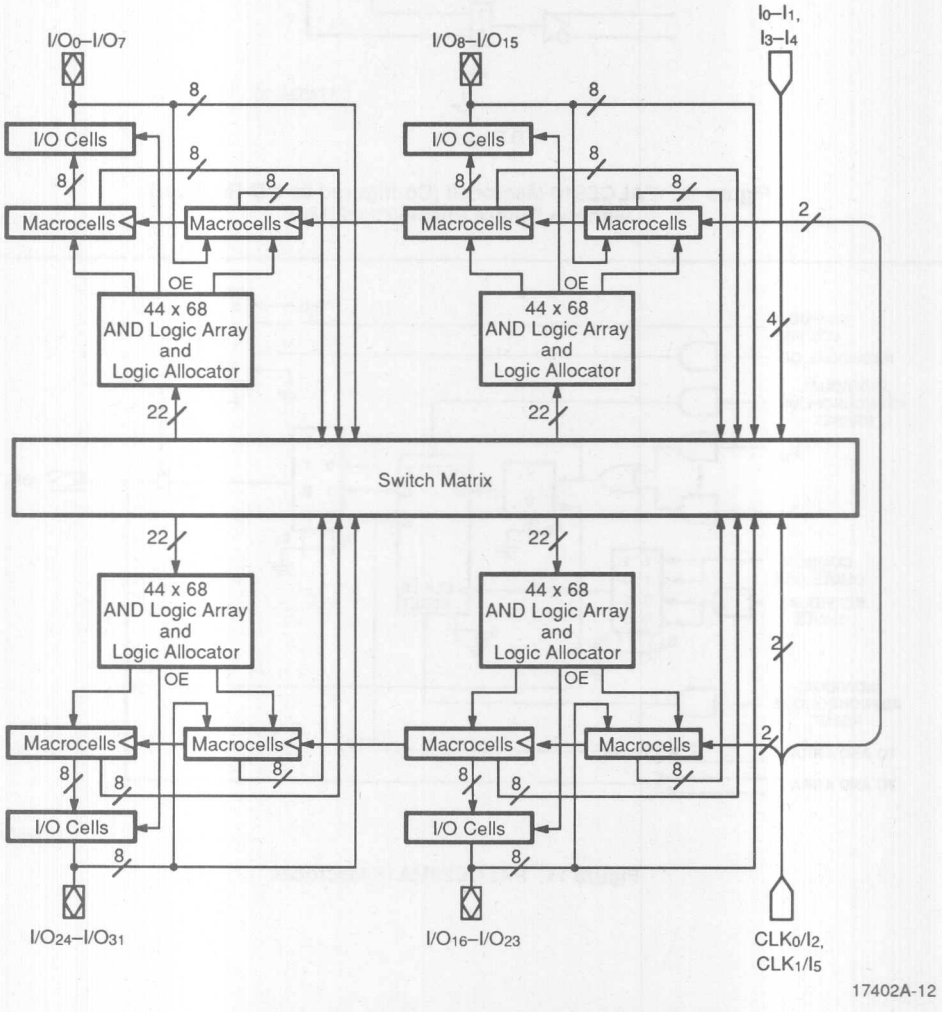


Figure 12. MACH210 Block Diagram

Both synchronous and asynchronous versions are available. The asynchronous MACH215 macrocell looks more like a PALCE20RA10 macrocell, rather than PALCE22V10 type macrocells. The synchronous devices are better suited to structured designs; the asynchronous MACH215 is better suited for random logic collection.

All MACH devices have the advantage of fast (10, 12, 15, and 20 ns), predictable timing, which is a unique advantage when compared to other mid-density PLDs.

SUMMARY

Selecting the appropriate PLD for a given application involves matching your requirements with various device capabilities. Following the guidelines in this article along with the "CMOS PAL Selection Route Map" makes it easier.

AMD's wide array of electrically-erasable CMOS PLDs, combined with strong third party support through our FusionPLD^{SM} relationships, means an excellent selection of devices, software, and programming hardware. This gives you a virtual toolbox of solutions for your system logic requirements, along with the strong technical support you expect.

COMMERCIAL PLDs FOR INDUSTRIAL APPLICATIONS

Advanced Micro Devices

Customers have expressed an interest in using AMD programmable logic devices over the industrial temperature range. To serve your need, we recommend the following:

1. Use any standard commercial device from the following family datasheets:
   PALCE16V8
   PALCE20V8
   PALCE22V10
   PALCE610
2. Slow down all commercial timing parameters by 20%.
3. Add 20 mA to the commercial I_{CC}.

All standard AMD warranties will apply to products used as noted above at V_{CC} of +5 V ±10% over the temperature range of –40°C to 85°C.

This approach will allow you to use broadly available commercial devices to fill your industrial temperature needs at no price premium. We are able to assure the performance to specification of these products since they are characterized and monitored over the full military temperature range (–55°C to 125°C).

CHAPTER

2 PAL DEVICE DATA SHEETS

PAL16R8 Family 2-3
PALCE16V8 Family 2-48
PALLV16V8-10 2-79
PALCE16V8Z Family 2-95
PALLV16V8Z Family 2-115
AmPAL18P8B/AL/A/L 2-155
PAL20R8 Family 2-165
PALCE20V8 Family 2-204
PALCE20RA10H-20 2-236
AmPAL22P10B/AL/A 2-249
PAL22V10 Family/AmPAL22V10A 2-258
PALCE22V10 Family 2-286
PALCE22V10Z Family 2-313
PALLV22V10Z-25 2-331
PALCE24V10H-15/25 2-345
PALCE26V12-15/20 2-360
PALCE29M16H-25 2-377
PALCE29MA16H-25 2-399
PALCE610 Family 2-424


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PAL16R8 Family

20-Pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 4.5 ns maximum propagation delay
- Popular 20-pin architectures: 16L8, 16R8, 16R6, 16R4
- Programmable replacement for high-speed TTL logic
- Register preload for testability
- Power-up reset for initialization
- Extensive third-party software and programmer support through FusionPLD partners
- 20-Pin DIP and PLCC packages save space
- 28-Pin PLCC-4 package provides ultra-clean high-speed signals

GENERAL DESCRIPTION

The PAL16R8 Family (PAL16L8, PAL16R8, PAL16R6, PAL16R4) includes the PAL16R8-5/4 Series which provides the highest speed in the 20-pin TTL PAL device family, making the series ideal for high-performance applications. The PAL16R8 Family is provided with standard 20-pin DIP and PLCC pinouts and a 28-pin PLCC pinout. The 28-pin PLCC pinout contains seven extra ground pins interleaved between the outputs to reduce noise and increase speed.

The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array.

The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

— Variable input/output pin ratio
— Programmable three-state outputs
— Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. Once the PAL device is programmed and verified, an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

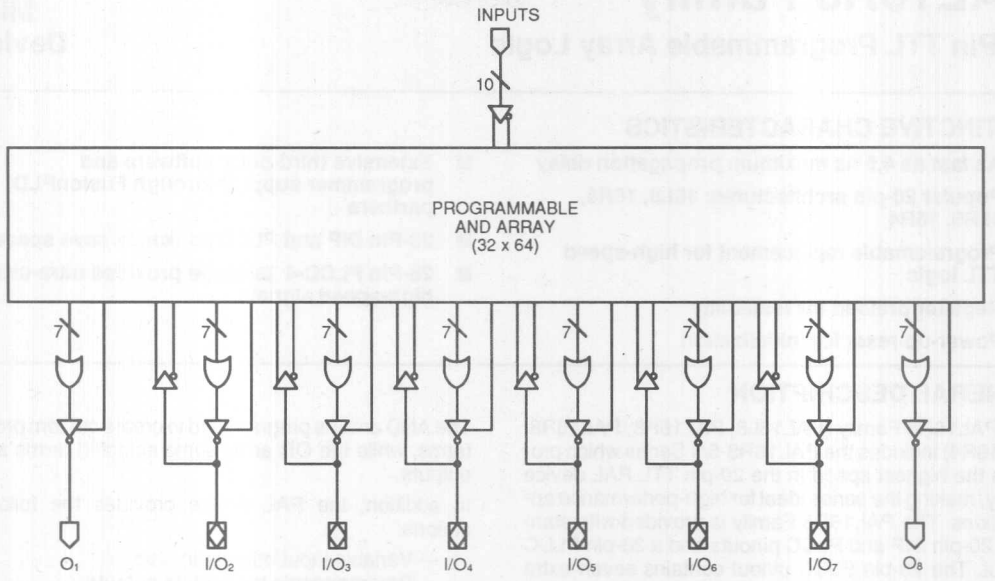
PRODUCT SELECTOR GUIDE

Device	Dedicated Inputs	Outputs	Product Terms/ Output	Feedback	Enable
PAL16L8	10	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL16R8	8	8 reg.	8	reg.	pin
PAL16R6	8	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL16R4	8	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Publication# 16492 Rev. B Amendment/0
Issue Date: June 1993

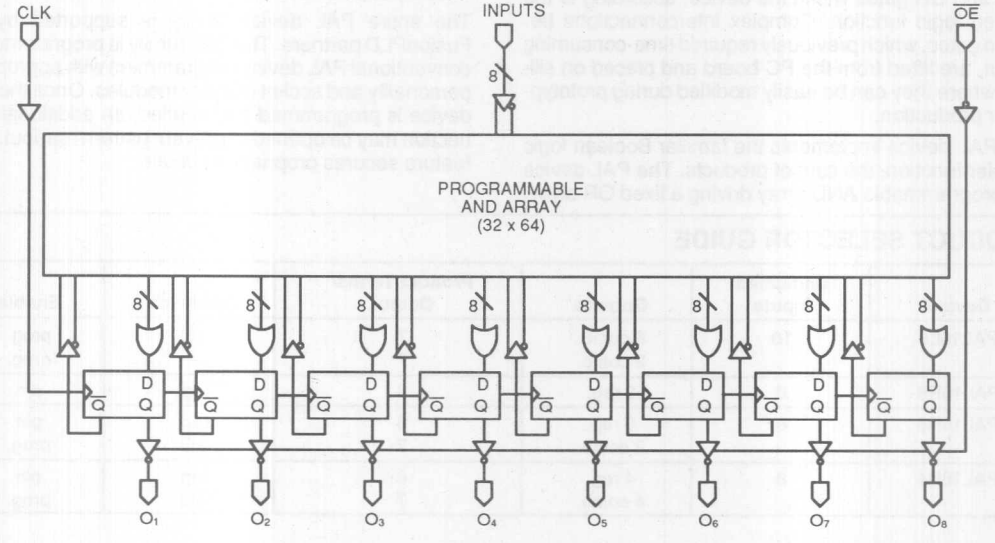
BLOCK DIAGRAMS

PAL16L8



16492B-1

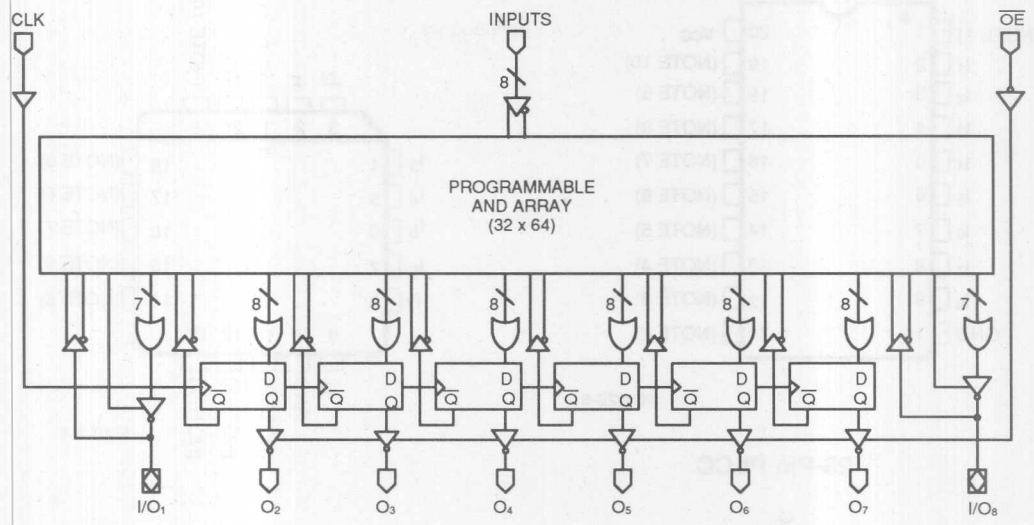
PAL16R8



16492B-2

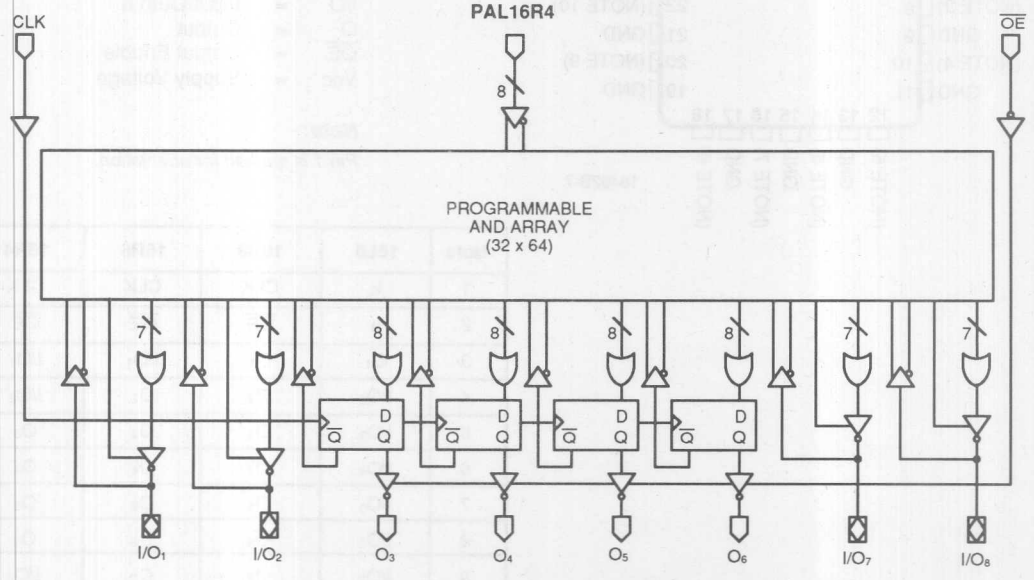
BLOCK DIAGRAMS

PAL16R6



16492B-3

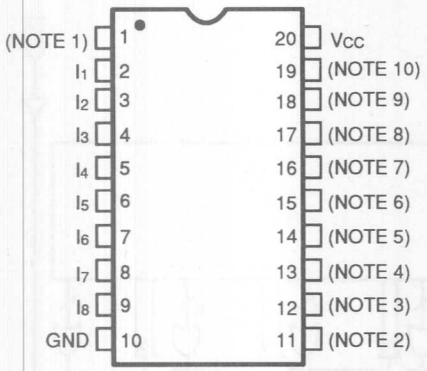
PAL16R4



16492B-4

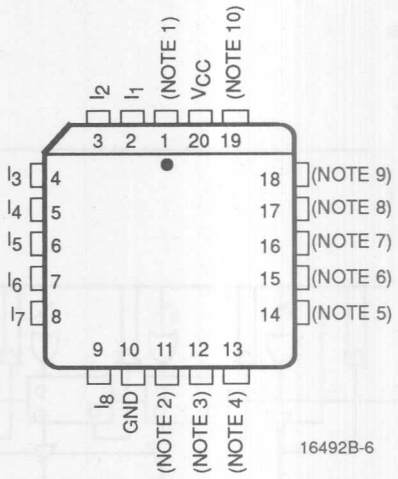
Top View

DIP



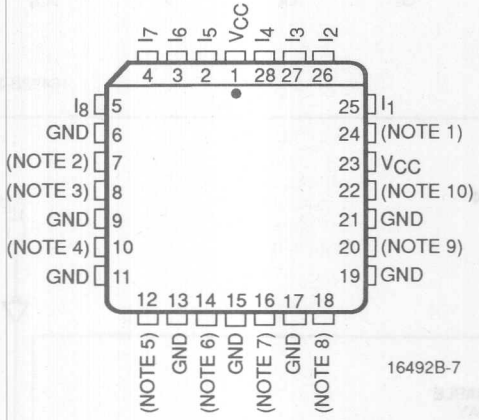
16492B-5

20-Pin PLCC



16492B-6

28-Pin PLCC



16492B-7

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
O	=	Output
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

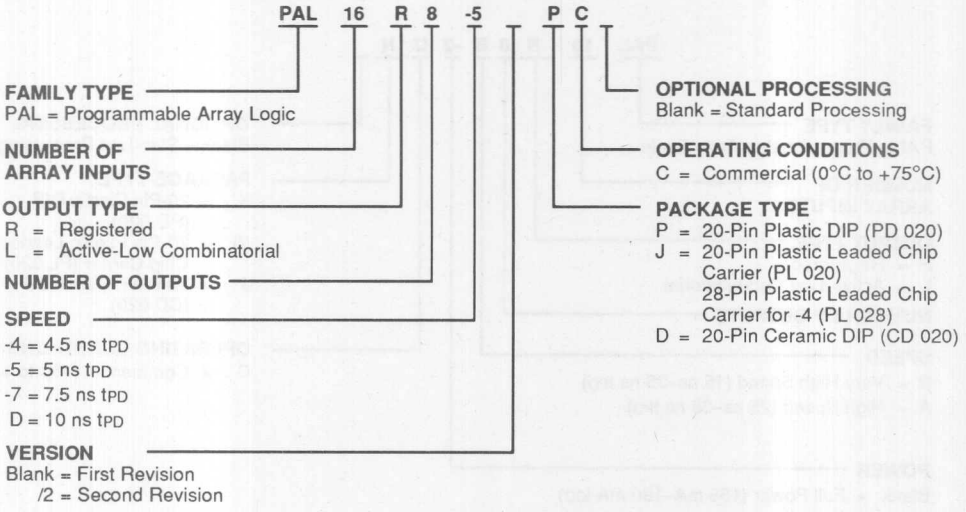
Note:

Pin 1 is marked for orientation.

Note	16L8	16R8	16R6	16R4
1	I_0	CLK	CLK	CLK
2	I_9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



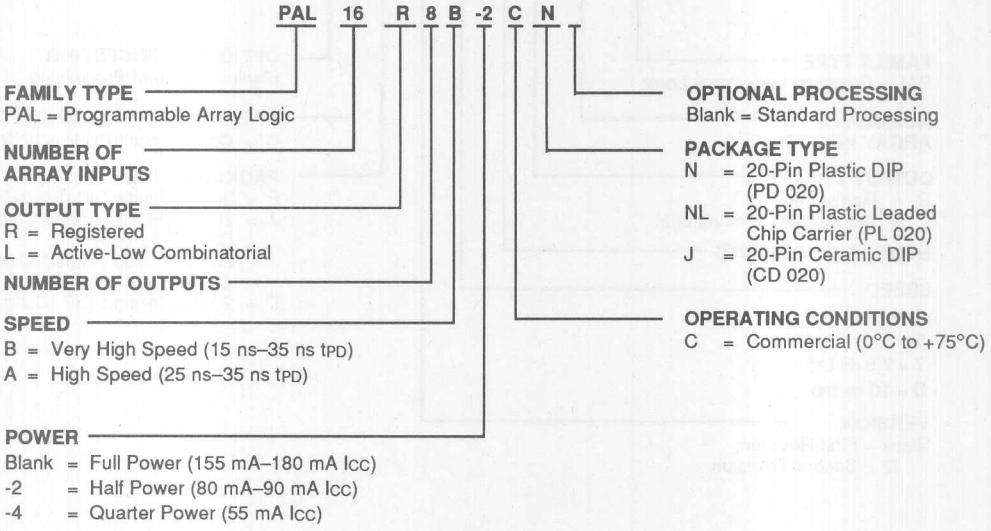
Valid Combinations	
PAL16L8	-5PC, -5JC, -4JC
PAL16R8	
PAL16R6	
PAL16R4	
PAL16L8-7	PC, JC, DC
PAL16R8-7	
PAL16R6-7	
PAL16R4-7	
PAL16L8D/2	PC, JC
PAL16R8D/2	
PAL16R6D/2	
PAL16R4D/2	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Commercial Products (MMI Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	B, B-2, A, B-4	CN, CNL, CJ
PAL16R8		
PAL16R6		
PAL16R4		

Valid Combinations

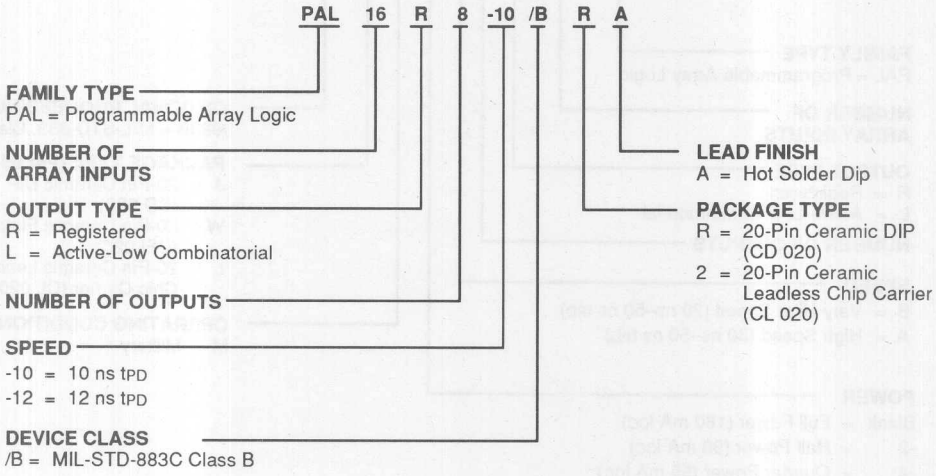
Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: *Marked with MMI logo.*

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	-10, -12	/BRA, /B2A
PAL16R8		
PAL16R6		
PAL16R4		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Military Burn-In

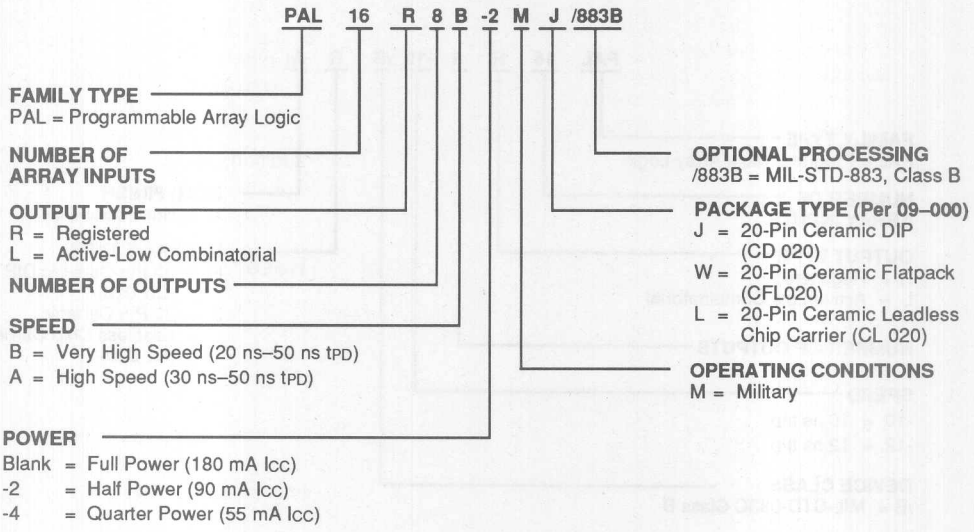
Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ORDERING INFORMATION
APL Products (MMI Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	B, B-2, A, B-4	MJ/883B, MW/883B, ML/883B
PAL16R8		
PAL16R6		
PAL16R4		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: *Marked with MMI logo.*

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Standard 20-Pin PAL Family

The standard bipolar 20-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Pinouts

The PAL16R8 Family is available in the standard 20-pin DIP and PLCC pinouts and the PAL16R8-4 Series is available in the new 28-pin PLCC pinout. The 28-pin PLCC pinout gives the designer the cleanest possible signal with only 4.5 ns delay.

The PAL16R8-4 pinout has been designed to minimize the noise that can be generated by high-speed signals. Because of its inherently shorter leads, the PLCC package is the best package for use in high-speed designs. The short leads and multiple ground signals reduce the effective lead inductance, minimizing ground bounce. Placing the ground pins between the outputs optimizes the ground bounce protection, and also isolates the outputs from each other, eliminating cross-talk. This pinout can reduce the effective propagation delay by as much as 20% from a standard DIP pinout. Design files for PAL16R8-4 Series devices are written as if the device had a standard 20-pin DIP pinout for most design software packages.

Variable Input/Output Pin Ratio

The registered devices have eight dedicated input lines, and each combinatorial output is an I/O pin. The PAL16L8 has ten dedicated input lines and six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin and may be configured as a dedicated input if the output buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Register Preload

The register on the PAL16R8 Family can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL16R8 Family will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Security Fuse

After programming and verification, a PAL16R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

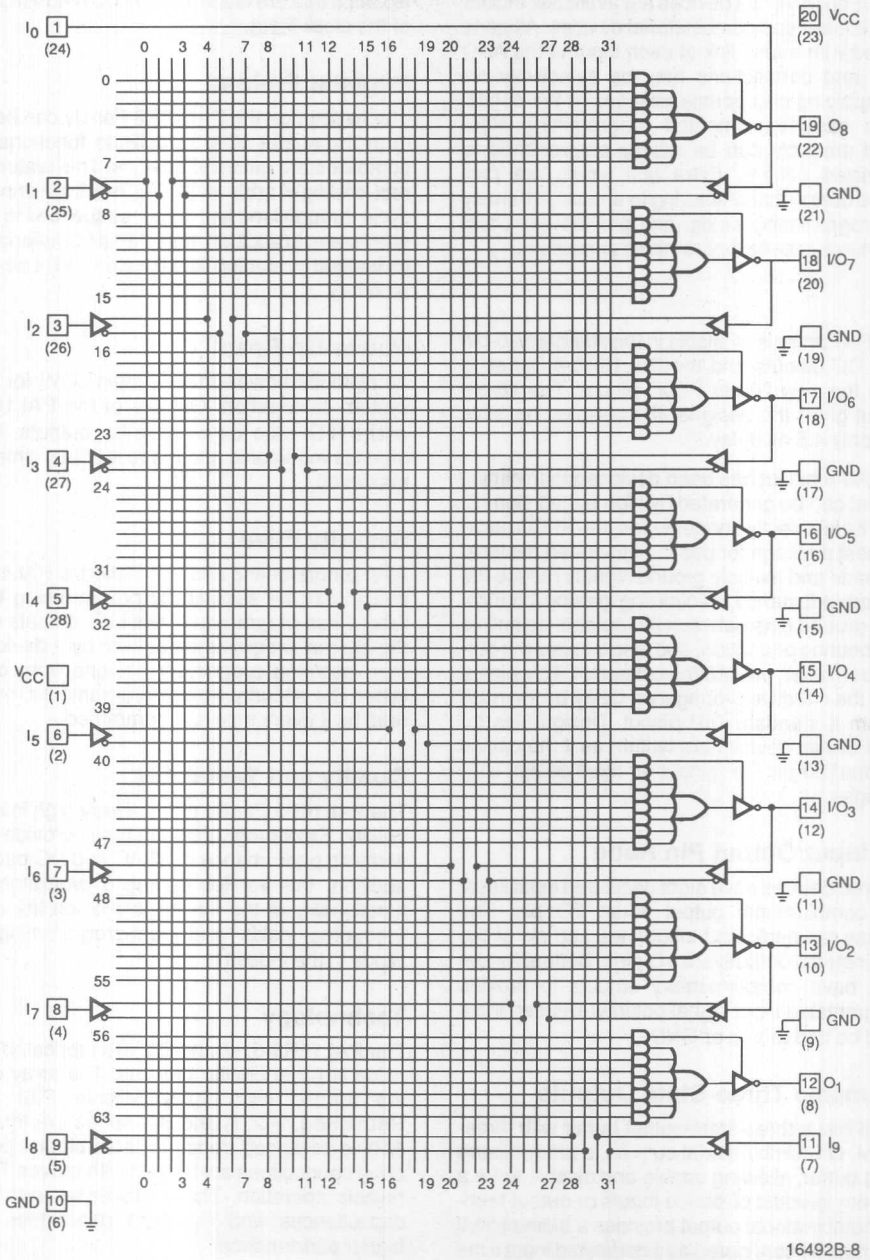
The PAL16R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL16R8-5, -7 and D/2 are fabricated with AMD's oxide isolated bipolar process. The array connections are formed with highly reliable PtSi fuses. The PAL16R8B, B-2, A and B-4 series are fabricated with AMD's advanced trench-isolated bipolar process. The array connections are formed with proven TiW fuses for reliable operation. These processes reduce parasitic capacitances and minimum geometries to provide higher performance.

LOGIC DIAGRAM
DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

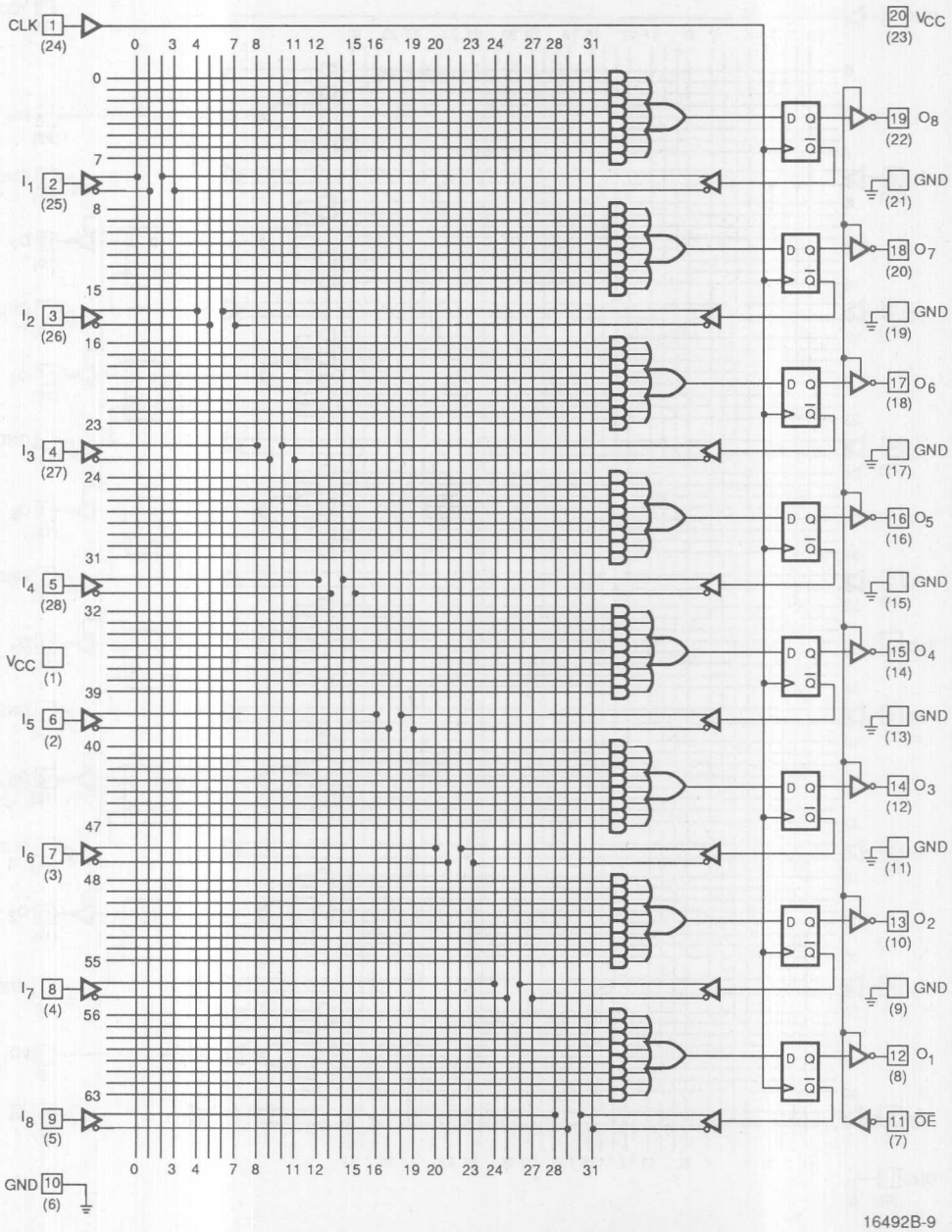
16L8 (-4)



16492B-8

LOGIC DIAGRAM
DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

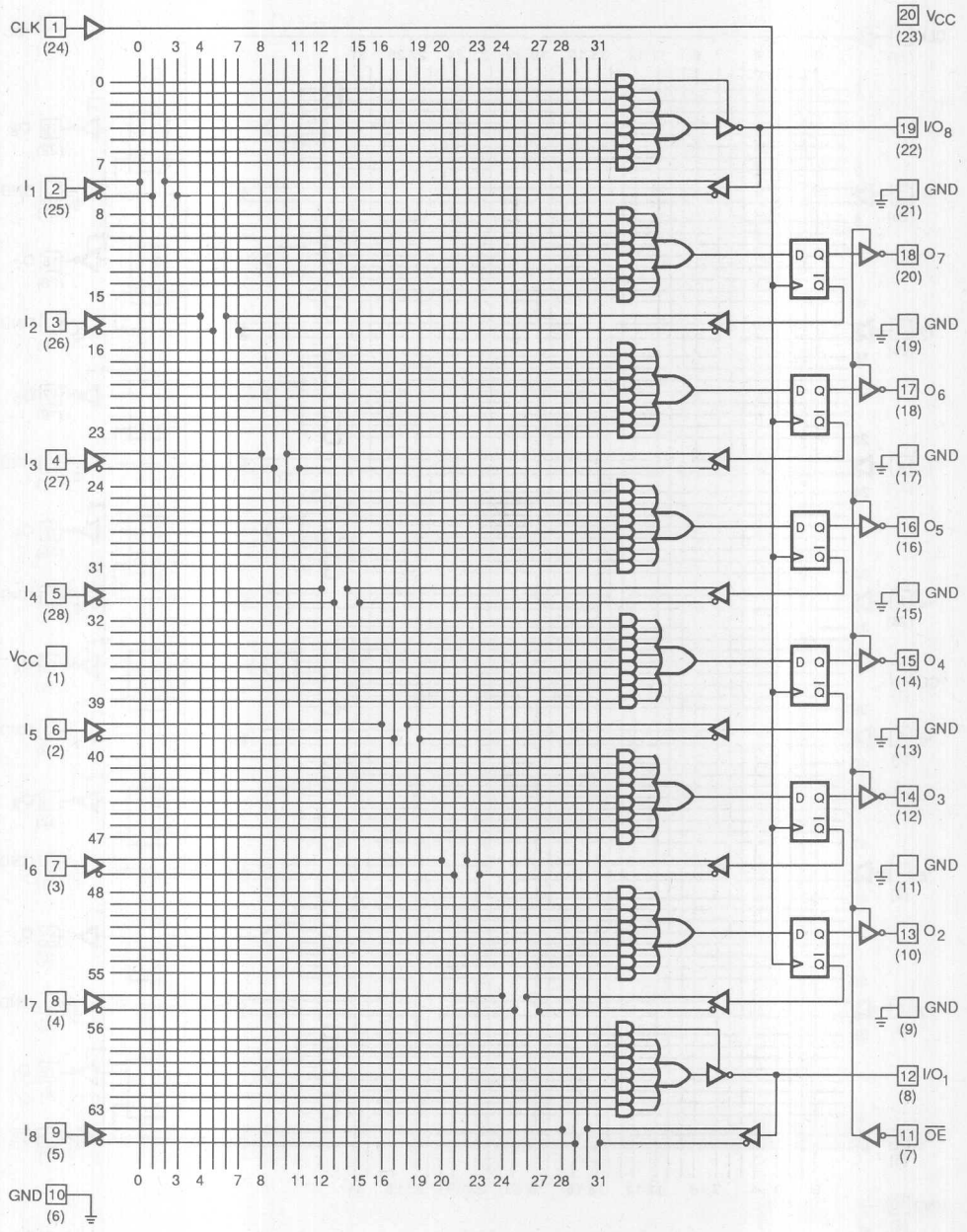
16R8 (-4)



LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

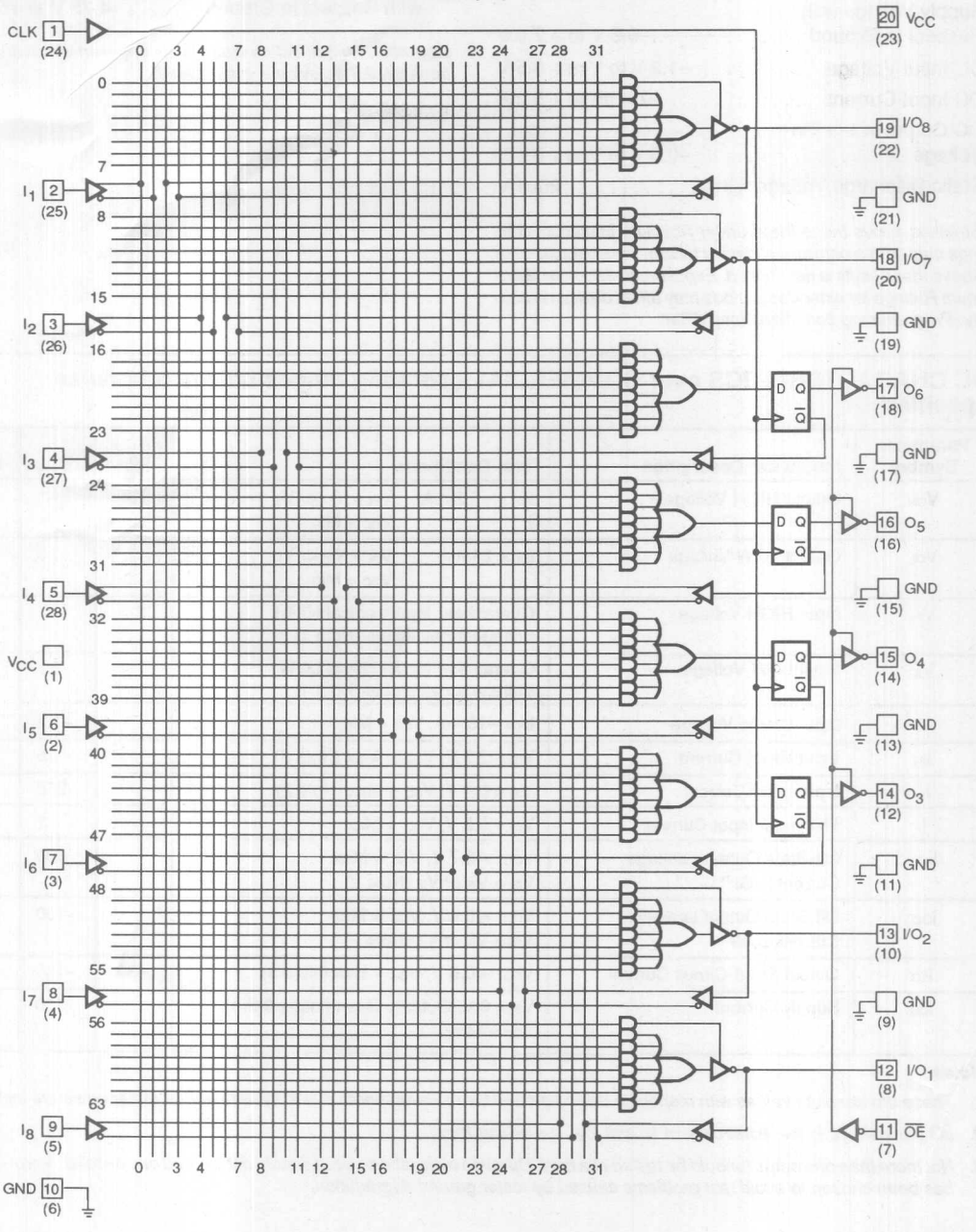
16R6 (-4)



16492B-10

LOGIC DIAGRAM
DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R4 (-4)



16492B-11

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature with Power Applied ..... –65°C to +150°C

Storage Temperature ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to + 7.0 V

DC Input Voltage ..... –1.2 V to V_{CC} + 0.5 V

DC Input Current ..... –30 mA to + 5 mA

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		210	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

C_{IN}	Input Capacitance	CLK, OE	V_{IN} = 2.0 V	V_{CC} = 5.0 V	8	pF
		I_1–I_8		T_A = 25°C	5	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-5		-4		Unit
					Min (Note 3)	Max	Min (Note 3)	Max	
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R8, 16R4	1	5	1	4.5	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	4.5		4.5		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output				1	4.0	1	3.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)					1		0.5	ns
t_{WL}	Clock Width	LOW			4		4		ns
t_{WH}		HIGH			4		4		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		117		125		MHz
		Internal Feedback (f_{CNT})			125		125		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		125		125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	6.5	1	6.5	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	5	1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	2	6.5	2	6.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				2	5	2	5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Skew testing takes into account pattern and switching direction differences between outputs.*
5. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –1.2 V to + 7.0 V

DC Input Current . . . . . –30 mA to + 5 mA

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	3	7.5	ns
		1 Output Switching			3	7	
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	7		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				1	6.5	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1	ns
t_{WL}	Clock Width	LOW			5		ns
t_{WH}		HIGH			5		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		74		MHz
		Internal Feedback (f_{CNT})			100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	8	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Skew is measured with all outputs switching in the same direction.*
5. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to + 7.0 V

DC Input Voltage ..... –1.5 V to + 5.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to + 5.5 V

Static Discharge Voltage ..... 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock				10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	7	ns
t_{WL}	Clock Width	LOW			8		ns
t_{WH}		HIGH		16R8, 16R6,	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	16R4	58.8		MHz
		Internal Feedback (f_{CNT})			60		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6,	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			16R4	3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		15	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					12	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					15	ns
t_{EA}	Input to Output Enable Using Product Term Control			16R8, 16R6, 16R4		15	ns
t_{ER}	Input to Output Disable Using Product Term Control					15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . . −55°C to +125°C

Supply Voltage with Respect to Ground . . . . . −0.5 V to +7.0 V

DC Input Voltage . . . . . −1.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . −0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		−100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		90	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			16R8, 16R6, 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Calculated from measured f_{MAX} internal.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –1.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage		I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage		I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage		Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage		I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current		V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current		V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current		V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH		V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW		V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current		V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	16L8	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		155	mA
		16R8/6/4			180	

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{CC} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			16R8, 16R6, 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Calculated from measured f_{MAX} internal.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.5 V to +5.5 V

DC Output or I/O Pin Voltage . . . . . 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–250	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		55	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V as been chosen to avoid test problems caused by tester ground degradation.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		35	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	35		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		16		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					25	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4		35	ns
t_{ER}	Input to Output Disable Using Product Term Control					35	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –1.2 V to +5.5 V

DC Input Current ..... –30 mA to +5 mA

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	Corner Pins	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	10	pF
		Middle Pins			5	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V		9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				-10 Min (Note 3)	-10 Max	-12 Min (Note 3)	-12 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	3	10	3	12	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	10		10		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output				3	9	3	11	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1		1	ns
t_{WL}	Clock Width	LOW			8		8		ns
t_{WH}		HIGH			8		8		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		52.6		47.6		MHz
		Internal Feedback (f_{CNT})			60.6		60.6		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		62.5		62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 5)				3	10	3	12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 5)				3	10	3	12	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)			16L8, 16R6, 16R4	3	10	3	12	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				3	10	3	12	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.*
4. *Skew is measured with all outputs switching in the same direction.*
5. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.5 V to +5.5 V

DC Output or I/O Pin Voltage . . . . . 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air . . . . . –55°C Min

Operating Case (T_C) Temperature . . . . . 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		10	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		20	ns
t_S	Setup Time from Input or Feedback to Clock			16L8, 16R6, 16R4	20		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					20	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –1.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		90	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			16L8, 16R6, 16R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					30	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to + 7.0 V

DC Input Voltage ..... –1.5 V to + 5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			16L8, 16R6, 16R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					30	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –1.5 V to + 5.5 V

DC Output or I/O Pin Voltage . . . . . 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air . . . . . –55°C Min

Operating Case (T_C) Temperature . . . . . 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–250	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		55	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

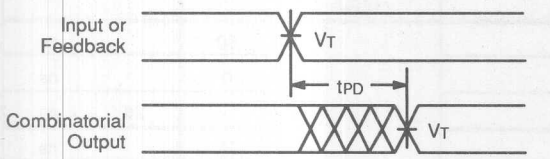
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		50	ns
t_S	Setup Time from Input or Feedback to Clock			16L8, 16R6, 16R4	50		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		13.3		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			16L8, 16R6, 16R4		45	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					45	ns

Notes:

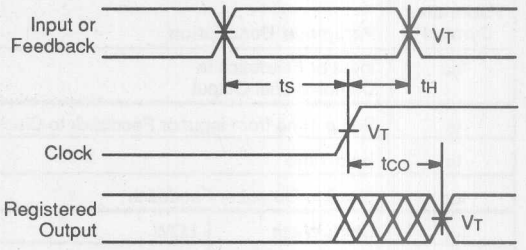
1. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

SWITCHING WAVEFORMS



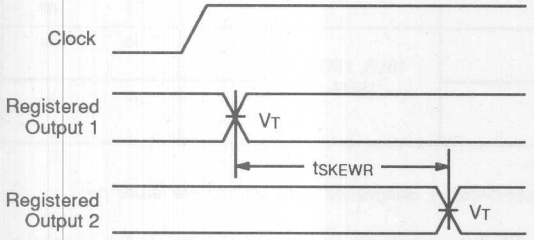
16492B-12

Combinatorial Output



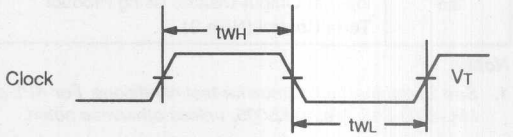
16492B-13

Registered Output



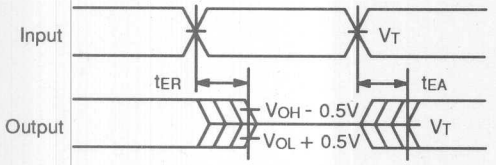
16492B-14

Registered Output Skew



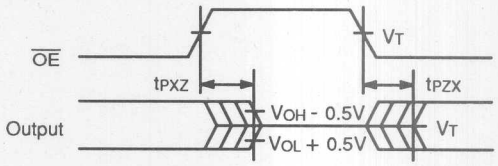
16492B-15

Clock Width



16492B-16

Input to Output Disable/Enable



16492B-17

$\overline{OE}$ to Output Disable/Enable

Notes:

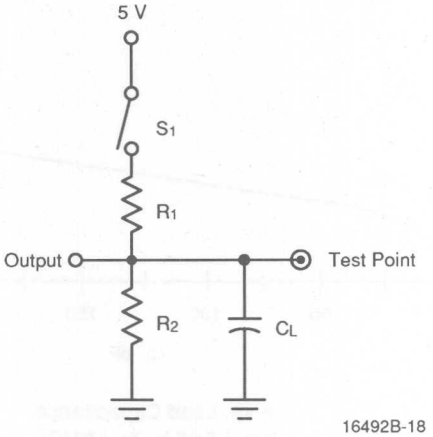
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2 ns–3 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

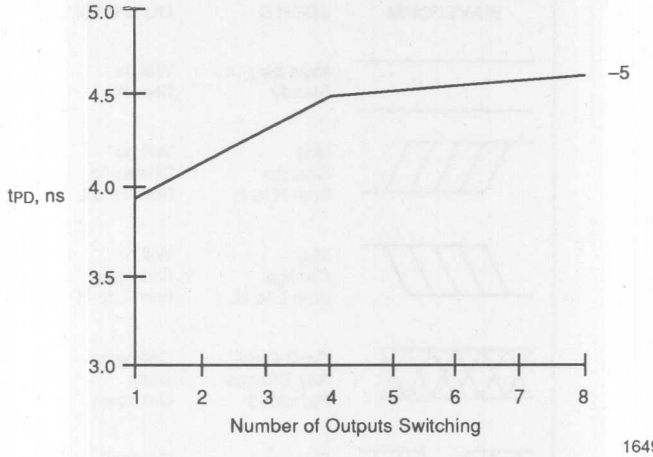


16492B-18

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	All but B-4: 200 Ω	All but B-4: 390 Ω	All but B-4: 390 Ω	All but B-4: 750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	B-4: 800 Ω	B-4: 1.56 kΩ	B-4: 800 Ω	B-4: 1.56 kΩ	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

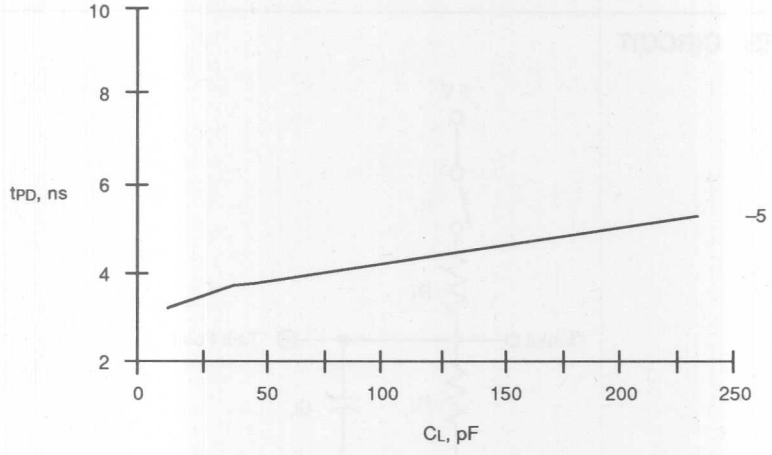
MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-5

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



16492B-12

t_{PD} vs. Number of Outputs Switching



16492B-13

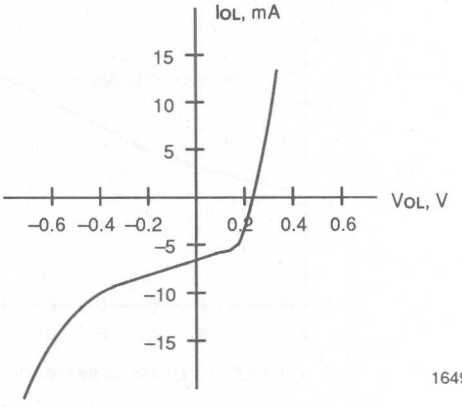
t_{PD} vs. Load Capacitance
V_{CC} = 5.25 V, T_A = 25°C

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.*

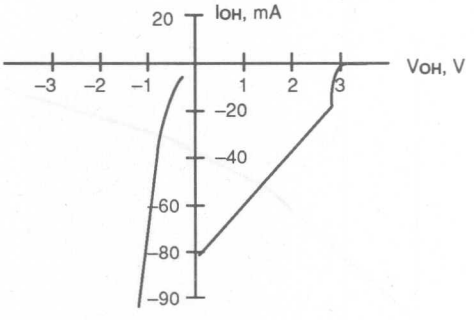
CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-4/5

V_{CC} = 5.0 V, T_A = 25°C



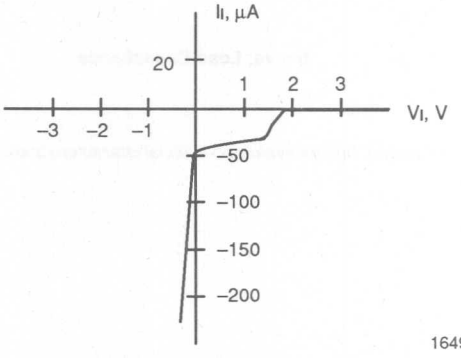
16492B-14

Output, LOW



16492B-15

Output, HIGH

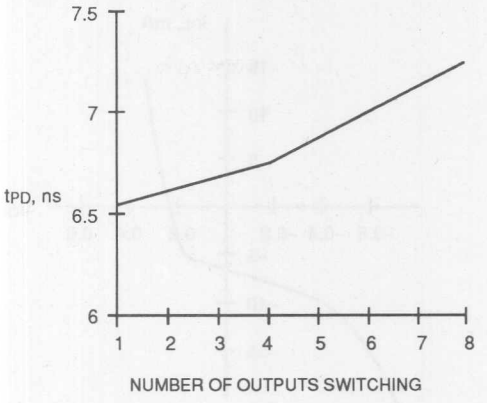


16492B-16

Input

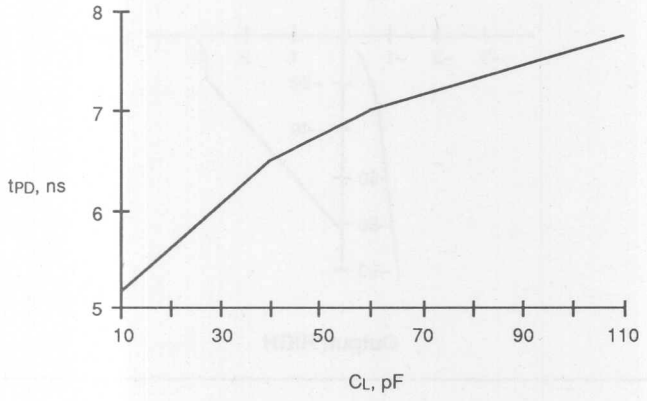
MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-7

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



16492B-12

t_{PD} vs. Number of Outputs Switching



16492B-13

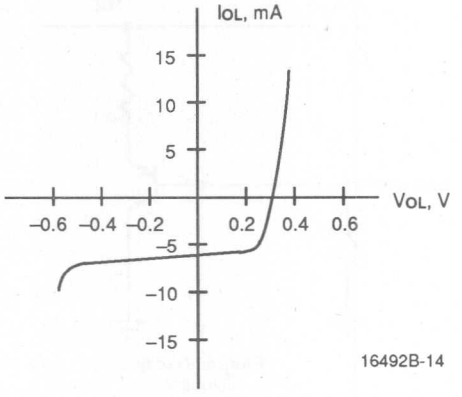
t_{PD} vs. Load Capacitance

Note:

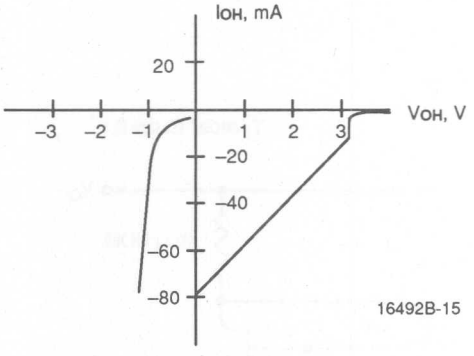
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.*

CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-7

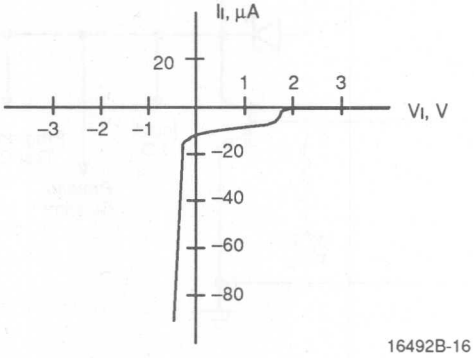
V_{CC} = 5.0 V, T_A = 25°C



Output, LOW



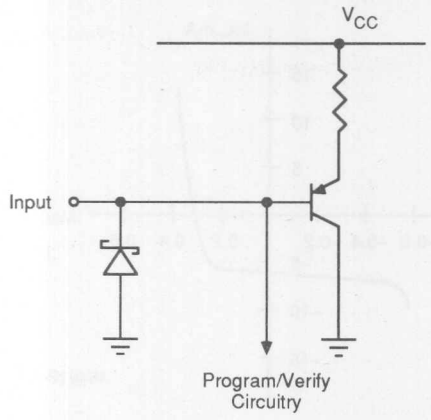
Output, HIGH



Input

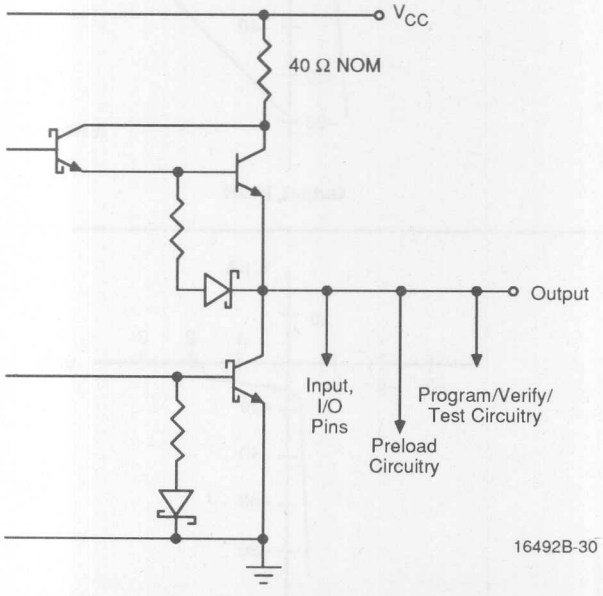
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



16492B-29

Typical Output



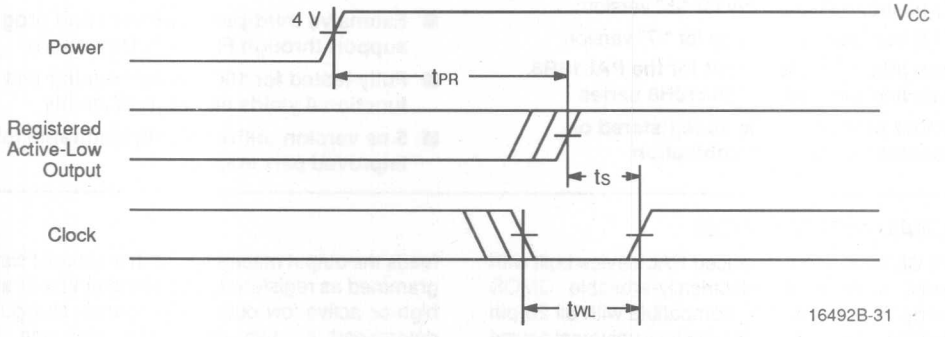
16492B-30

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PALCE16V8 Family

EE CMOS 20-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin, function and fuse-map compatible with all 20-pin GAL devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - 5 ns propagation delay for "-5" version
  - 7.5 ns propagation delay for "-7" version
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**
- **5 ns version utilizes a split leadframe for improved performance**

GENERAL DESCRIPTION

The PALCE16V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

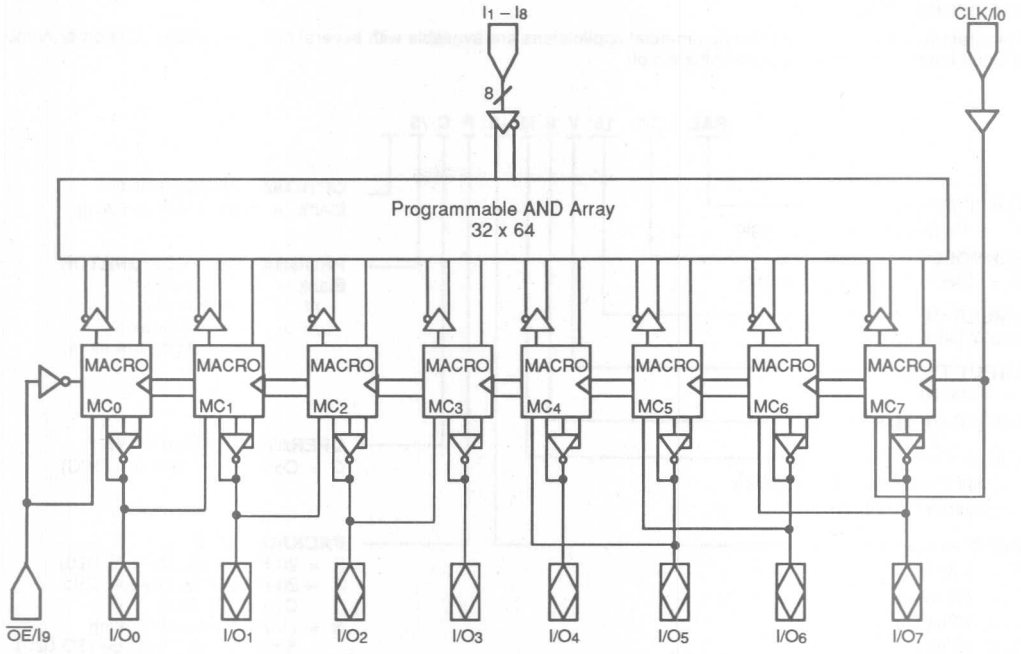
The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 16493 Rev. B Amendment /0
Issue Date: June 1993

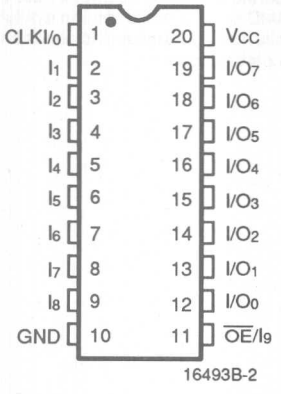
BLOCK DIAGRAM



16493B-1

CONNECTION DIAGRAMS
Top View

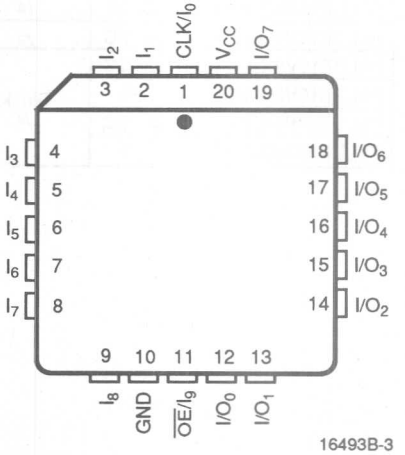
DIP/SOIC



16493B-2

Note: *Pin 1 is marked for orientation*

PLCC/LCC



16493B-3

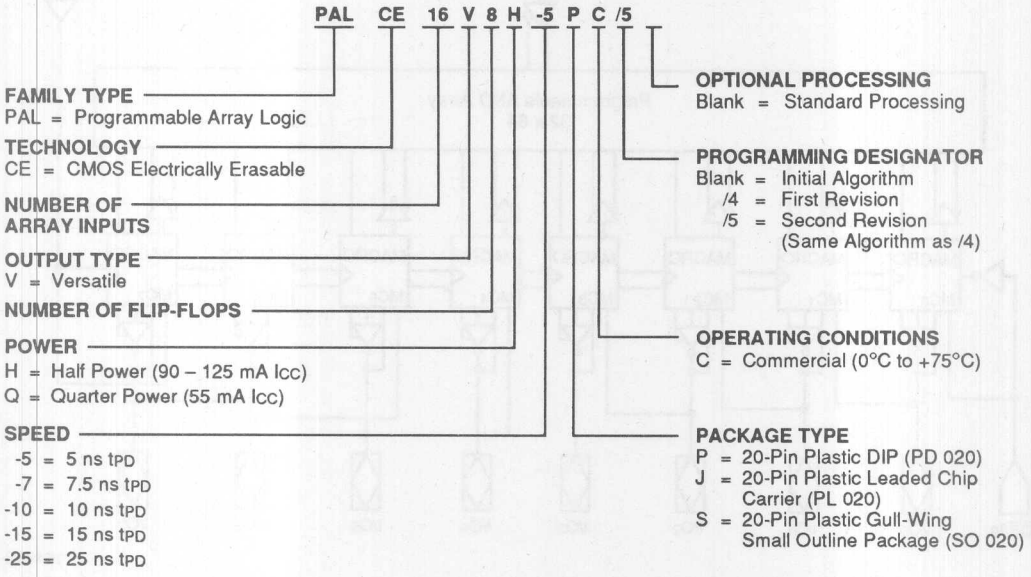
PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE16V8H-5	JC	/5
PALCE16V8H-7	PC, JC	
PALCE16V8H-10	PC, JC, SC	/4
PALCE16V8Q-10	PC, JC, SC	/5
PALCE16V8H-15	PC, JC, SC	Blank, /4
PALCE16V8Q-15	PC, JC	
PALCE16V8H-25	PC, JC, SC	
PALCE16V8Q-25	PC, JC	

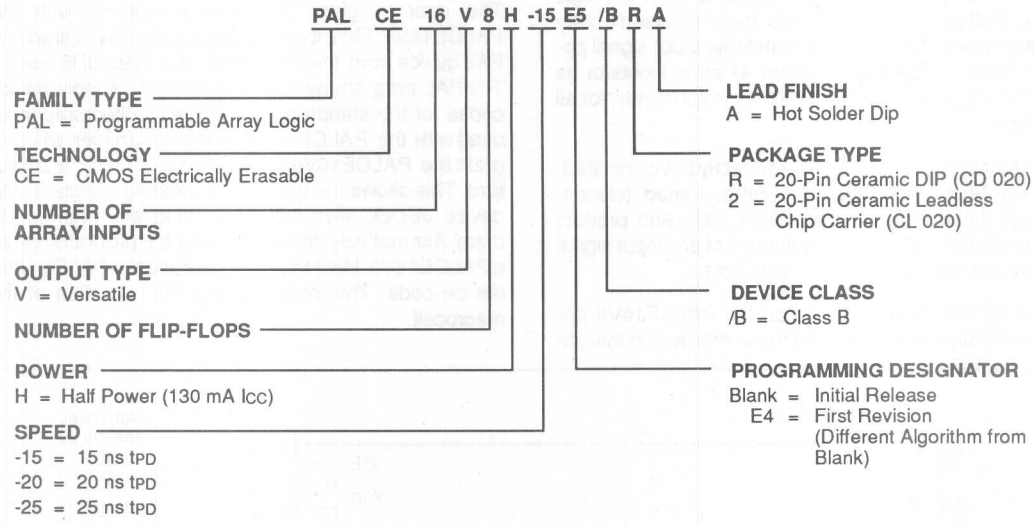
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products (Military)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE16V8H-15	E4	/BRA /B2A
PALCE16V8H-20	Blank, E4	
PALCE16V8H-25		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

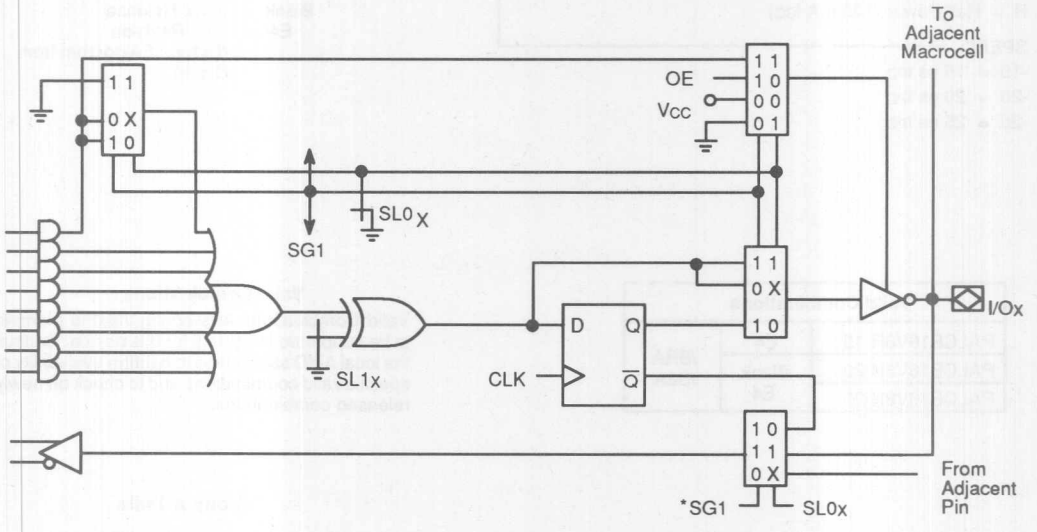
FUNCTIONAL DESCRIPTION

The PALCE16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

16493B-4

PALCE16V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 15 and 16. Pins 15 and 16 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

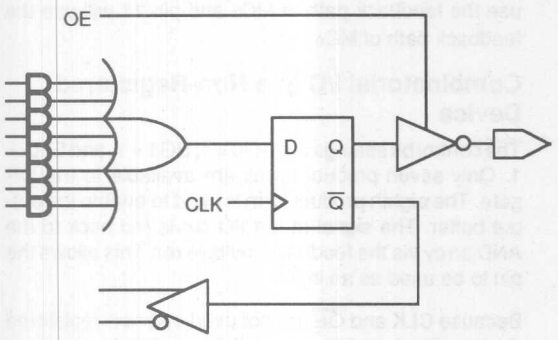
Table 1. Macrocell Configuration

SG0	SG1	SL0x	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

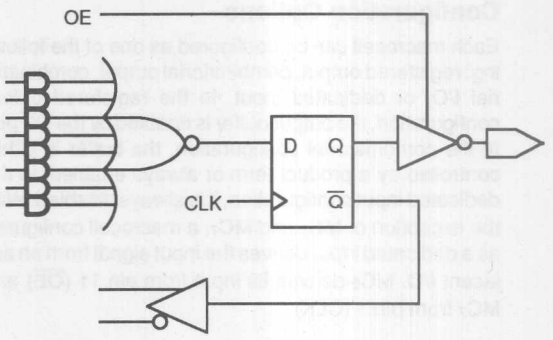
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

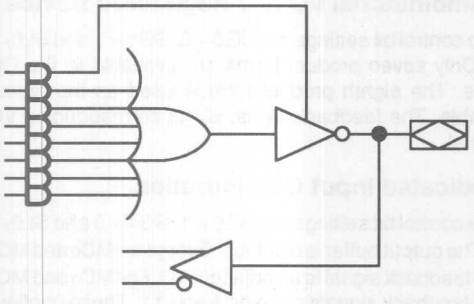
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



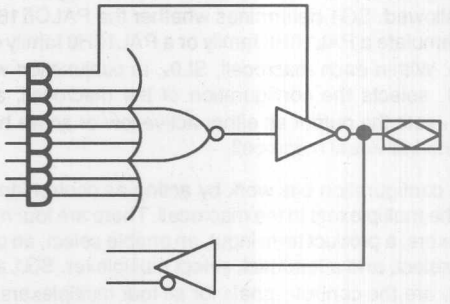
Registered Active Low



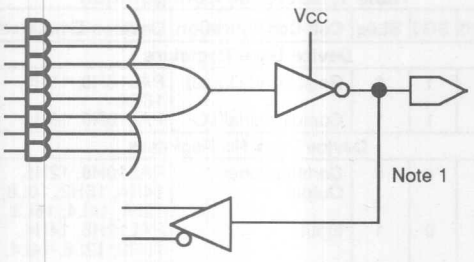
Registered Active High



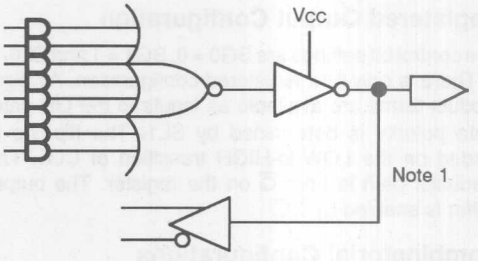
Combinatorial I/O Active Low



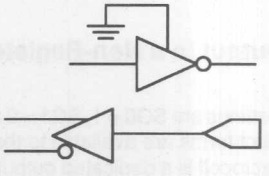
Combinatorial I/O Active High



Combinatorial Output Active Low



Combinatorial Output Active High



Dedicated Input

16493B-5

Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *This configuration is not available on pins 15 and 16.*

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

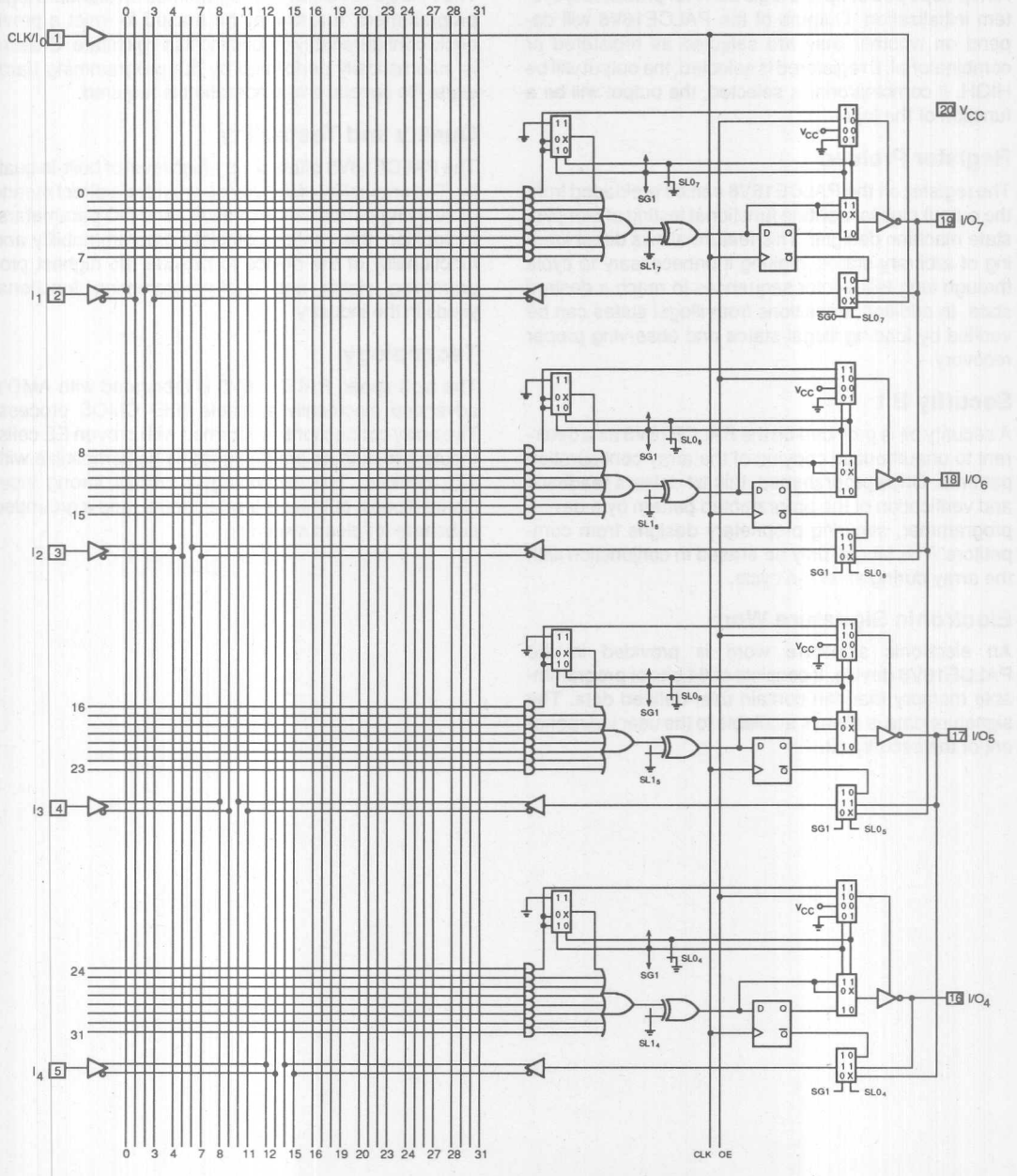
Quality and Testability

The PALCE16V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

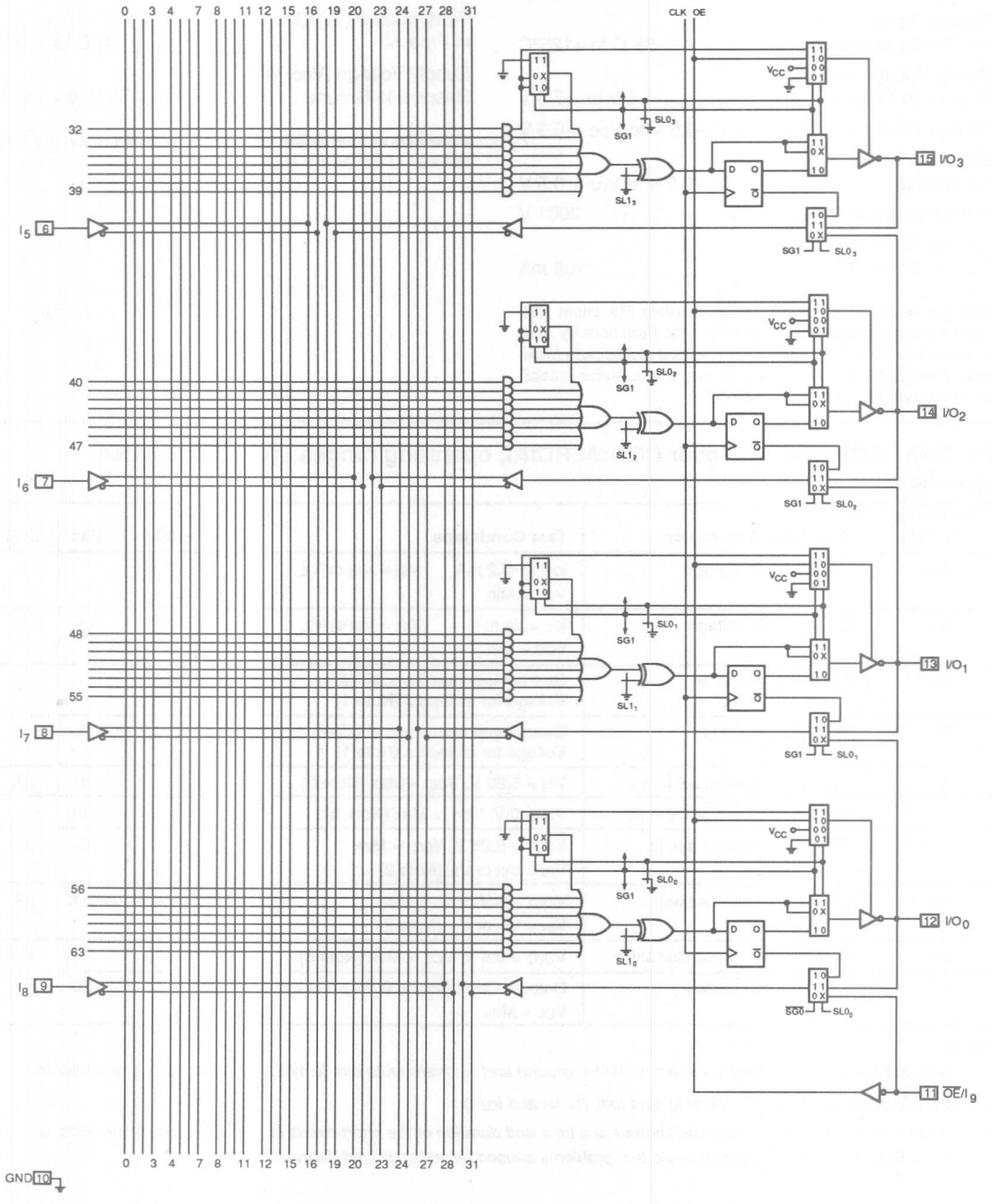
The high-speed PALCE16V8 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



16493B-6

LOGIC DIAGRAM (continued)



16493B-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Static)	Outputs Open (I_{OUT} = 0 mA), V_{IN} = 0 V V_{CC} = Max		125	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 5)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	5	ns
t_S	Setup Time from Input or Feedback to Clock			3		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		3		ns
t_{WH}		HIGH		3		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT})		166		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	166		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			2	6	ns
t_{ER}	Input to Output Disable Using Product Term Control			2	5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to + 7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 5)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output		8 Outputs Switching	3	7.5	ns
			1 Output Switching	3	7	ns
t_S	Setup Time from Input or Feedback			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	100		MHz
		Internal Feedback (f_{CNT})		125		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXA}	$\overline{OE}$ to Output Disable			1	6	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	9	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})		71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})		71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to + 7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback (f_{CNT})		50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		20	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_C = –55°C to +125°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C) . . . . . –55°C to +125°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Note:

1. *Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.*

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.0 V, V_{OUT} = 0.5 V (Note 5), T = 25°C	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		130	mA

Notes:

2. *For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input or Feedback to Clock			12		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				12	ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	41.6		MHz
		Internal Feedback (f_{CNT})		45.5		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				15	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_C = –55°C to +125°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

Operating Case Temperature (T_C) ..... –55°C to +125°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. *Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.*

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.0 V, V_{OUT} = 0.5 V (Note 5), T = 25°C	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz		130	mA

Notes:

2. *For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

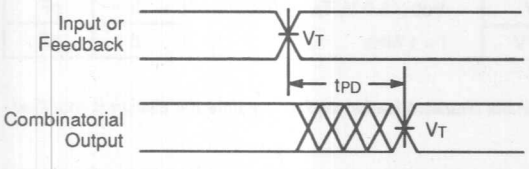
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				20		15	ns
t_S	Setup Time from Input or Feedback to Clock			15		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				15		20	ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	33.3		28.6		MHz
		Internal Feedback (f_{CNT})		35.7		30.3		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	41.7		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				20		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				20		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				20		55	ns

Notes:

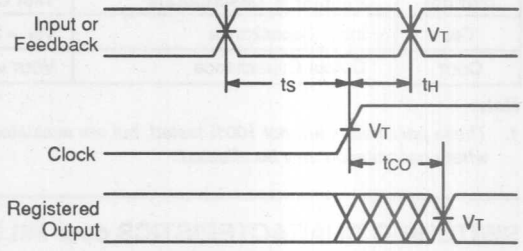
2. *See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

SWITCHING WAVEFORMS



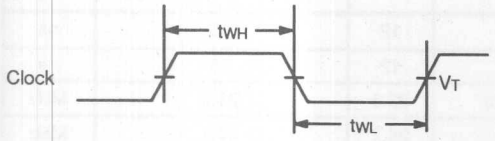
16493B-7

Combinatorial Output



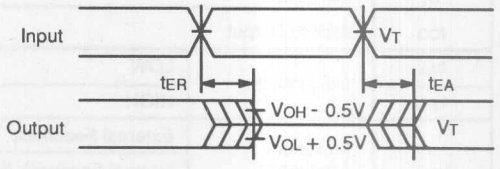
16493B-8

Registered Output



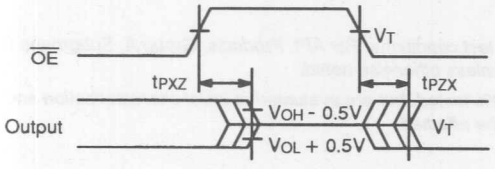
16493B-9

Clock Width



16493B-10

Input to Output Disable/Enable



16493B-11

$\overline{OE}$ to Output Disable/Enable

Notes:

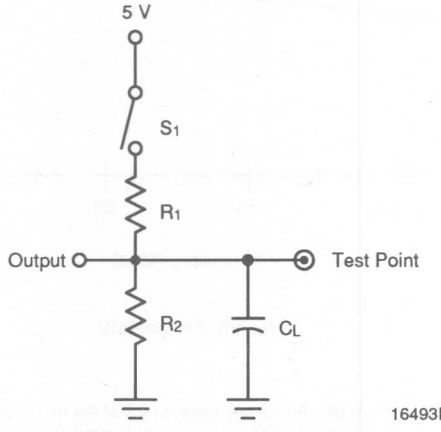
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

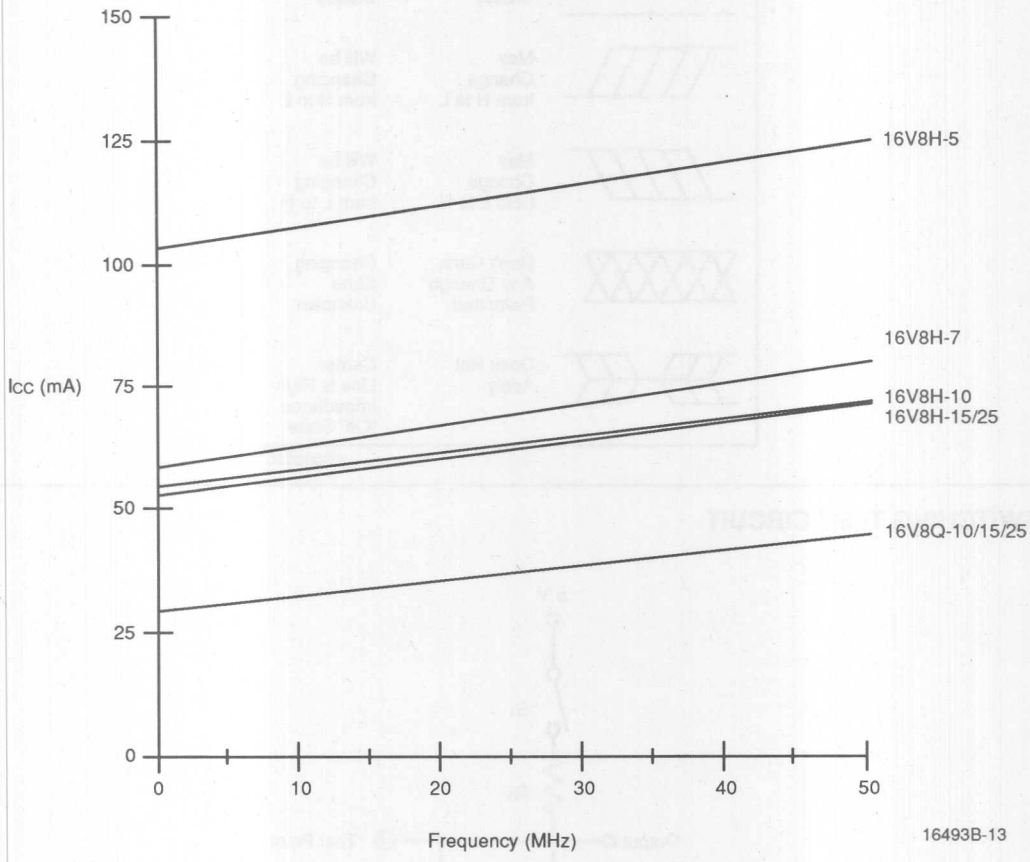


16493B-12

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF		H-5: 200 Ω			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

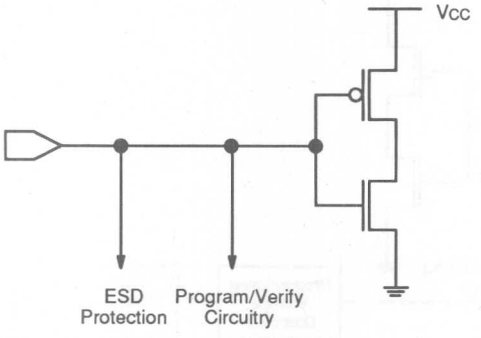
By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

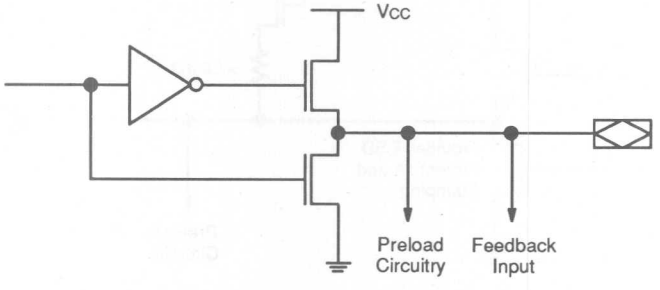
The PALCE16V8 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



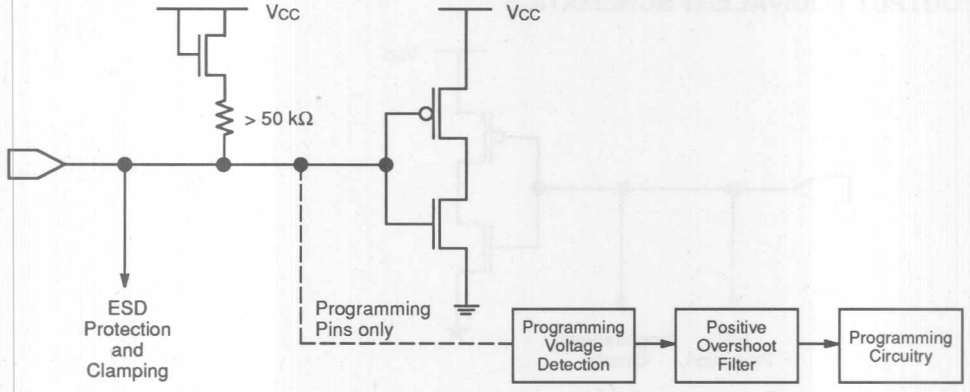
Typical Output

16493B-14

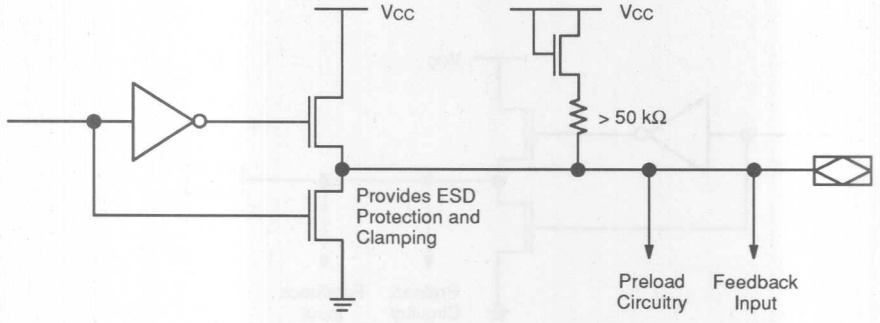
ROBUSTNESS FEATURES

PALCE16V8X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 versions. Selected /4 devices are also being retrofitted with these robustness features. See chart below for device listings.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSIONS AND SELECTED /4 VERSIONS*



Typical Input



Typical Output

16493B-15

*

Device	Rev Letter	
	Filter Only	Filter and Pullups
PALCE16V8H-10	E, F	I
PALCE16V8H-15	D, E, F, G	H, I
PALCE16V8Q-15	D, G	H
PALCE16V8H-25	D, G	H
PALCE16V8Q-25	D, G	H

Topside Marking:

AMD CMOS PLD's are marked on the top of the package in the following manner:

PALCEXXXX

Date Code (3 numbers) Lot ID (4 characters)– –(Rev. Letter)

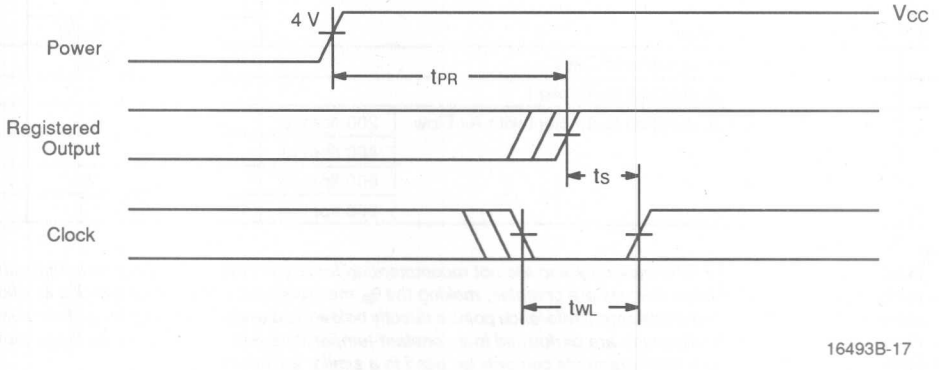
The Lot ID and Rev Letter are separated by two spaces.

POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

/4 Devices (PALCE16V8H-10/4)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PDIP	Typ. PLCC	Unit
θ_{jc}	Thermal Impedance, Junction to Case		25	22	°C/W
θ_{ja}	Thermal Impedance, Junction to Ambient		71	64	°C/W
θ_{jma}	Thermal Impedance, Junction to Ambient with Air Flow	200 lfpm air	61	55	°C/W
		400 lfpm air	55	51	°C/W
		600 lfpm air	51	47	°C/W
		800 lfpm air	47	45	°C/W

/5 Devices (PALCE16V8H-7/5)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PDIP	Typ. PLCC	Unit
θ_{jc}	Thermal Impedance, Junction to Case		29	23	°C/W
θ_{ja}	Thermal Impedance, Junction to Ambient		70	61	°C/W
θ_{jma}	Thermal Impedance, Junction to Ambient with Air Flow	200 lfpm air	64	53	°C/W
		400 lfpm air	58	47	°C/W
		600 lfpm air	53	44	°C/W
		800 lfpm air	X	X	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PRELIMINARY COM'L: -10

PALLV16V8-10

Low-Voltage 20-Pin EE CMOS Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
  - V_{CC} = +3.0 V to +3.6 V
- **Pin, function and fuse-map compatible with all 20-pin GAL devices**
- **Electrically-erasable CMOS technology provides reconfigurable logic and full testability**
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Designed to interface with both 3.3 V and 5 V logic**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALLV16V8 is an advanced PAL device built with low-voltage, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALLV16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALLV16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

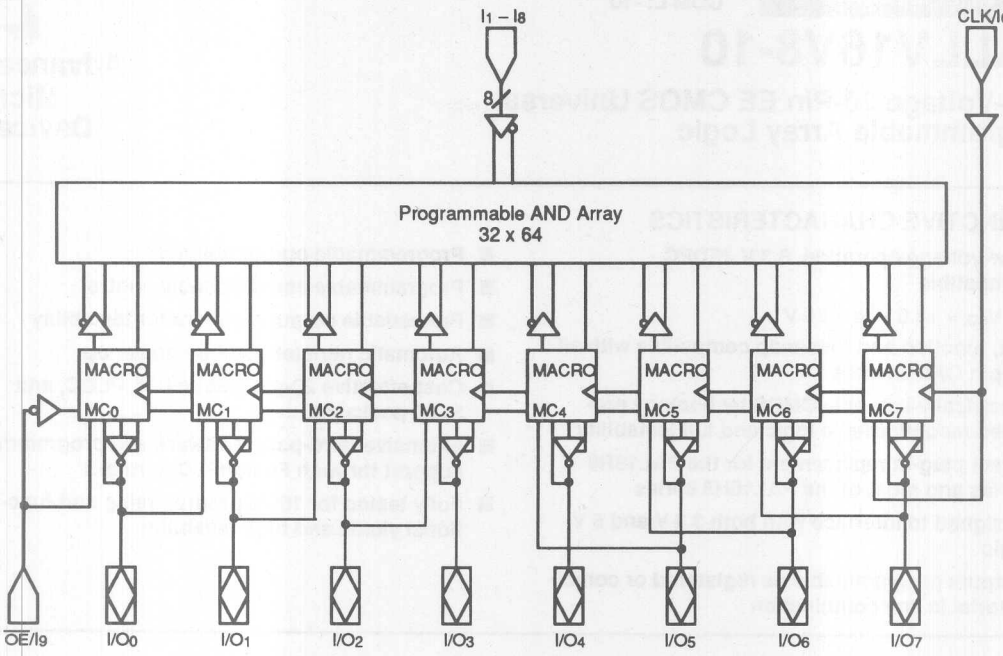
The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALLV16V8 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the Software Reference Guide to PLD Compilers for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 17713 Rev. A Amendment /0
Issue Date: June 1993

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

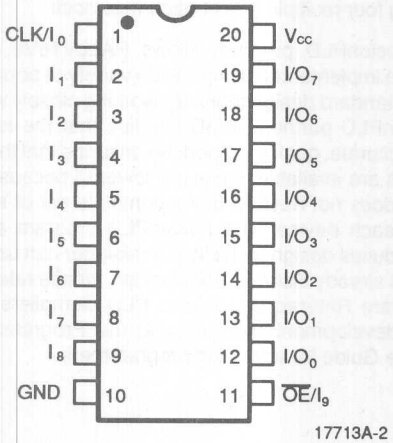
BLOCK DIAGRAM



17713A-1

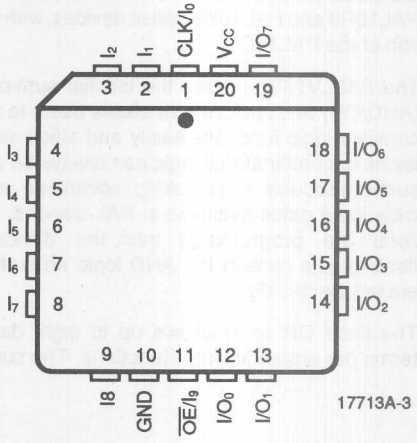
CONNECTION DIAGRAMS (Top View)

DIP/SOIC



17713A-2

PLCC



17713A-3

PIN DESIGNATIONS

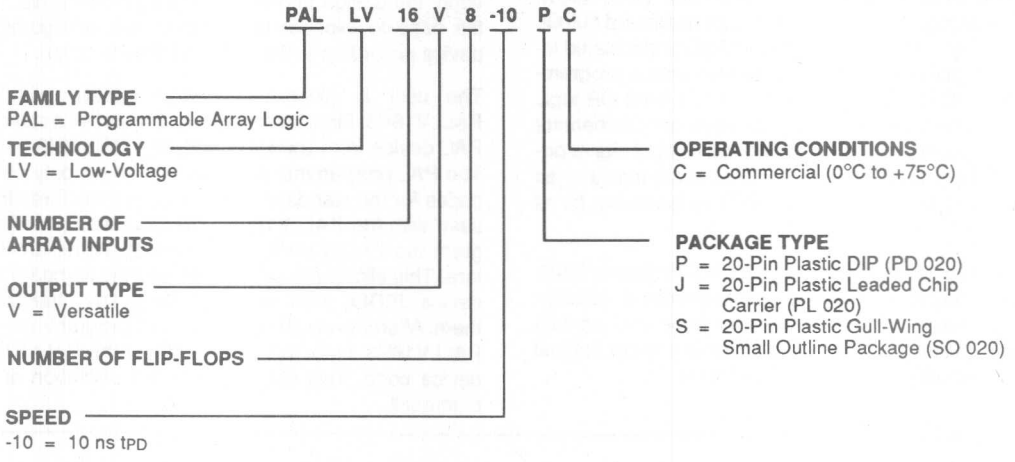
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
$\overline{OE}$ = Output Enable
VCC = Supply Voltage

Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION

Commerical Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALLV16V8-10	PC, JC, SC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

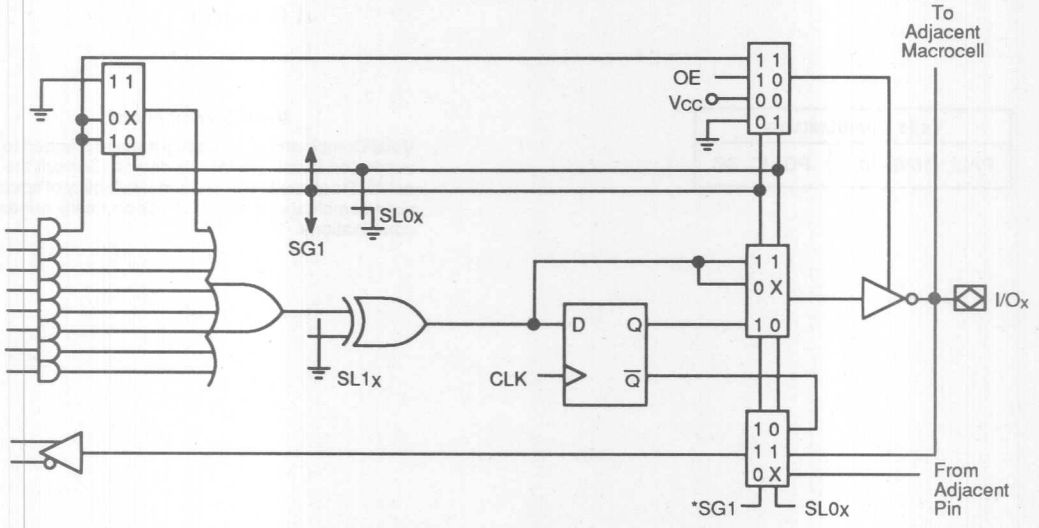
The PALLV16V8 is a low-voltage, EE CMOS version of the PALCE16V8.

The PALLV16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALLV16V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALLV16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALLV16V8. The programmer will program the PALLV16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALLV16V8. Here the user must use the PALLV16V8 device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

17713A-4

Figure 1. PALLV16V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALLV16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x = 0$. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALLV16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x = 0$. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x = 1$. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x = 1$. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x = 1$. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

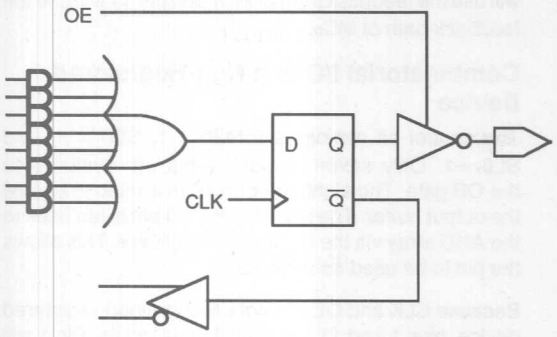
Table 1. Macrocell Configuration

SG0	SG1	SL0x	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

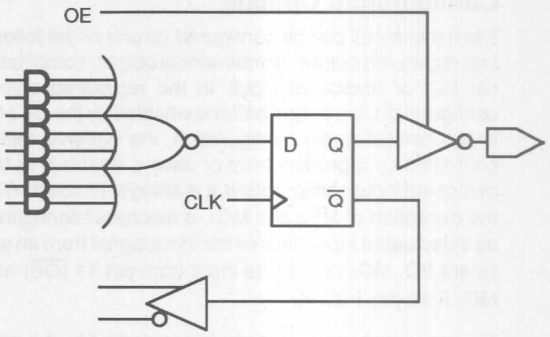
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

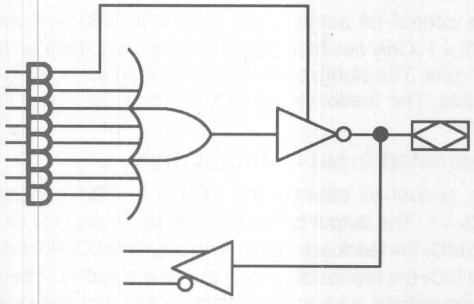
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



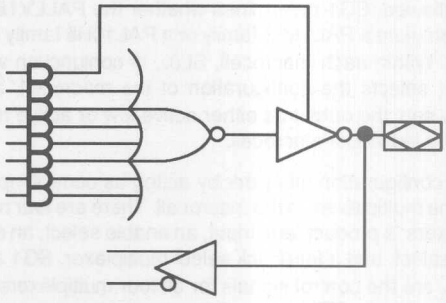
Registered Active Low



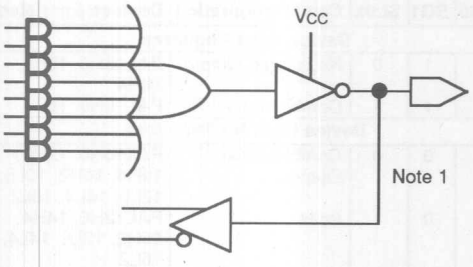
Registered Active High



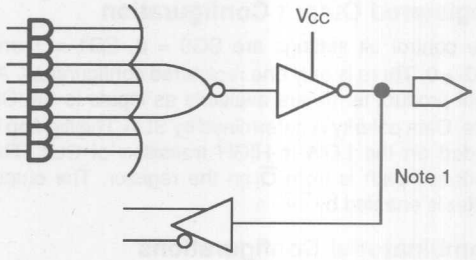
Combinatorial I/O Active Low



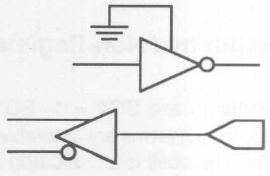
Combinatorial I/O Active High



Combinatorial Output Active Low



Combinatorial Output Active High



Dedicated Input

17713A-5

Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *The dedicated-input configuration is not available on pins 15 and 16.*

Figure 2. Macrocell Configurations

Benefits of Lower Operating Voltage

The PALLV16V8 has an operating voltage range of 3.0 V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. Lower operating voltage also reduces electromagnetic radiation noise and makes obtaining FCC approval easier.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALLV16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALLV16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALLV16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALLV16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALLV16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

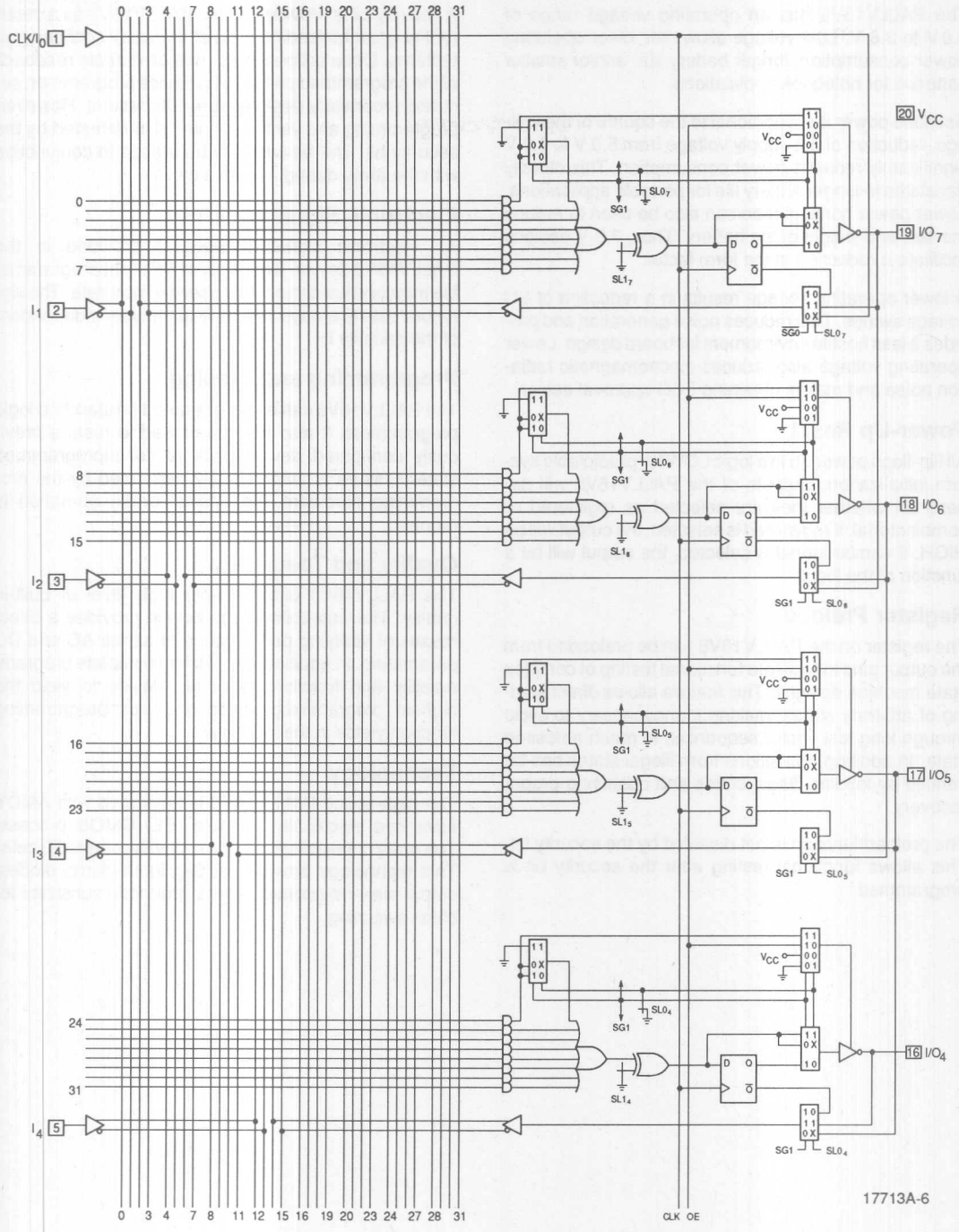
Quality and Testability

The PALLV16V8 offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

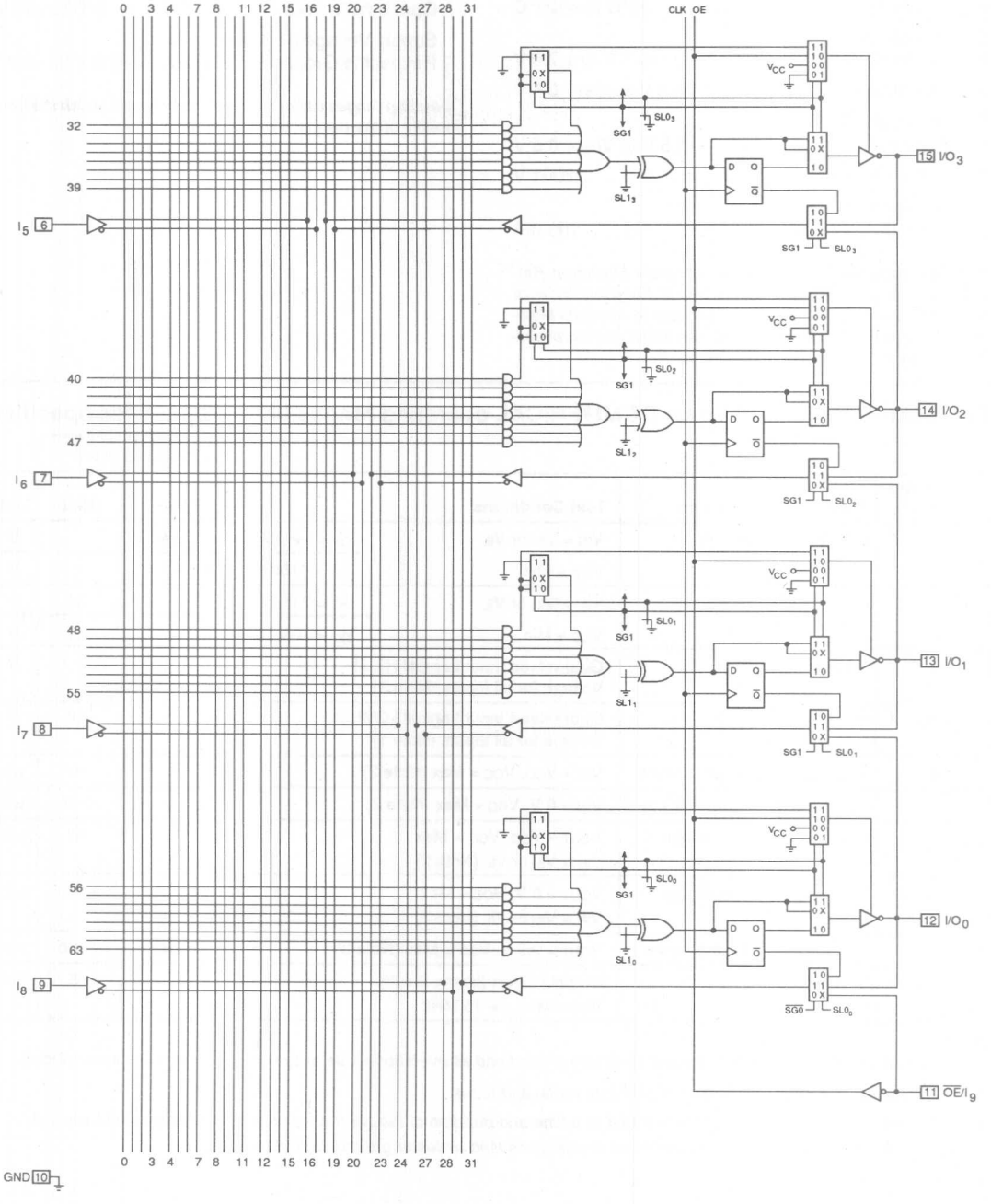
Technology

The high-speed PALLV16V8 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



17713A-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to 85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERICAL operating ranges unless otherwise specified

				PRELIMINARY		
Parameter Symbol	**Parameter Description**	**Test Conditions**		**Min**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –2 mA	2.4		V
		V_{CC} = Min	I_{OH} = –100 µA	V_{CC} – 0.2 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 2 mA		0.4	V
		V_{CC} = Min	I_{OL} = 100 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz			55	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

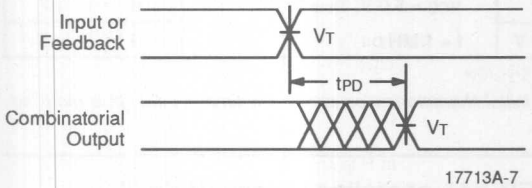
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			PRELIMINARY Min	PRELIMINARY Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})		71.4		MHz
		No Feedback	$1/(t_S+t_H)$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				10	ns

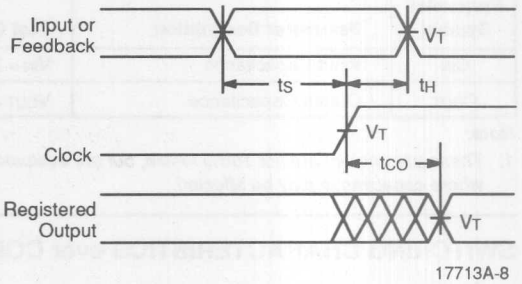
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

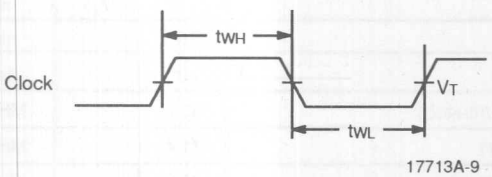
SWITCHING WAVEFORMS



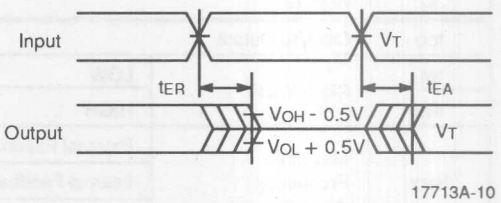
Combinatorial Output



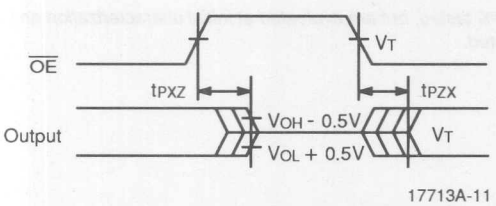
Registered Output



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

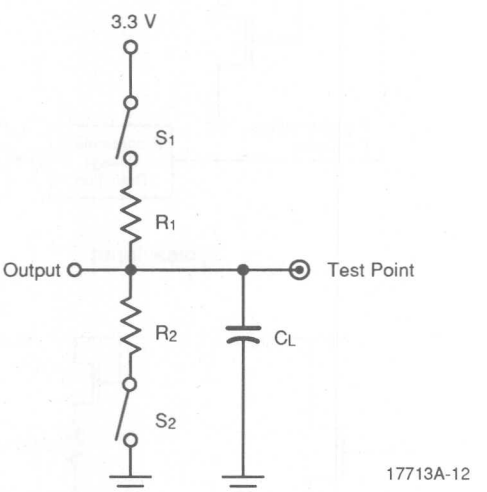
1. *V_T = 1.5 V for Input Signals and 1.65 V for Output Signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns –5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



17713A-12

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	1.6K	1.6K	1.65 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				1.65 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

ENDURANCE CHARACTERISTICS

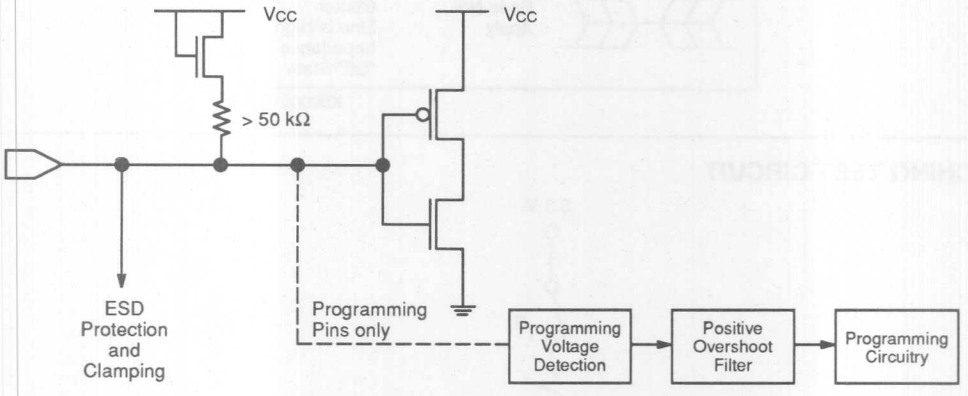
The PALLV16V8 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

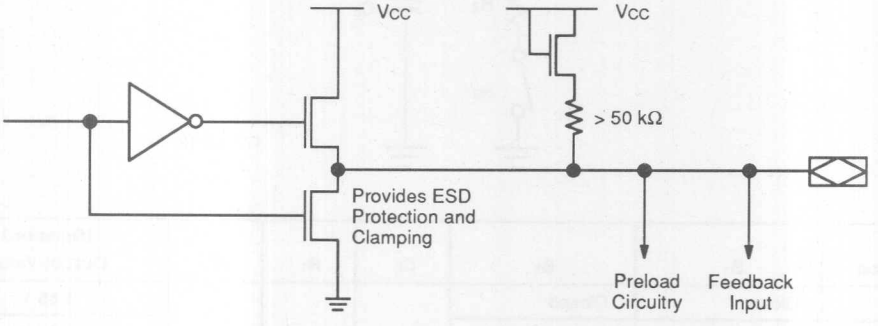
ROBUSTNESS FEATURES

The PALLV16V8 has some unique features that make it extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

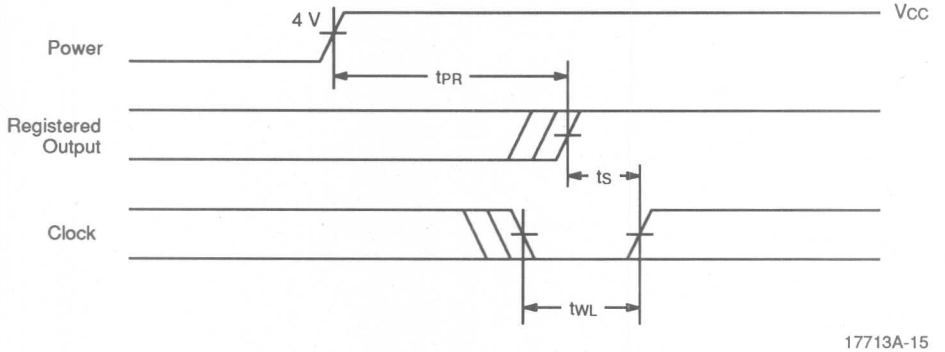
17713A-14

POWER-UP RESET

The PALLV16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



17713A-15



ZPAL™ Devices

FINAL | COM'L: -15/25 IND: -15/25

PALCE16V8Z FAMILY

Zero-Power 20-Pin EE CMOS Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero-Power CMOS technology**
  - — 15 µA Standby Current
  - — 15 ns propagation delay for "-15" version
  - — 25 ns propagation delay for "-25" version
- **Unused product term disable for reduced power consumption**
- **Available in Industrial operating range**
  - — T_C = –40°C to +85°C
  - — V_{CC} = +4.5 V to +5.5 V
- **HC- and HCT-Compatible inputs and outputs**
- **Pin, function and fuse-map compatible with all 20-pin GAL devices**
- **Electrically-erasable CMOS technology provides reconfigurable logic and full testability**
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP and PLCC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALCE16V8Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8Z will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALCE16V8Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALCE16V8Z allows battery powered operation for an extended period.

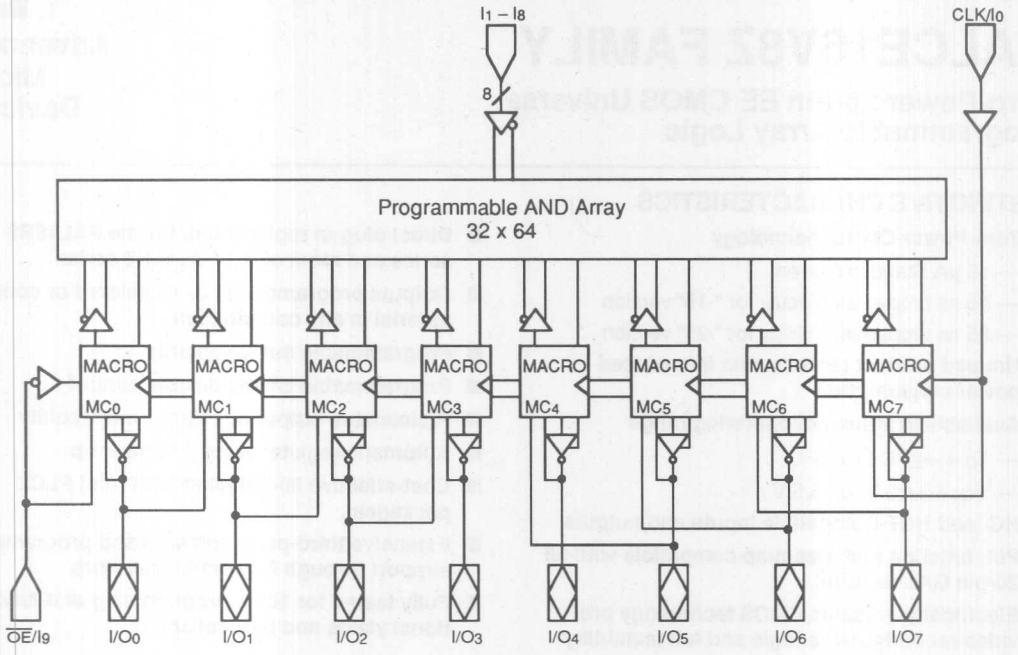
The PALCE16V8Z utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active- high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 13061 Rev. C Amendment /0
Issue Date: June 1993

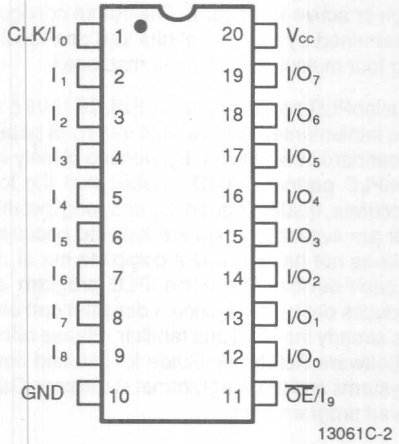
BLOCK DIAGRAM



13061C-1

CONNECTION DIAGRAMS
Top View

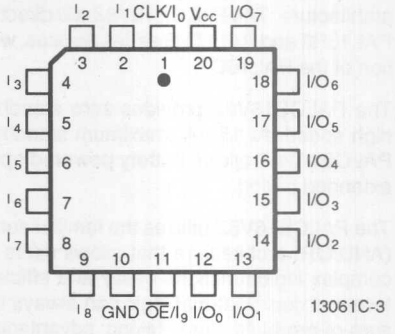
DIP



13061C-2

Note:
Pin 1 is marked for orientation

PLCC



13061C-3

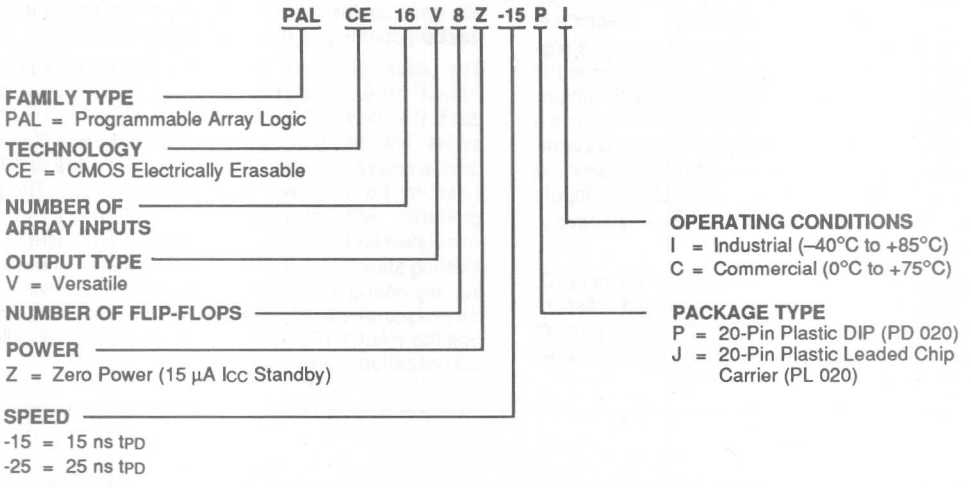
PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE16V8Z-15	PI, JI, PC, JC
PALCE16V8Z-25	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

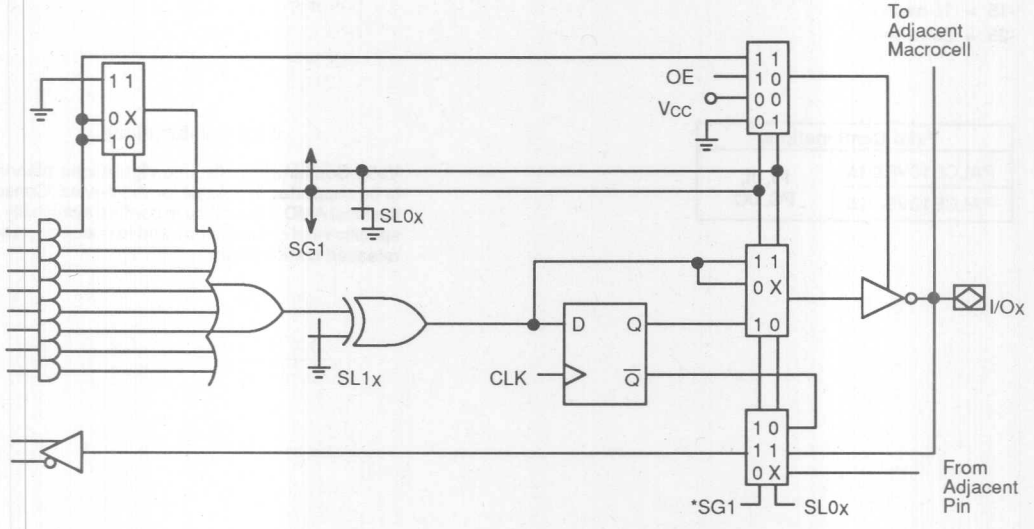
The PALCE16V8Z is the zero-power version of the PALCE16V8. It has all the architectural features of the PALCE16V8. In addition, the PALCE16V8Z has zero standby power and unused product term disable.

The PALCE16V8Z is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8Z are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8Z. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8Z. The programmer will program the PALCE16V8Z in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8Z. Here the user must use the PALCE16V8Z device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

13061C-4

Figure 1. PALCE16V8Z Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8Z will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8Z has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

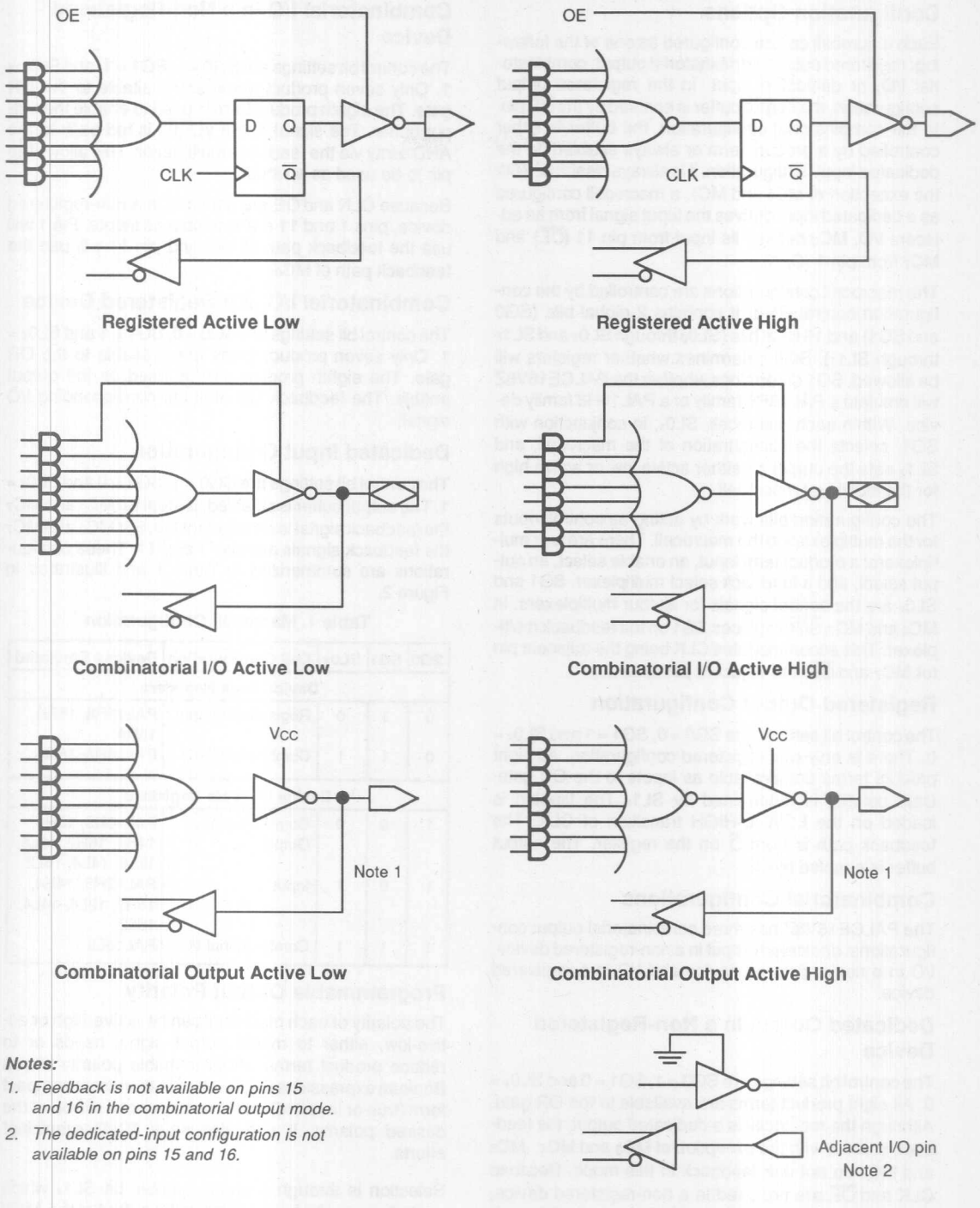
Table 1. Macrocell Configuration

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *The dedicated-input configuration is not available on pins 15 and 16.*

Figure 2. Macrocell Configurations

Zero-Standby Power Mode

The PALCE16V8Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE16V8Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 15\ \mu A$). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the I_{CC} vs. frequency graph.

Product-Term Disable

On a programmed PALCE16V8Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs frequency graph, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note, "Minimizing Power Consumption with Zero-Power PLDs".

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8Z will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALCE16V8Z as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8Z device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

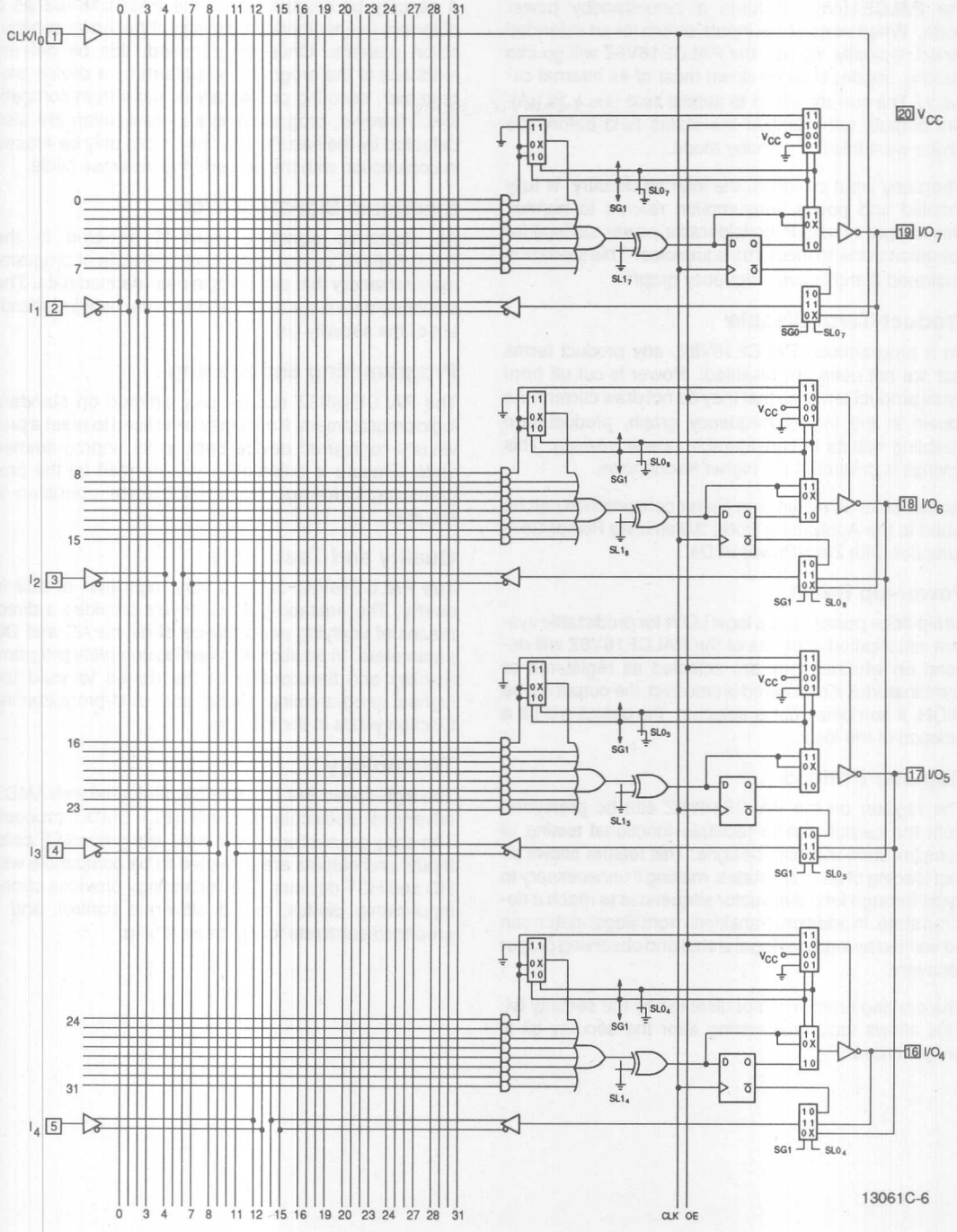
Quality and Testability

The PALCE16V8Z offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

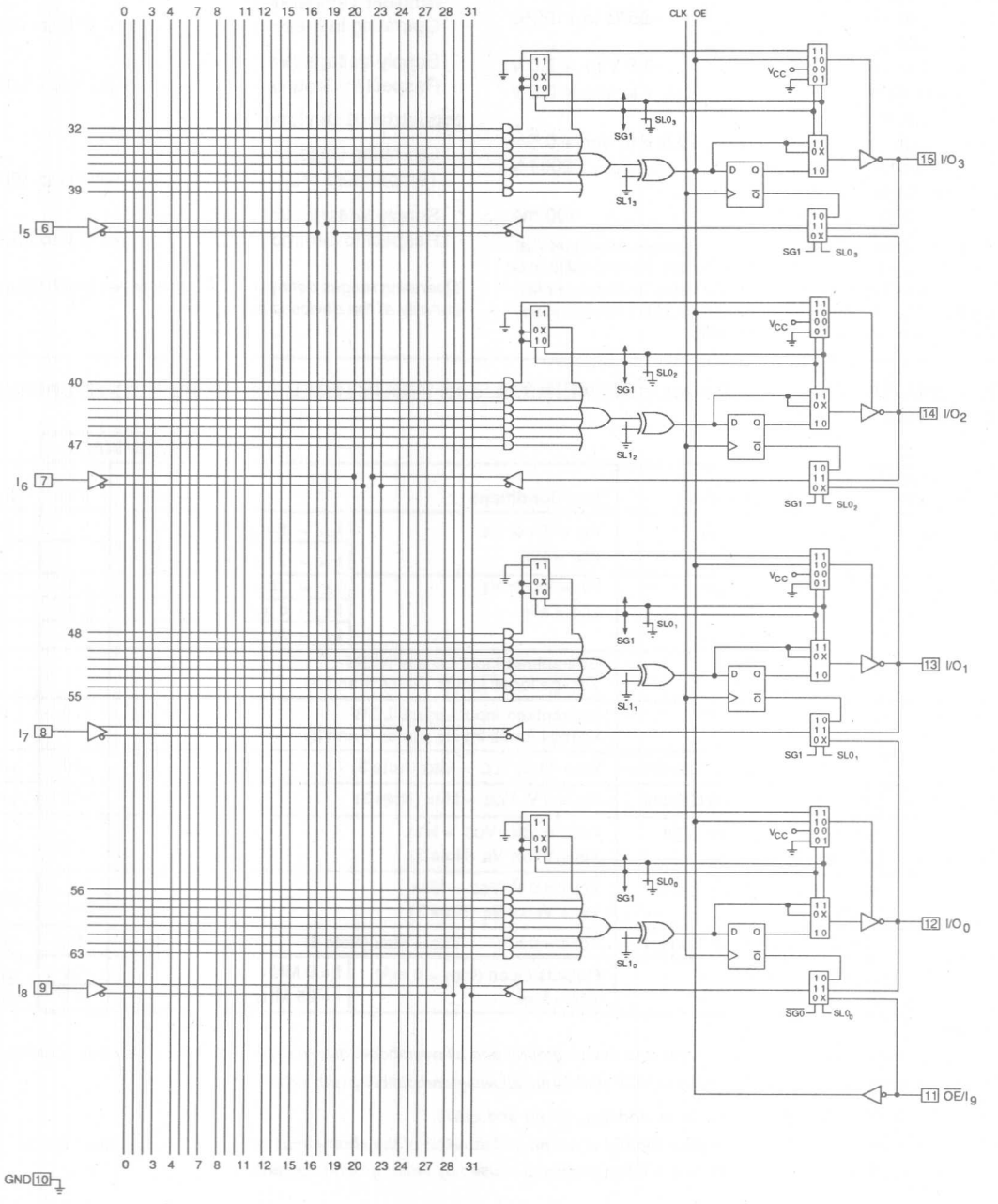
Technology

The high-speed PALCE16V8Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



13061C-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature
with Power Applied ..... –55°C to +125°C
Supply Voltage with
Respect to Ground ..... –0.5 V to + 7.0 V
DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V
DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case
Temperature (T_C) ..... –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

				PRELIMINARY		
Parameter Symbol	**Parameter Description**	**Test Conditions**		**Min**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	f = 0 MHz		15	µA
			f = 25 MHz		75	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

				PRELIMINARY		
Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input or Feedback to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		58.8		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15	ns
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature
with Power Applied ..... –55°C to +125°C
Supply Voltage with
Respect to Ground ..... –0.5 V to + 7.0 V
DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V
DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case
Temperature (T_C) ..... –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	f = 0 MHz		15	µA
			f = 25 MHz		90	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

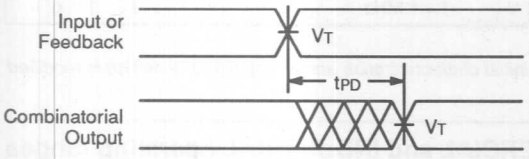
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input or Feedback to Clock			20		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})		50		MHz
		No Feedback	$1/(t_S+t_H)$	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

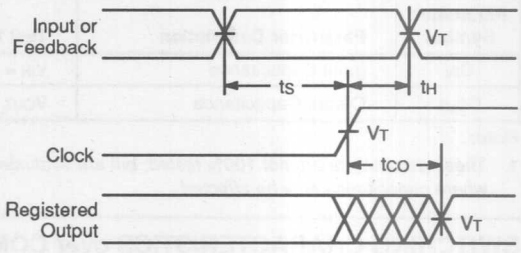
2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 2 ns faster.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING WAVEFORMS



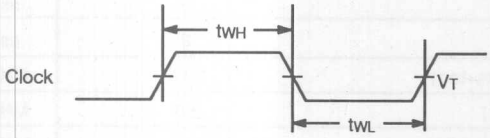
13061C-7

Combinatorial Output



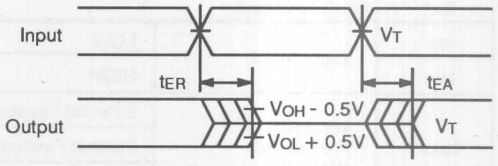
13061C-8

Registered Output



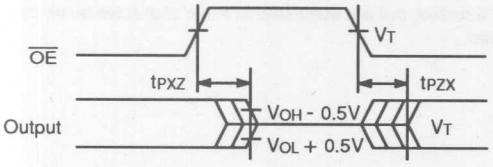
13061C-9

Clock Width



13061C-10

Input to Output Disable/Enable



13061C-11

$\overline{OE}$ to Output Disable/Enable

Notes:

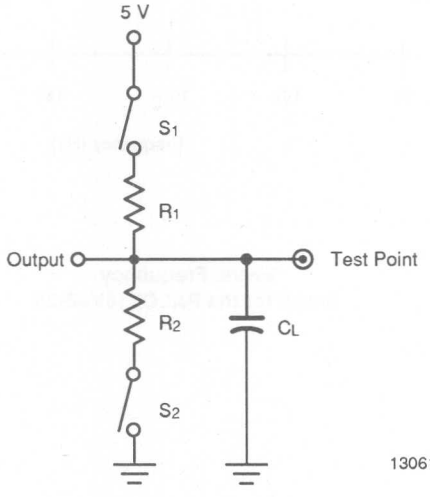
1. *V_T = 1.5 V for Input Signals and 2.5 V for Output Signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

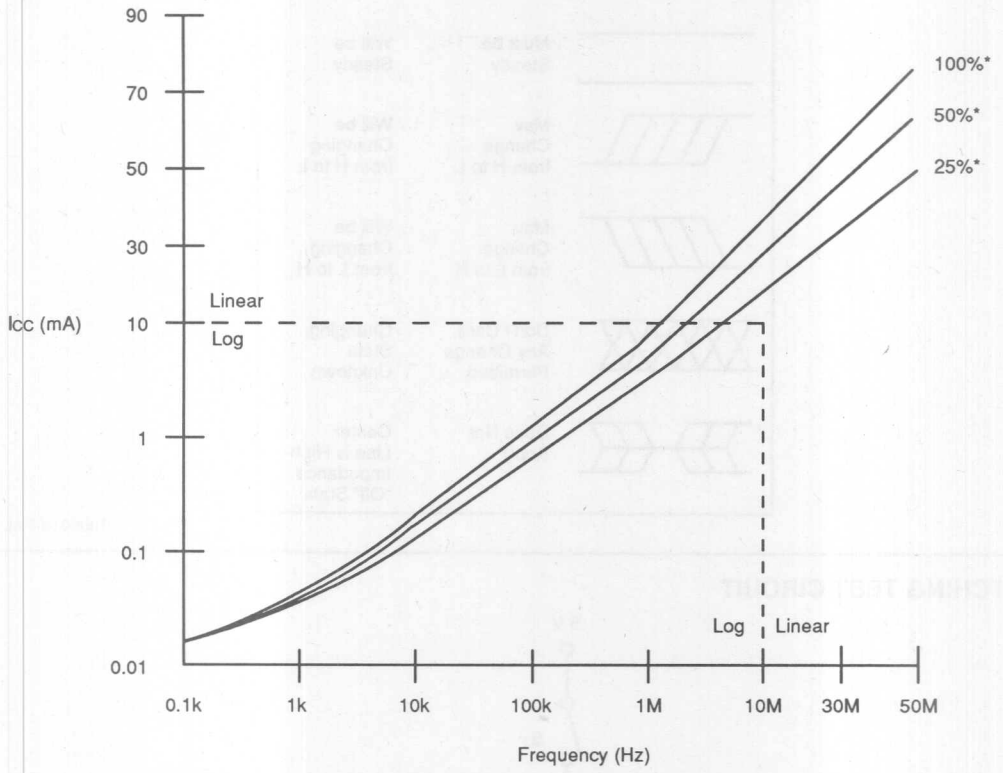


13061C-12

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	820 Ω	820 Ω	2.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				2.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE16V8Z-25

V_{CC} = 5.0 V, T_A = 25°C



*Percent of product terms used.

13061C-13

I_{CC} vs. Frequency Graph for the PALCE16V8Z-25

ENDURANCE CHARACTERISTICS

The PALCE16V8Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

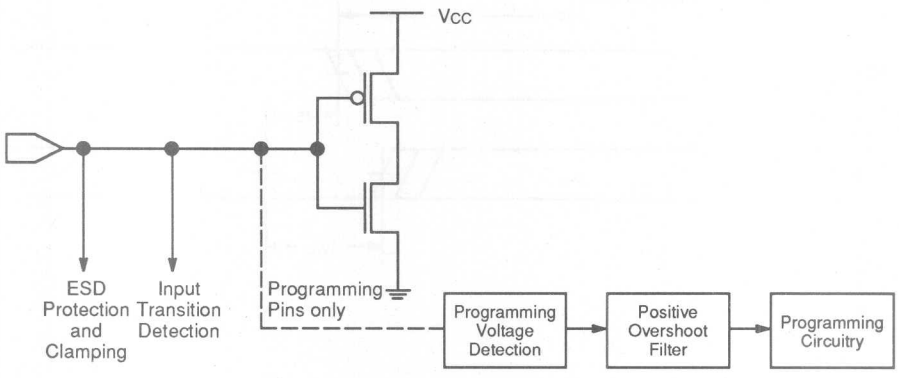
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

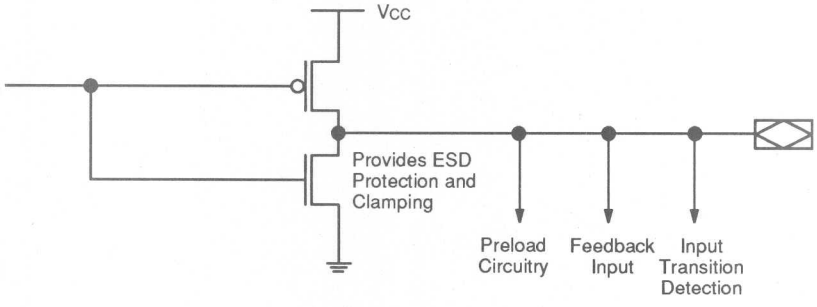
ROBUSTNESS FEATURES

The PALCE16V8Z has some unique features that make it extremely robust, especially when operating in high-speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

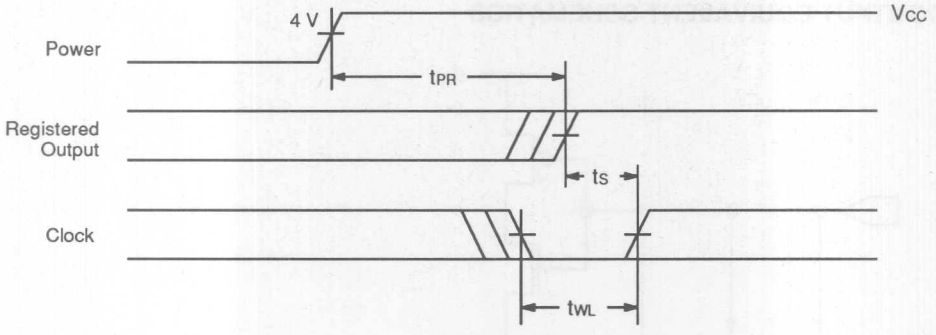
13061C-14

POWER-UP RESET

The PALCE16V8Z has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



13061C-15

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

PALCE16V8Z-25

Parameter Symbol	Parameter Description		Typ. PDIP	Typ. PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		20	19	°C/W
θ_{ja}	Thermal impedance, junction to ambient		65	57	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	58	41	°C/W
		400 lfpm air	51	37	°C/W
		600 lfpm air	47	35	°C/W
		800 lfpm air	44	33	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



ZPAL™ Devices

PALLV16V8Z Family

Low-Voltage, Zero-Power, 20-Pin EE CMOS Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
  - — V_{CC} = +3.0 V to +3.6 V
- **Zero-power CMOS technology**
  - — 15 µA standby current
  - — 25 ns propagation delay for "-25" version
  - — 30 ns propagation delay for "-30" version
- **Industrial operating temperature range**
  - — T_C = –40°C to +85°C
- **Unused product term disable for reduced power consumption**
- **Pin, function and fuse-map compatible with all 20-pin GAL devices**
- **Electrically-erasable CMOS technology provides reconfigurable logic and full testability**
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALLV16V8Z is an advanced PAL device built with low-voltage, zero-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALLV16V8Z will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALLV16V8Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALLV16V8Z allows battery powered operation for an extended period.

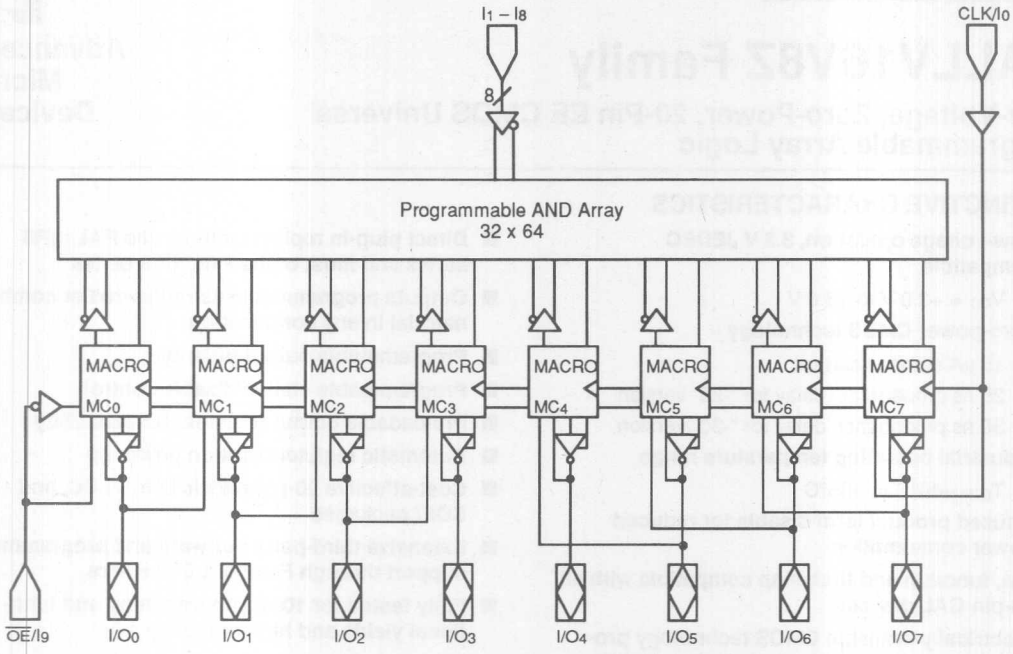
The PALLV16V8Z utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALLV16V8Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the Software Reference Guide to PLD Compilers for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 17422 Rev. B Amendment/0
Issue Date: June 1993

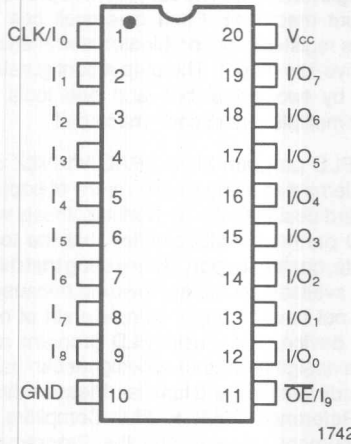
BLOCK DIAGRAM



17422B-1

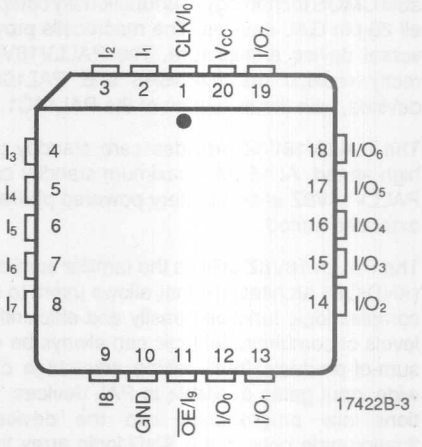
CONNECTION DIAGRAMS (Top View)

DIP/SOIC



17422B-2

PLCC



17422B-3

PIN DESIGNATIONS

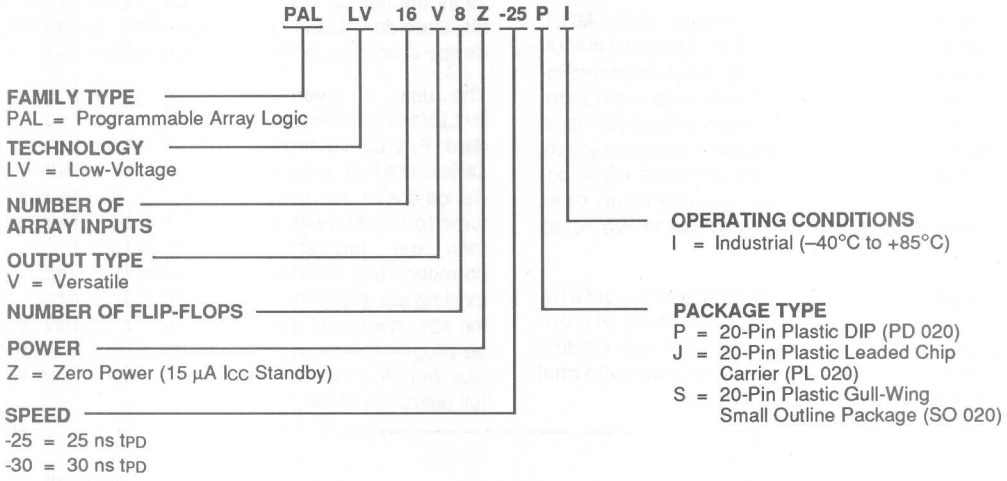
CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALLV16V8Z-25	PI, JI, SI
PALLV16V8Z-30	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

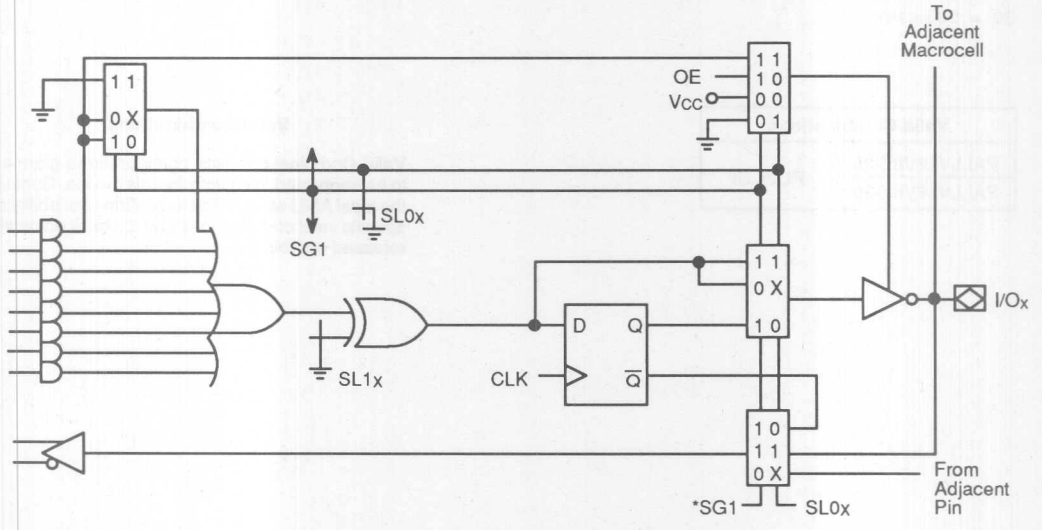
The PALLV16V8Z is a low-voltage, EE CMOS version of the PALCE16V8. In addition, the PALLV16V8Z has zero standby power and unused product term disable.

The PALLV16V8Z is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALLV16V8Z are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALLV16V8Z. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALLV16V8Z. The programmer will program the PALLV16V8Z in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALLV16V8Z. Here the user must use the PALLV16V8Z device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

17422B-4

Figure 1. PALLV16V8Z Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALLV16V8Z will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x = 0$. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALLV16V8Z has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x = 0$. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x = 1$. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x = 1$. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x = 1$. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

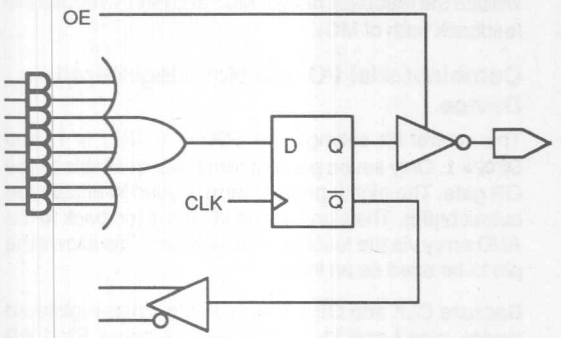
Table 1. Macrocell Configuration

SG0	SG1	SL0x	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

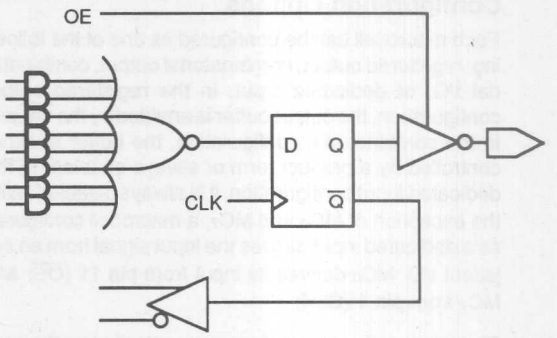
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

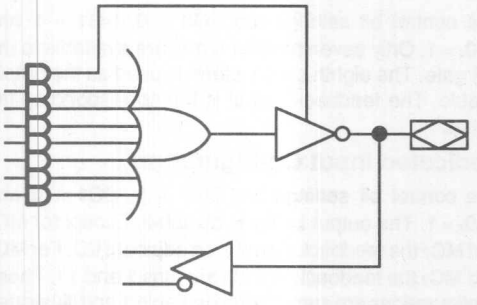
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



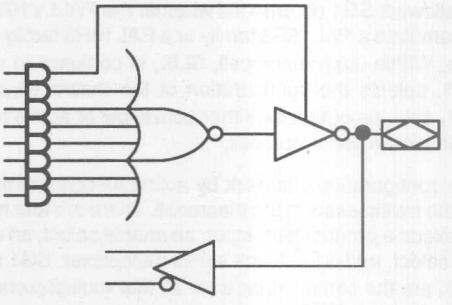
Registered Active Low



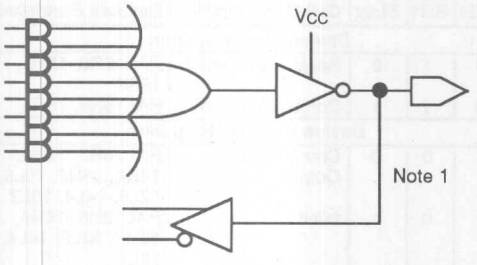
Registered Active High



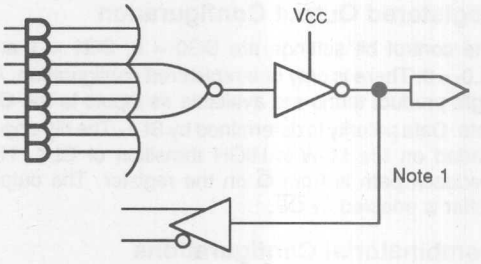
Combinatorial I/O Active Low



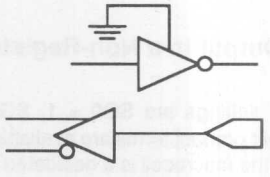
Combinatorial I/O Active High



Combinatorial Output Active Low



Combinatorial Output Active High



Dedicated Input

17422B-5

Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *The dedicated-input configuration is not available on pins 15 and 16.*

Figure 2. Macrocell Configurations

Benefits of Lower Operating Voltage

The PALLV16V8Z has an operating voltage range of 3.0 V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. Lower operating voltage also reduces electromagnetic radiation noise and makes obtaining FCC approval easier.

Zero-Standby Power Mode

The PALLV16V8Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALLV16V8Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 15\ \mu A$). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the I_{CC} vs. frequency graph.

Product-Term Disable

On a programmed PALLV16V8Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs frequency graph, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note "Minimizing Power Consumption with Zero-Power PLDs."

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALLV16V8Z will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALLV16V8Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALLV16V8Z as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALLV16V8Z device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALLV16V8Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

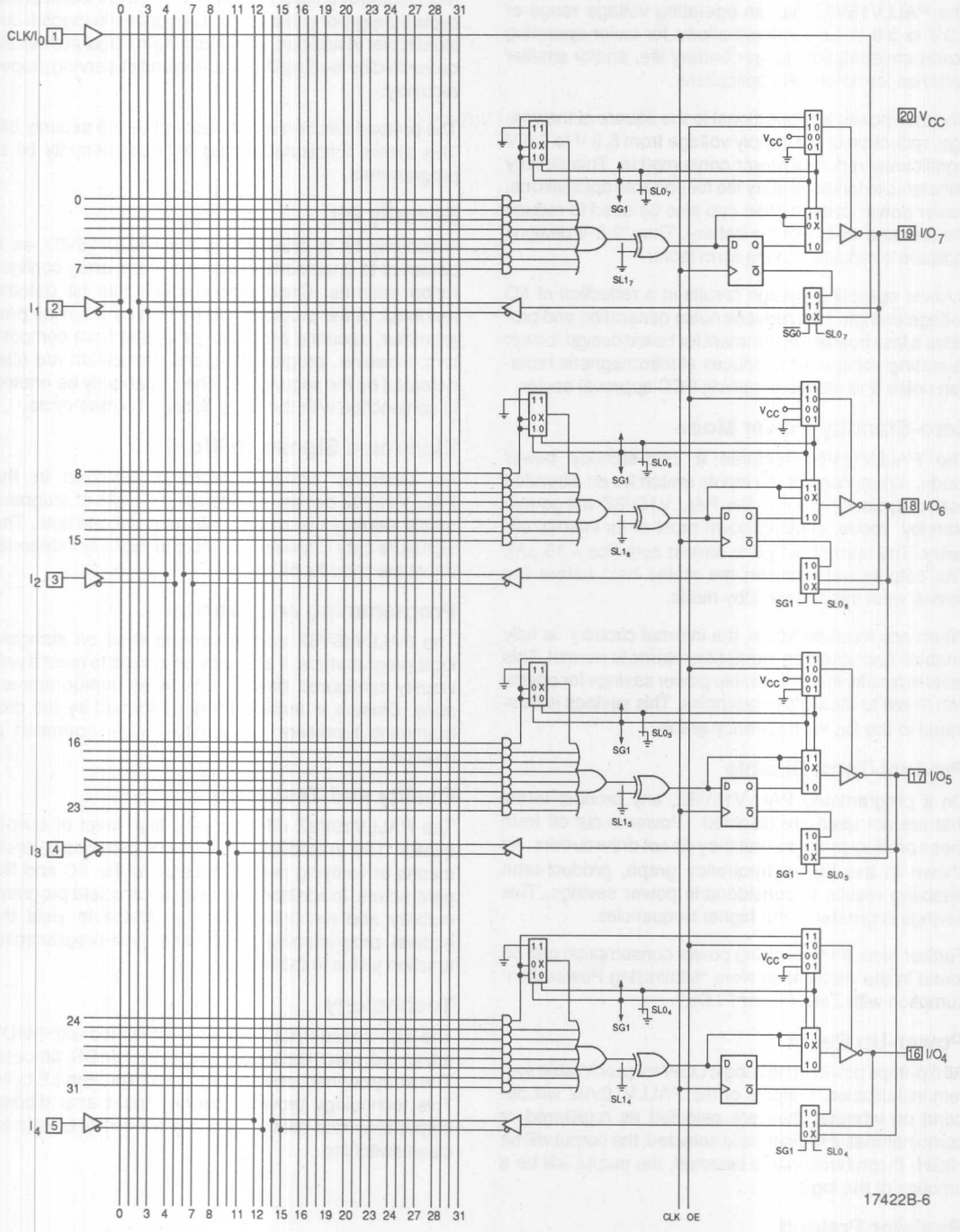
Quality and Testability

The PALLV16V8Z offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

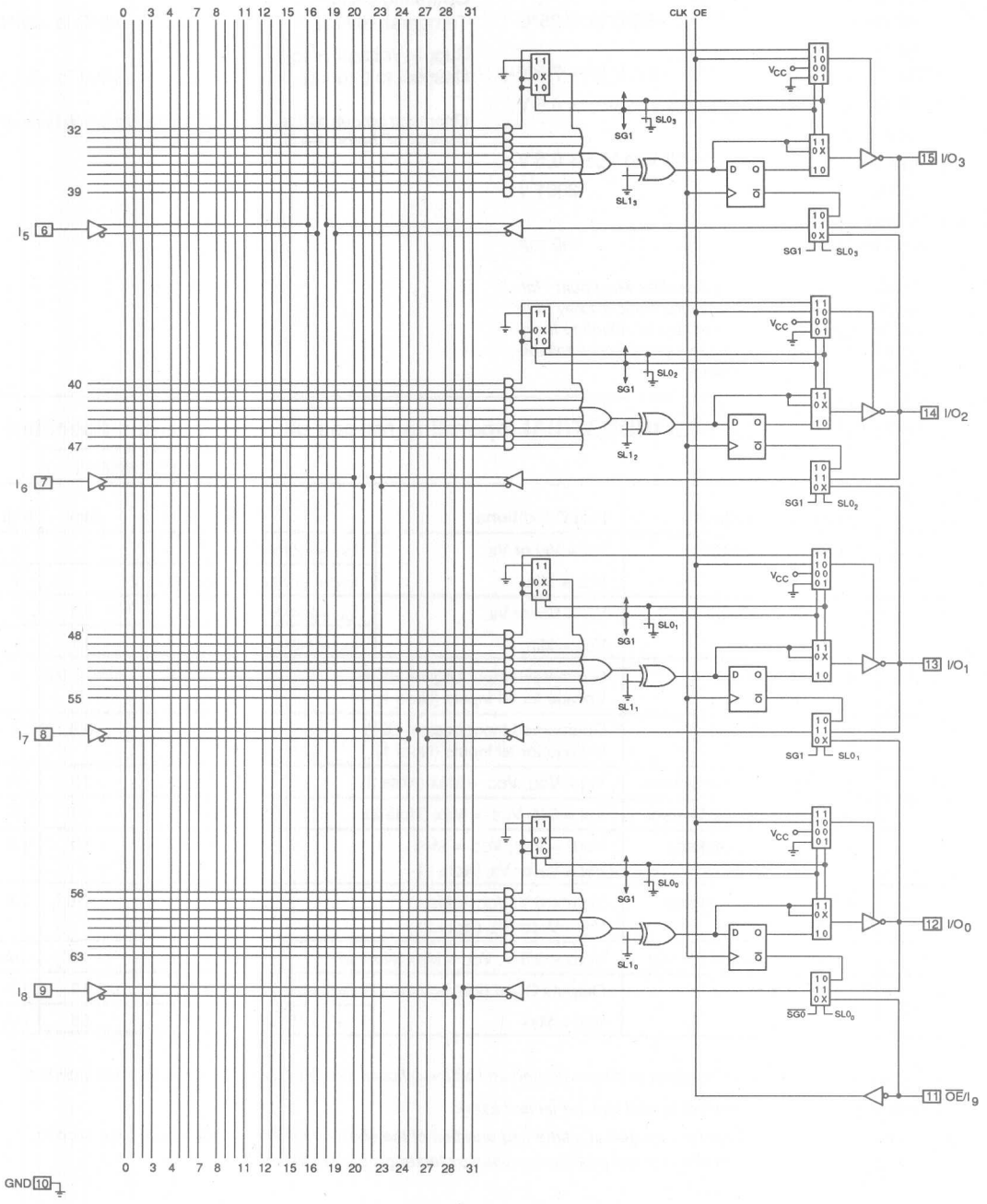
Technology

The high-speed PALLV16V8Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



17422B-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to 85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case Temperature (T_C) . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

				PRELIMINARY		
Parameter Symbol	**Parameter Description**	**Test Conditions**		**Min**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –2 mA	2.4		V
		V_{CC} = Min	I_{OH} = –100 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 2 mA		0.4	V
		V_{CC} = Min	I_{OL} = 100 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		15	µA
		V_{CC} = Max	f = 25 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

				PRELIMINARY		
Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input or Feedback to Clock			20		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})		50		MHz
		No Feedback	$1/(t_S+t_H)$	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be about 2 ns faster.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_A = –40°C to 85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case
Temperature (T_C) . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
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		V_{CC} = Min	I_{OH} = –100 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 2 mA		0.4	V
		V_{CC} = Min	I_{OL} = 100 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		15	µA
		V_{CC} = Max	f = 25 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

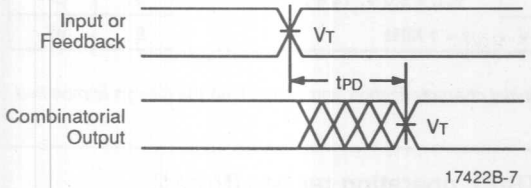
SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				30	ns
t_S	Setup Time from Input or Feedback to Clock			30		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{WL}	Clock Width	LOW		13		ns
t_{WH}		HIGH		13		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S+t_{CO})$	22		MHz
		Internal Feedback (f_{CNT})		38.4		MHz
		No Feedback	$1/(t_S+t_H)$	38.4		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				30	ns
t_{ER}	Input to Output Disable Using Product Term Control				30	ns

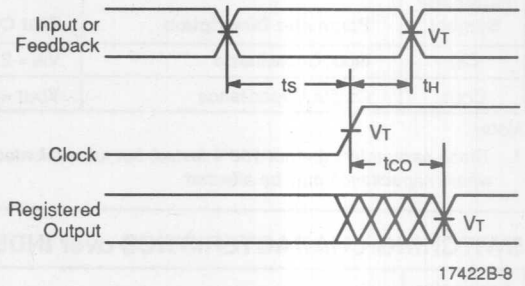
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be about 2 ns faster.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

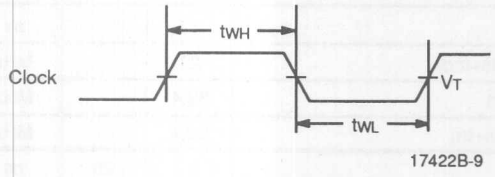
SWITCHING WAVEFORMS



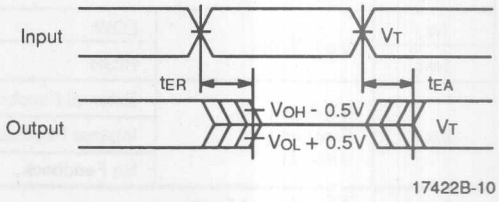
Combinatorial Output



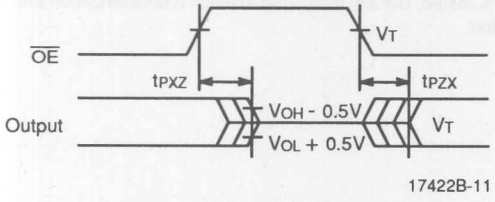
Registered Output



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

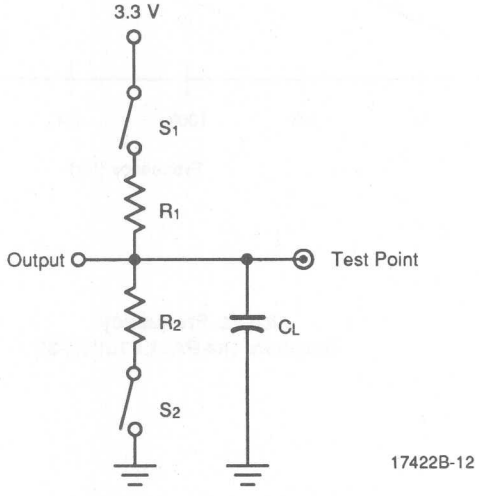
1. *V_T = 1.5 V for Input Signals and 1.65 V for Output Signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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SWITCHING TEST CIRCUIT

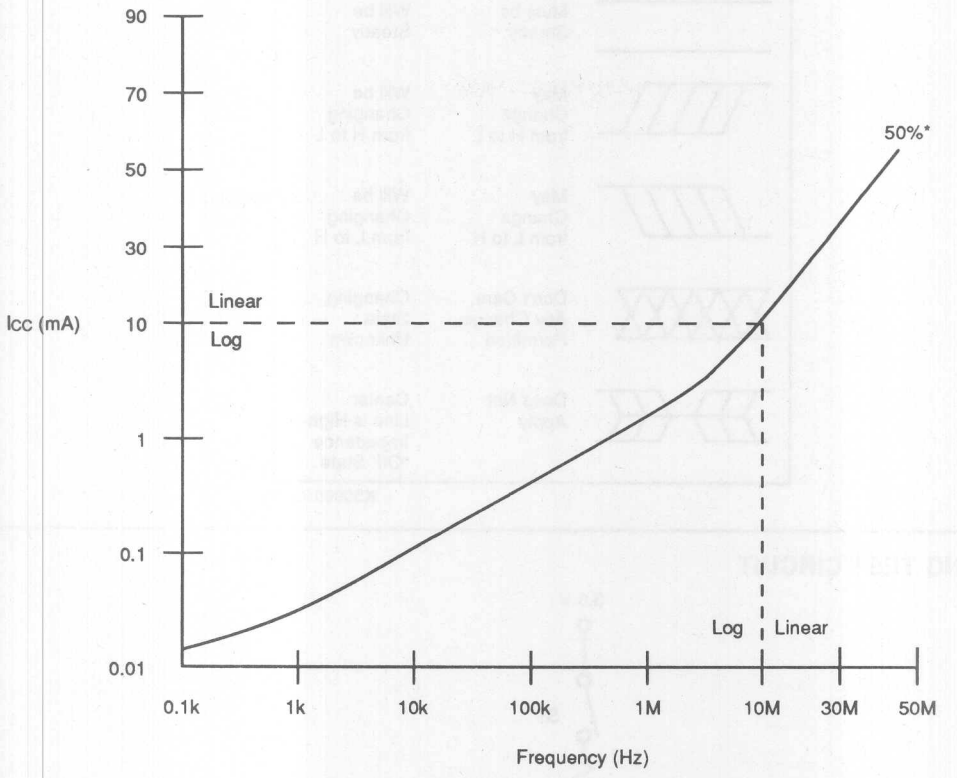


17422B-12

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	1.6K	1.6K	1.65 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				1.65 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALLV16V8Z-30

V_{CC} = 3.3 V, T_A = 25°C



*Percent of product terms used.

17422A-13

I_{CC} vs. Frequency Graph for the PALLV16V8Z-30

ENDURANCE CHARACTERISTICS

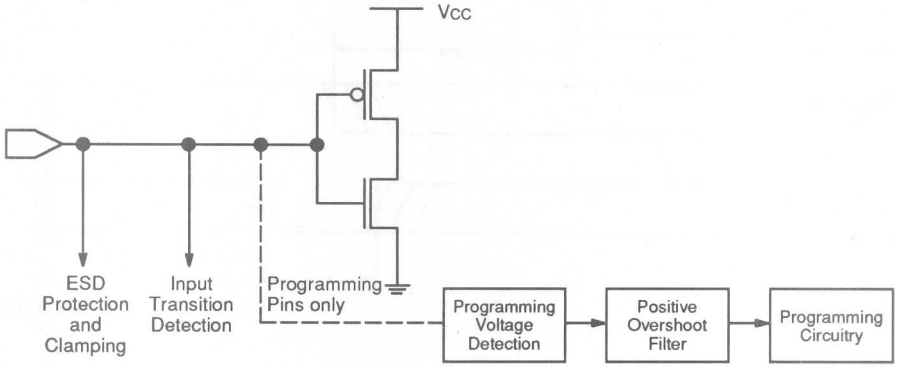
The PALLV16V8Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

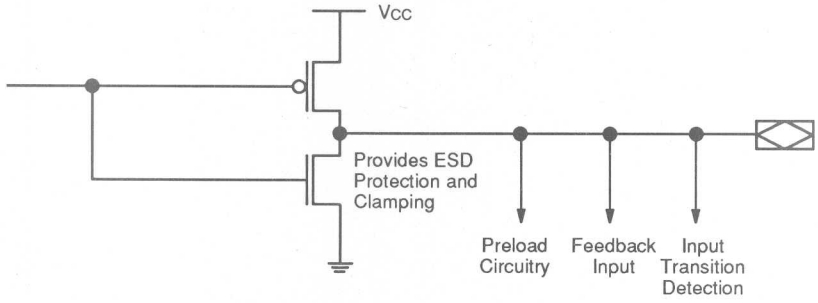
ROBUSTNESS FEATURES

The PALLV16V8Z has some unique features that make it extremely robust, especially when operating in high-speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

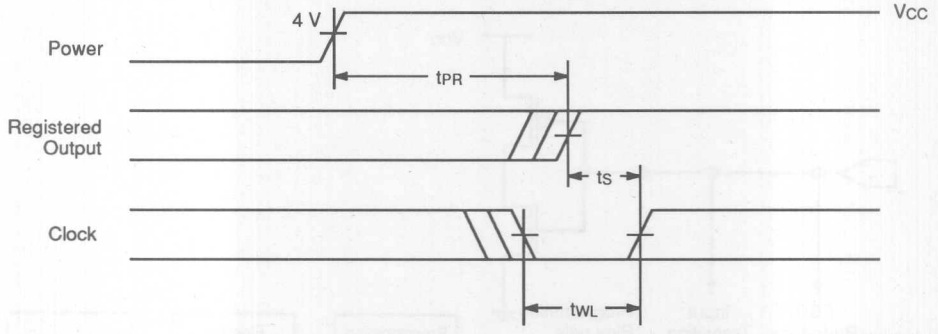
17422B-14

POWER-UP RESET

The PALLV16V8Z has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



17422B-15

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

PALLV16V8Z-30

Parameter Symbol	Parameter Description		Typ. PDIP	Typ. PLCC	Unit
θ_{jc}	Thermal Impedance, Junction to Case		20	19	°C/W
θ_{ja}	Thermal Impedance, Junction to Ambient		65	57	°C/W
θ_{jma}	Thermal Impedance, Junction to Ambient with Air Flow	200 lfpm air	58	41	°C/W
		400 lfpm air	51	37	°C/W
		600 lfpm air	47	35	°C/W
		800 lfpm air	44	33	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.


IMPORTANT
NOTES

FINAL COM'L: -15

PALCE16V8HD-15

EE CMOS 24-Pin High-Drive Universal PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High output-current drive capability (64 mA I_{OL})
- Programmable Totem-Pole or Open-Drain Outputs
- 200 mV Hysteresis
- Programmable Direct or Latched Inputs
- Outputs configurable as D or T flip-flops
- Outputs programmable as registered or combinatorial in any combination
- Automatic register reset on power-up
- Preloadable output registers for testability
- Programmable enable/disable control
- Electrically Erasable CMOS technology provides reconfigurable logic and full testability
- Cost-effective 24-pin plastic SKINNYDIP® and 28-pin PLCC packages
- Extensive third-party software and programmer support through FusionPLD partners
- Fully tested for 100% programming and functional yields and high reliability

GENERAL DESCRIPTION

The PALCE16V8HD is the first CMOS PAL device to combine high-current drive capability with a PAL architecture. The PALCE16V8HD can sink up to 64 mA for bus applications. It also has an advanced PAL architecture using a programmable macrocell to help provide a universal solution.

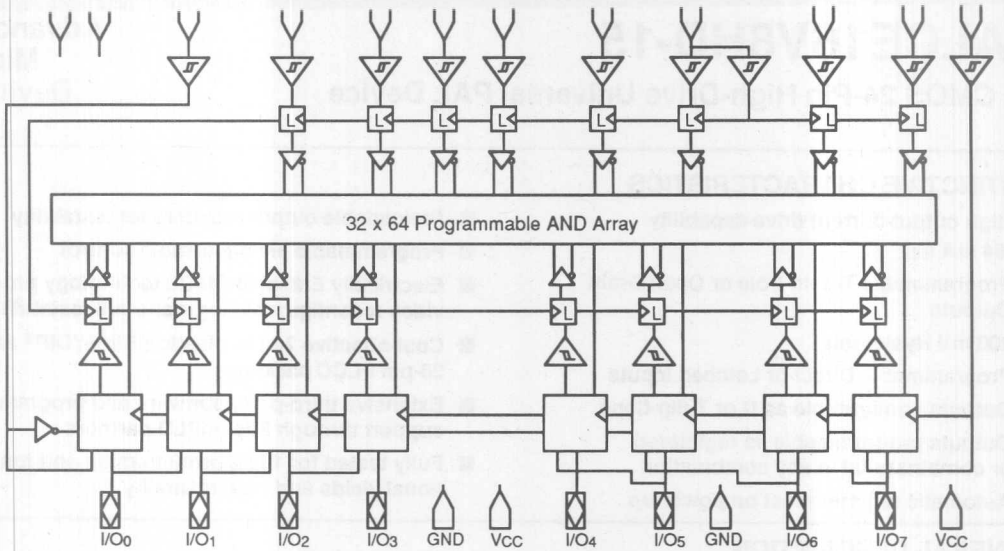
The PALCE16V8HD utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

The PALCE16V8HD has some additional features that make it an ideal choice for bus applications. These include input hysteresis of 200 mV, clean output-switching signals, programmable totem-pole or open-drain output configurations, programmable direct or latched inputs, and programmable D- or T-type output registers.

AMD's FusionPLD program allows PALCE16V8HD designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 15559 Rev. D Amendment/0
Issue Date: June 1993

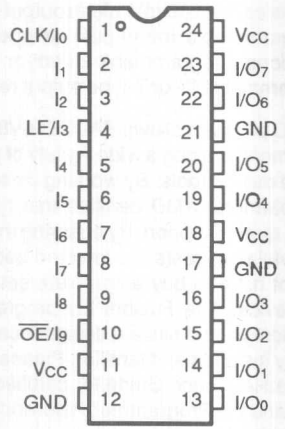


15559D-1

CONNECTION DIAGRAMS

Top View

SKINNYDIP

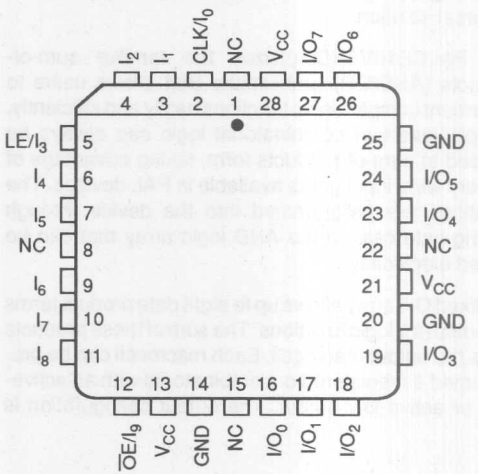


15559D-2

Note:

Pin 1 is marked for orientation.

PLCC



15559D-3

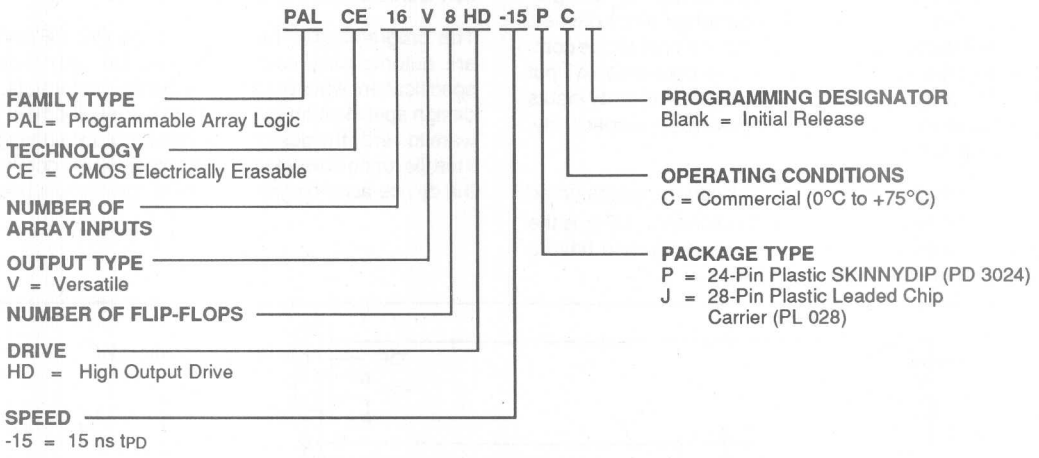
PIN DESIGNATIONS

CLK	=	Clock
LE	=	Latch Enable
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE16V8HD-15	PC, JC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

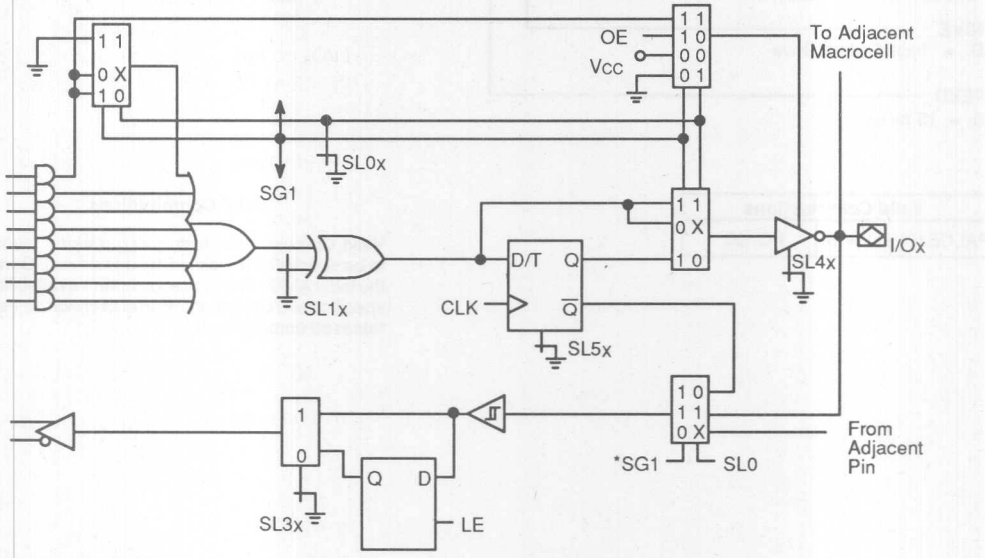
FUNCTIONAL DESCRIPTION

The PALCE16V8HD is a universal PAL device with eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 10 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

All inputs to the array can be individually programmed as either direct or transparent-latch inputs. LE/I_3 is the latch enable pin. The inputs to the array also have a minimum of 200 mV of hysteresis.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

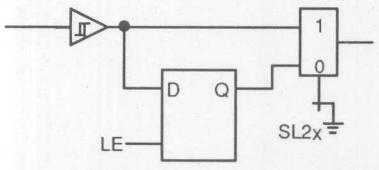
The programmable functions on the PALCE16V8HD are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

15559D-4

Figure 1. PALCE16V8HD I/O Macrocell



15559D-5

Figure 2. PALCE16V8HD Input Macrocell

Device Configuration

The configuration of the PALCE16V8HD is controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 48 local bits ($SL0_0$ through $SL0_7$, $SL1_0$ through $SL1_7$, $SL2_1$ through $SL2_8$, $SL3_0$ through $SL3_7$, $SL4_0$ through $SL4_7$ and $SL5_0$ through $SL5_7$). SG0 determines whether registers will be allowed. SG1 and the individual SL0x bits select the output macrocell configuration as registered output, combinatorial input, combinatorial output, or combinatorial I/O. SL3x sets the feedback path to the array as either direct or latched. SL4x sets the output buffer as either a totem pole or an open drain. SL5x sets the register as either a D or T type flip-flop. At each input pin, SL2x sets the input as direct or latched.

Input Pin Configuration Options

Each input pin can be configured as either a direct input or a transparent latch. The input-pin configuration is set by the local fuse SL2x. When SL2x is unprogrammed, the input is direct. When SL2x is programmed, the input is through a corresponding transparent latch.

The latch is enabled via LE/I_3. The latches hold data when LE/I_3 is low. They are transparent when LE/I_3 is HIGH.

I/O Macrocell Configuration Options

Each I/O macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 10 ($\overline{OE}$) and MC_7 from pin 1 (CLK). These configurations are summarized in Table 1 and illustrated in Figure 3.

The feedback path in each macrocell can be programmed as either direct or latched. The feedback configuration is set by the local fuse SL3x. When SL3x is unprogrammed, the corresponding feedback path is direct to the array. When SL3x is programmed, the corresponding feedback path is through a corresponding transparent latch.

The latch is enabled via LE/I_3. The latches hold data when LE/I_3 is LOW. They are transparent when LE/I_3 is HIGH.

Registered Output Configurations

There are two registered configurations: D-type and T-type. The type is selected by SL5x.

In the registered configurations all eight product terms are available as inputs to the OR gate. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The output buffer is enabled by OE.

Feedback to the array can be either direct or latched. Direct feedback is from Q of the register to the product-term array. Latched feedback is from Q of the register through a transparent latch to the product-term array. LE/I_3 is the latch-enable signal.

Combinatorial Configurations

The PALCE16V8HD has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

In this configuration, the output buffer is always enabled; therefore all eight product terms are available to the OR gate. The feedback to the array is from an adjacent I/O pin. I/O_3 and I/O_4 do not have connections to adjacent macrocells; therefore, MC_3 and MC_4 do not have feedback to the array in this mode.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 10 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 10 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

Only seven product terms are available to the OR gate in this configuration. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 10 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 10 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

In this configuration only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The output buffer is disabled in this configuration. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 10.

Pins 16 (19) and 19 (23) do not have connections to adjacent macrocells. The dedicated-input configuration is not available on these pins.

Device Uses Registers				
0	1	0	0	T-Type Registered Output
0	1	0	1	D-Type Registered Output
Device Uses No Registers				
1	0	0	X	Combinatorial Output
1	0	1	X	Dedicated Input
1	1	1	X	Combinatorial I/O

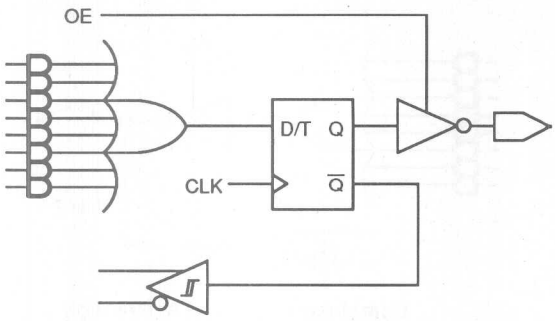
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

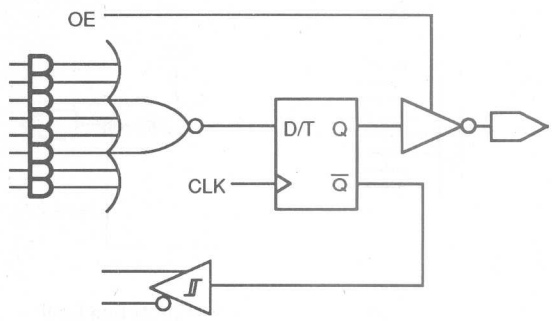
low if $SL1_x$ is 0.

Output Buffer Configurations

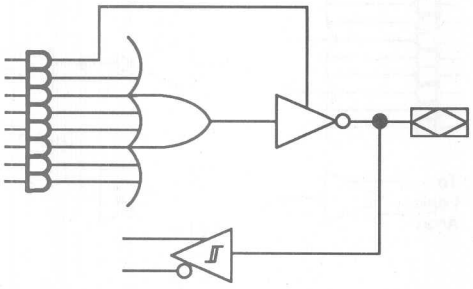
The output buffer can be configured as either a totem-pole output or an open-drain output. This configuration is set by $SL4_x$. The buffer is a totem-pole output when $SL4_x$ is unprogrammed and an open-drain output when $SL4_x$ is programmed. In the totem-pole configuration, the output voltage levels are the standard V_{OH} and V_{OL} levels. In the open-drain configuration, V_{OL} is the standard value. However, V_{OH} will depend on the termination circuitry.



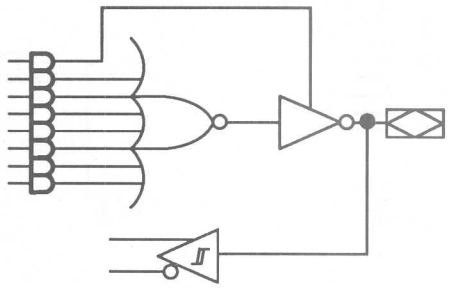
Registered Active Low



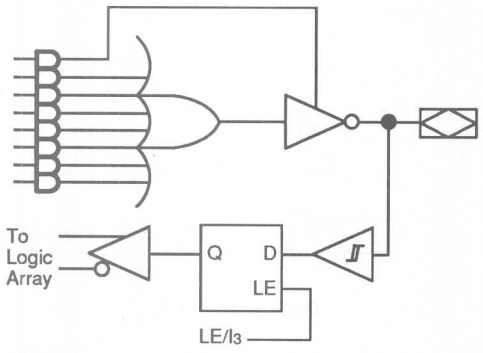
Registered Active High



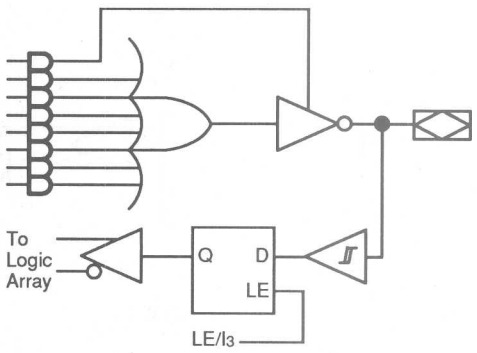
Combinatorial I/O Active Low



Combinatorial I/O Active High



Combinatorial I/O Active Low
with Latched Feedback



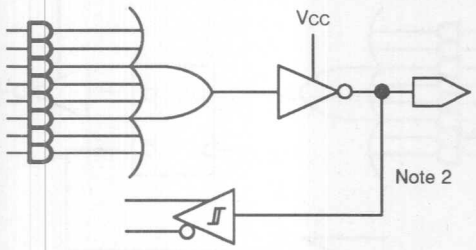
Combinatorial I/O Active High
with Latched Feedback

Note:

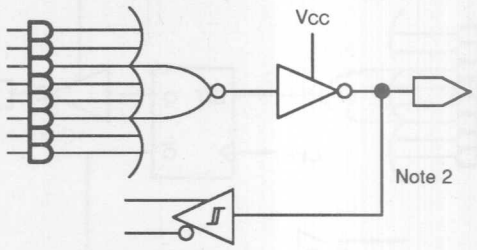
1. *All output and I/O configurations are valid as either totem-pole outputs or open-collector outputs.*

15559D-6

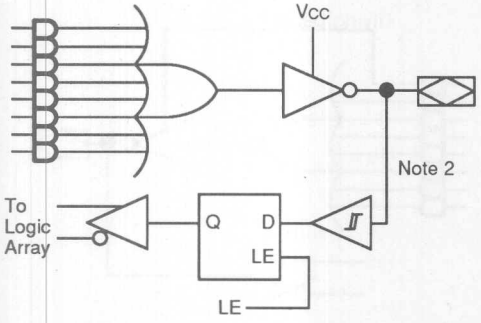
Figure 3. Macrocell Configurations



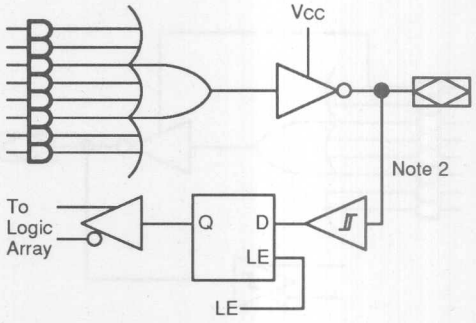
Combinatorial Output Active Low



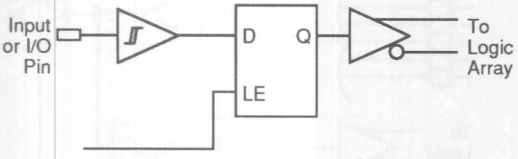
Combinatorial Output Active High



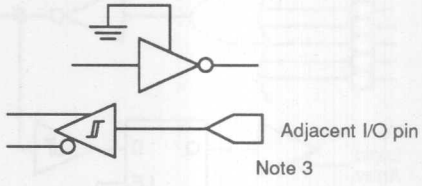
Combinatorial Output Active Low with Latched Feedback



Combinatorial Output Active High with Latched Feedback



Latched Input



Dedicated Input

15559D-7

Notes:

1. *All output and I/O configurations are valid as either totem-pole outputs or open-collector outputs.*
2. *Feedback is not available on pins 16 and 19 in the combinatorial output mode.*
3. *The dedicated-input configuration is not available on pins 16 and 19.*

Figure 4. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8HD will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8HD can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE16V8HD as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8HD device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8HD can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

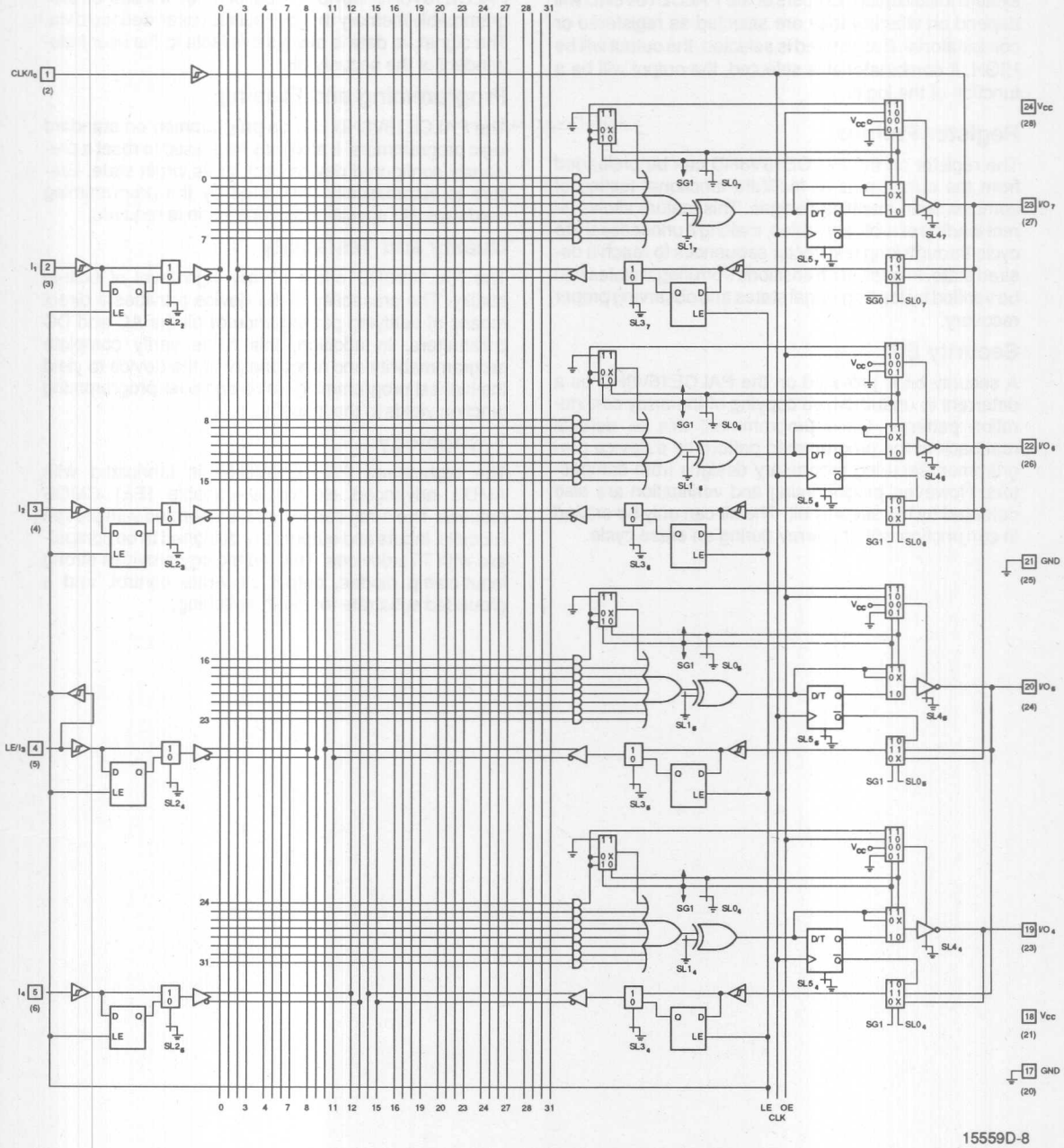
The PAL16V8HD offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this helps verify complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

Technology

The high-speed PALCE16V8HD is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

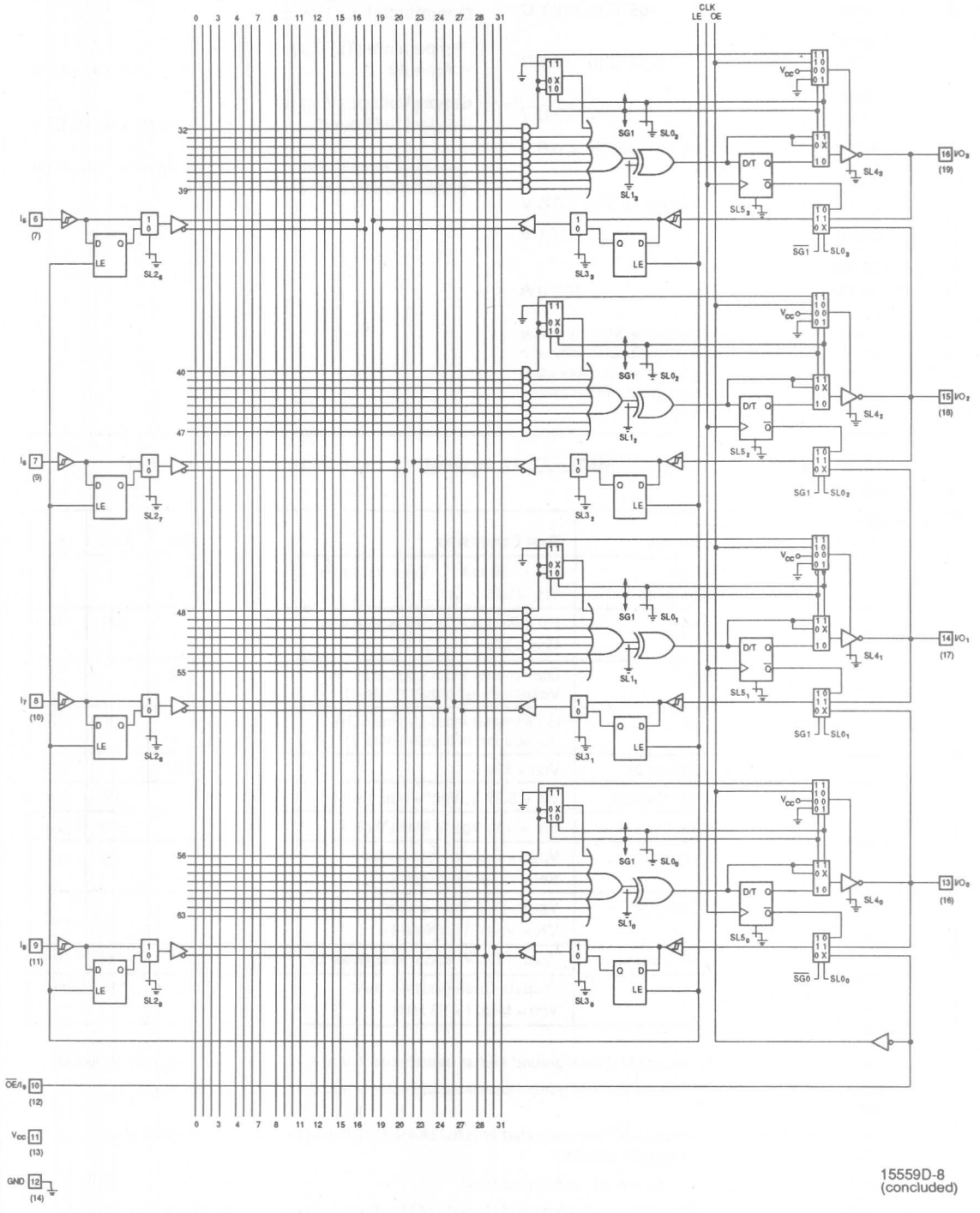
LOGIC DIAGRAM

SKINNYDIP/Flatpack (PLCC) Pinouts



15559D-8

LOGIC DIAGRAM (continued)



15559D-8
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground .....–0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage .....–0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage Totem-pole Configuration	I_{OH} = –16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 64 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_{HYS}	Hysteresis (Notes 2 and 3)	V_{CC} = Min	200		mV
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Hysteresis is the difference between the positive going input threshold voltage and the negative going input threshold voltage.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

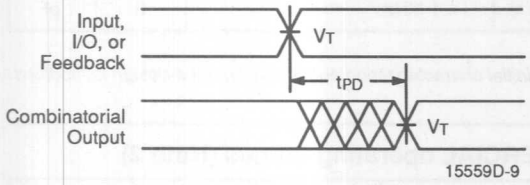
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			10		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width		LOW	6		ns
t_{WH}			HIGH	6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		66		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$	83.3		MHz
t_{SIL}	Input Latch Setup Time			4		ns
t_{HIL}	Input Latch Hold Time			6		ns
t_{IGO}	Input Latch Enable to Combinatorial Output				15	ns
t_{WIGH}	Input Latch Enable Width HIGH			15		ns
t_{IGS}	Input Latch Enable to Output Register Setup Time			10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch				15	ns
t_{SLR}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Register			10		ns
t_{HLR}	Hold Time from Input, I/O or Feedback Through Input Latch to Output Register			0		ns
t_{PZX}	$\overline{OE}$ to Output Enable				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15	ns
t_{EA}	Input, I/O, or Feedback to Output Enable				15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable				15	ns
t_{EAL}	Input, I/O, or Feedback to Output Enable Through Transparent Latch (Note 3)				15	ns
t_{ERL}	Input, I/O, or Feedback to Output Disable Through Transparent Latch (Note 3)				15	ns

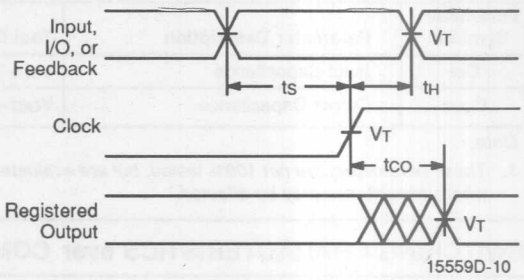
Notes:

2. *See Switching Test Circuit, page 15, for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

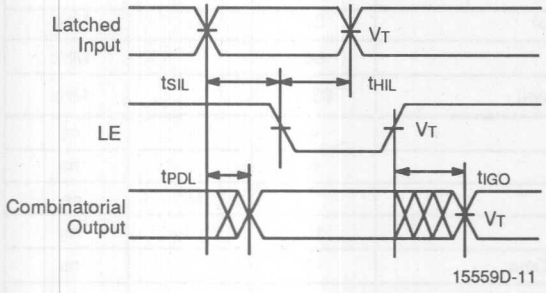
SWITCHING WAVEFORMS



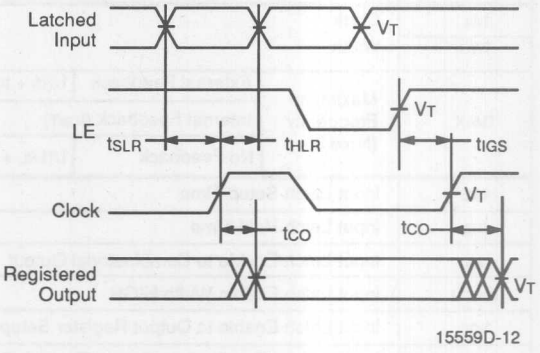
Combinatorial Output



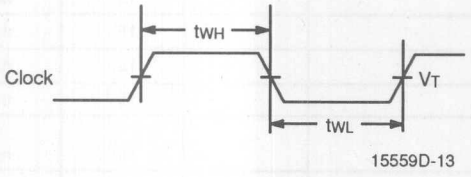
Registered Output



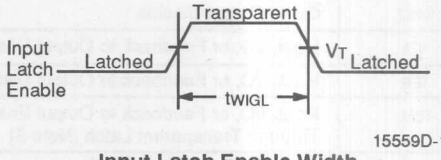
Latched Input with Combinatorial Output



Latched Input with Registered Output



Clock Width

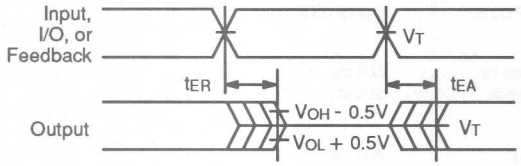


Input Latch Enable Width

Notes:

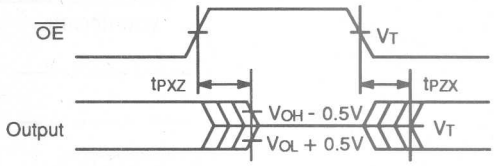
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns – 5 ns typical.*

SWITCHING WAVEFORMS



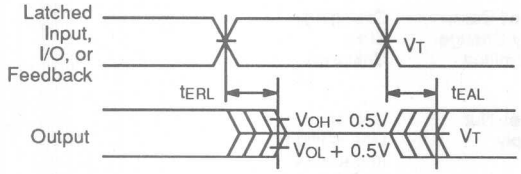
15559D-15

Input to Output Disable/Enable



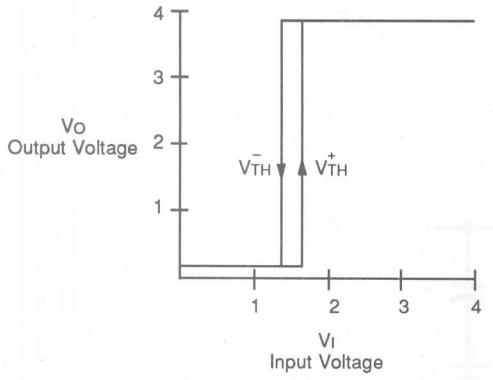
15559D-16

OE to Output Disable/Enable

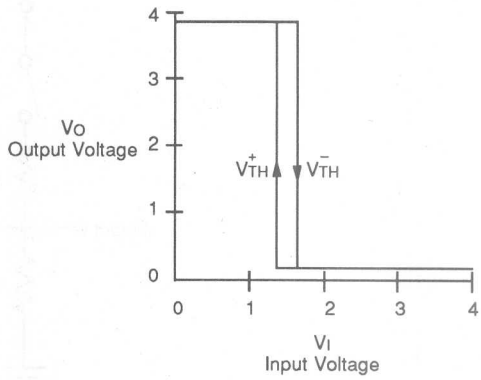


15559D-17

Input to Output Disable/Enable Through Transparent Latch



15559D-18

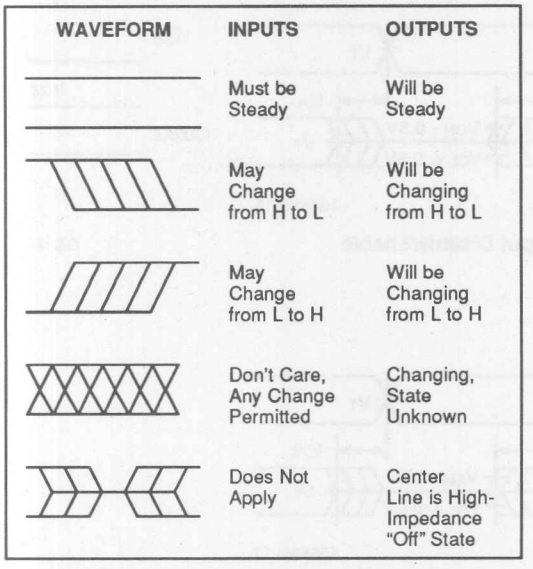


15559D-19

Notes:

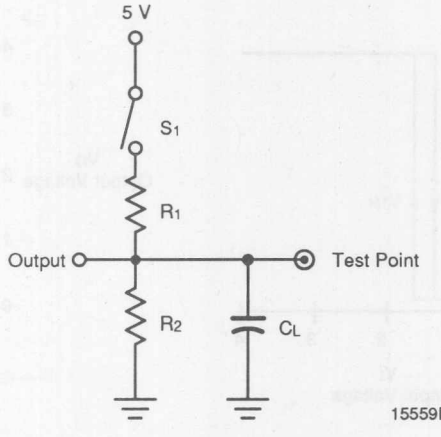
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



15559D-20

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{PDL}, t_{CO}	Closed	50 pF	80 Ω	160 Ω	1.5 V
t_{PZX}, t_{EA}, t_{EAL}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}, t_{ERL}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

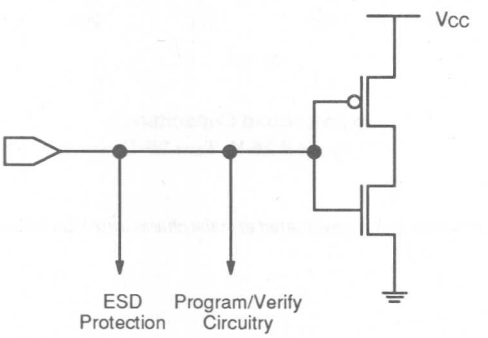
ENDURANCE CHARACTERISTICS

The PALCE16V8HD is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

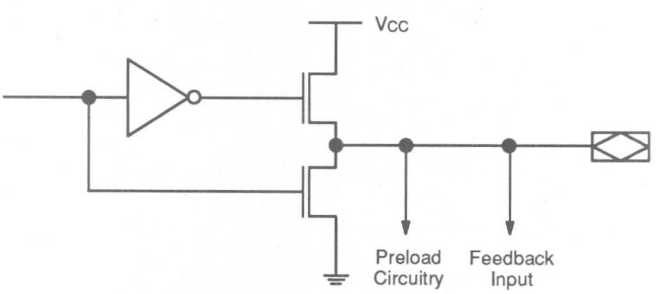
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature (Military)	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS

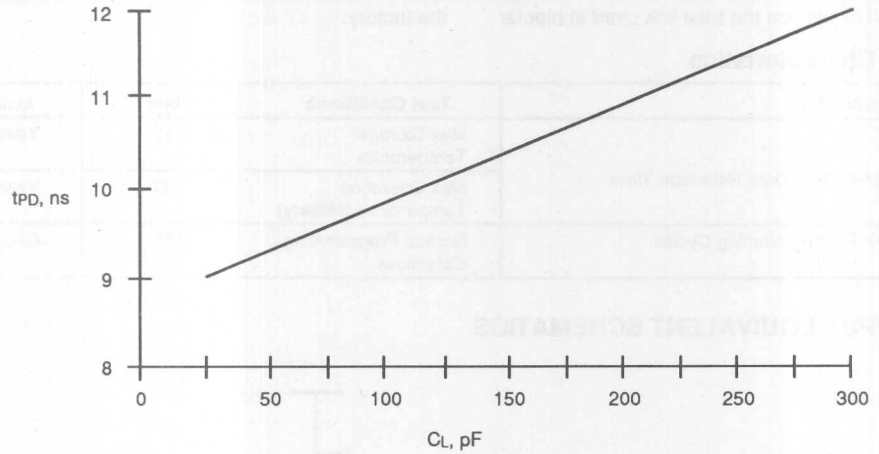


Typical Input



Typical Output

15559D-21



t_{PD} vs. Load Capacitance
V_{CC} = 5.25 V, T_A = 25°C

15559D-22

Note:

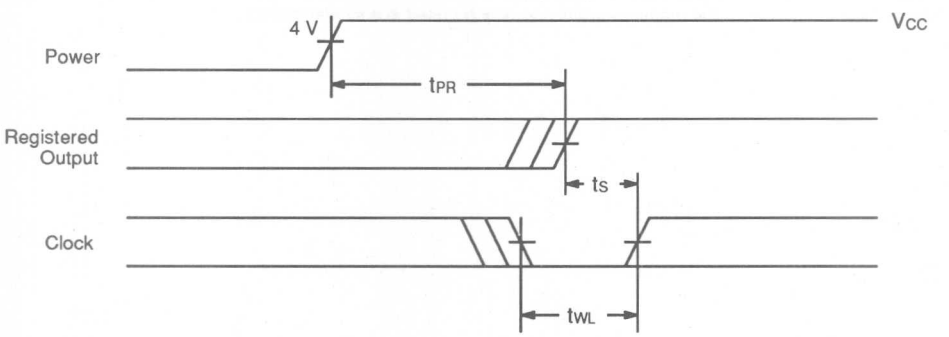
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.*

POWER-UP RESET

The PALCE16V8HD has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



15559D-23

Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

PALCE16V8HD-15

Parameter Symbol	Parameter Description		Typ. SKINNYDIP	Typ. PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		22	17	°C/W
θ_{ja}	Thermal impedance, junction to ambient		70	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	65	47	°C/W
		400 lfpm air	60	42	°C/W
		600 lfpm air	56	38	°C/W
		800 lfpm air	53	36	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL COM'L

AmPAL18P8B/AL/A/L

20-Pin Combinatorial TTL Prorammable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 15 ns maximum propagation delay**
- **Universal combinatorial architecture**
- **Programmable output polarity**
- **Programmable replacement for high-speed TTL logic**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **20-pin DIP and 20-pin PLCC packages save space**

GENERAL DESCRIPTION

The AmPAL18P8 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL18P8 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

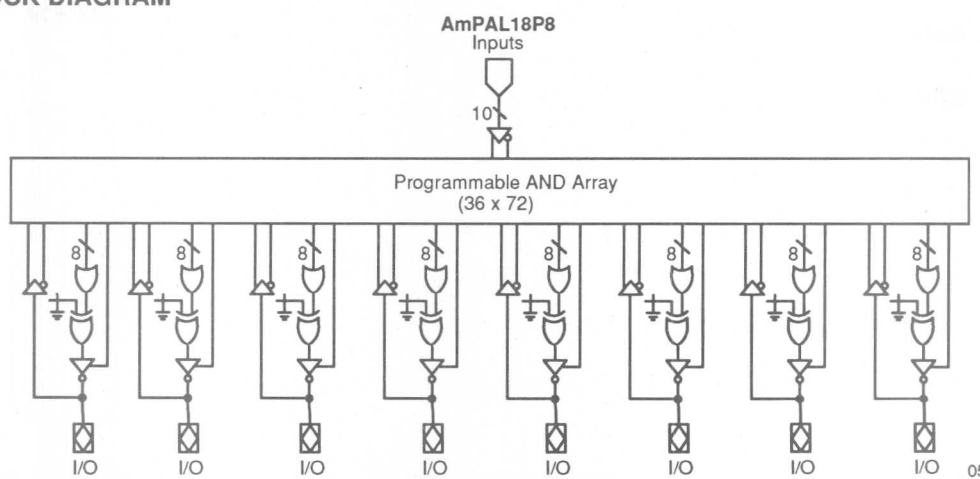
— Variable input/output pin ratio

— Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

BLOCK DIAGRAM



Publication# 05799 Rev. G Amendment /0
Issue Date: January 1992

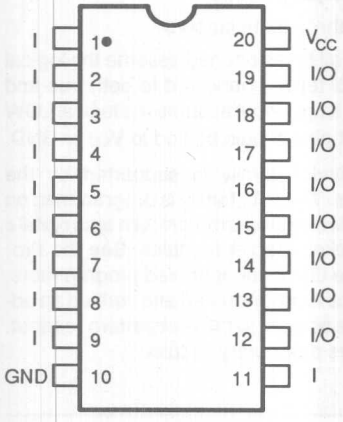
PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max)	I_{CC} mA (Max)	I_{OL} mA (Min)
Very High-Speed ("B") Versions	15	180	24
High-Speed ("A") Versions	25	180	24
High-Speed, Half-Power ("AL") Versions	25	90	24
Half-Power ("L") Versions	35	90	24

CONNECTION DIAGRAMS

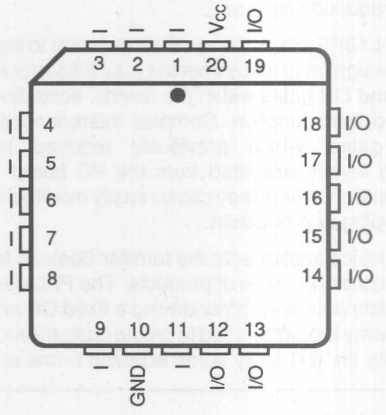
Top View

DIP



05799G-2

PLCC



05799G-3

Note:
Pin 1 is marked for orientation.

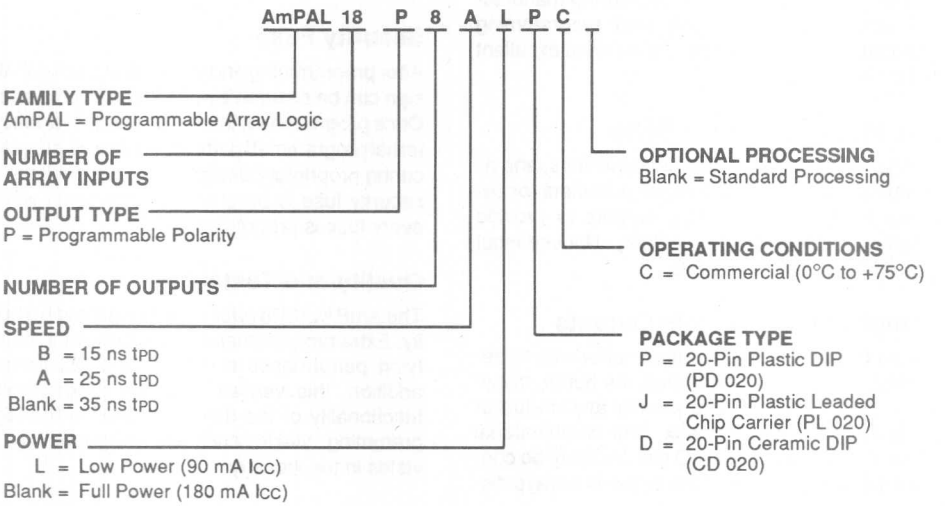
PIN DESIGNATIONS

GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
AmPAL18P8	B, AL, A, L	PC, JC, DC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL18P8 has ten dedicated input lines, and all eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL18P8 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

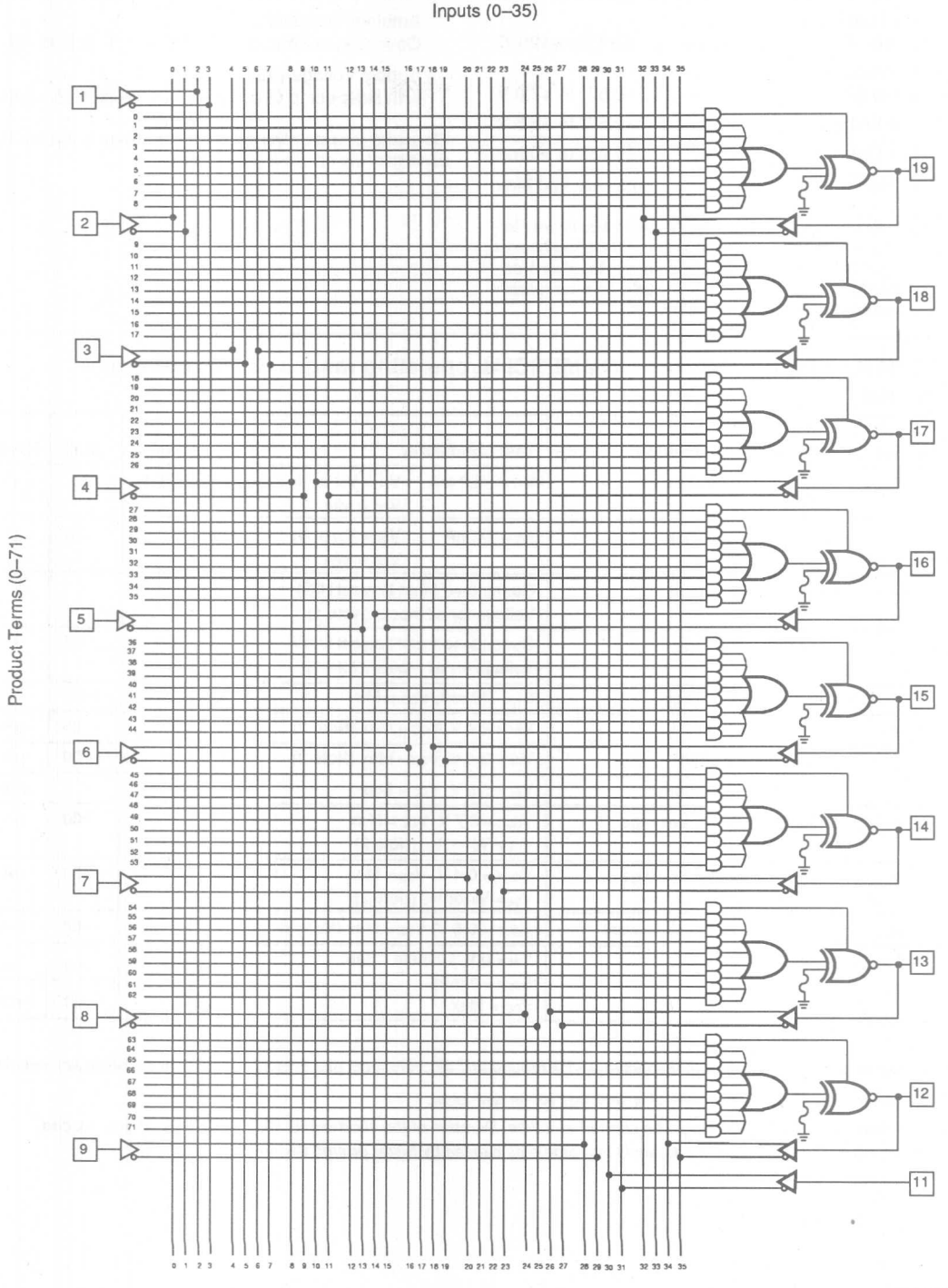
Quality and Testability

The AmPAL18P8 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL18P8 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM



05799G-4

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to +5.5 V

DC Input Current ..... –30 mA to +5 mA

DC I/O Pin Voltage ..... –0.5 V to V_{CC} Max

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–250	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	B, A		180	mA
			AL		90	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

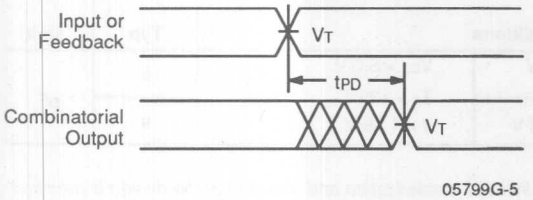
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		L		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output		15		25		35	ns
t_{EA}	Input to Output Enable Using Product Term Control		15		25		35	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25		35	ns

Note:

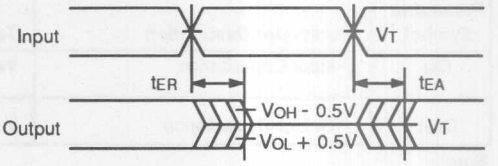
2. *See Switching Test Circuit for test conditions.*

SWITCHING WAVEFORMS



05799G-5

Combinatorial Output



05799G-6

Input to Output Disable/Enable

Notes:

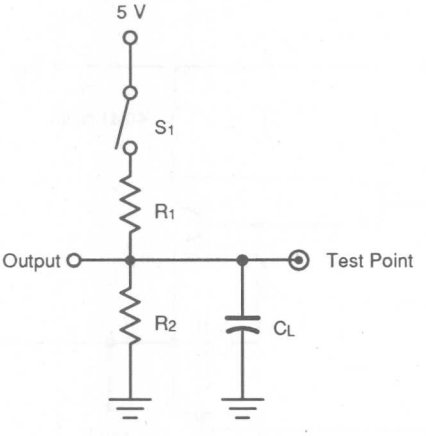
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

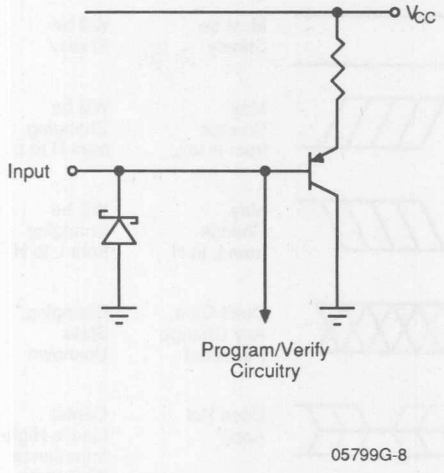
SWITCHING TEST CIRCUIT



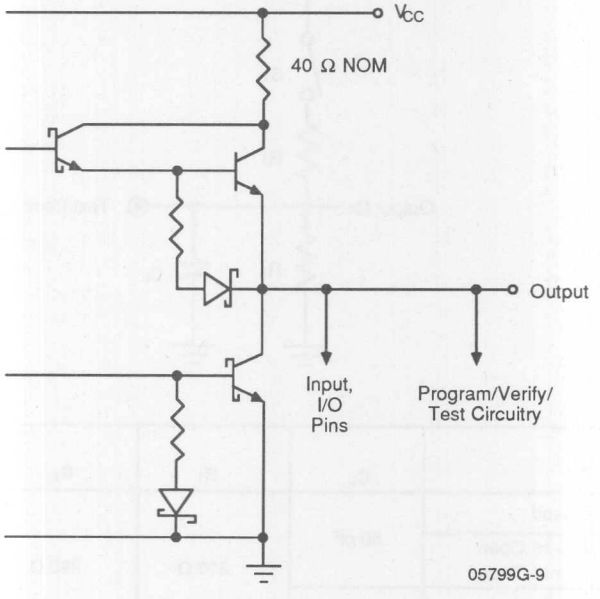
05799G-7

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

PAL20R8 Family

24-Pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 5 ns maximum propagation delay
- Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) includes the PAL20R8-5 Series which is ideal for high-performance applications. The PAL20R8 Family is provided in the standard 24-pin DIP and 28-pin PLCC pinouts.

The devices provide user programmable logic for replacing conventional SSI/LSI gates and flip-flops at a reduced chip cost.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

— Variable input/output pin ratio
— Programmable three-state outputs
— Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

AMD's FusionPLD program allows PAL20R8 Family designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

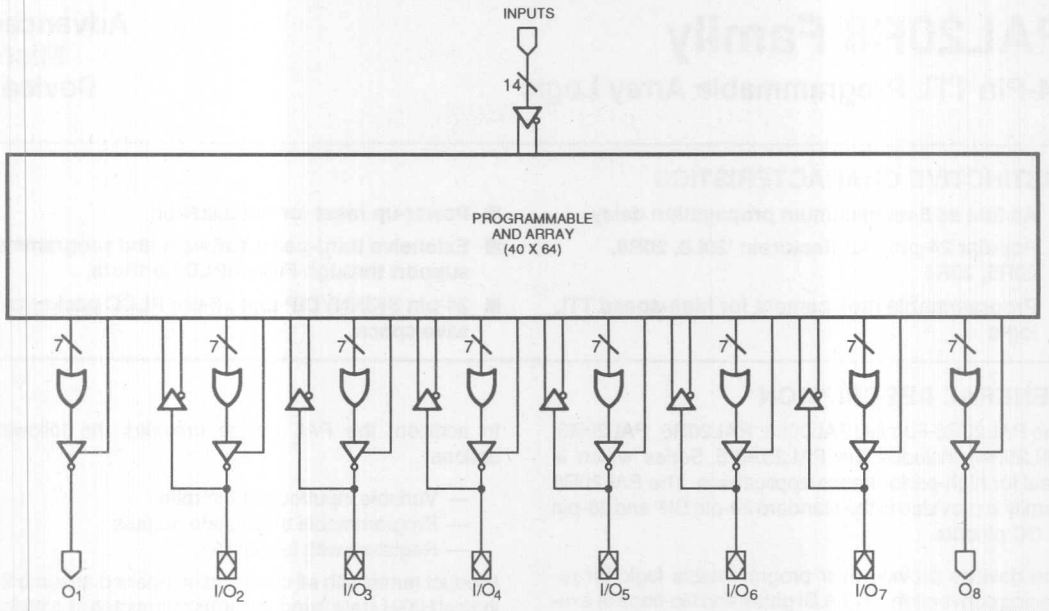
PRODUCT SELECTOR GUIDE

Device	Dedicated Inputs	Outputs	Product Terms/Output	Feedback	Enable
PAL20L8	14	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL20R8	12	8 reg.	8	reg.	pin
PAL20R6	12	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL20R4	12	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Publication# 16490 Rev. B Amendment/0
Issue Date: June 1993

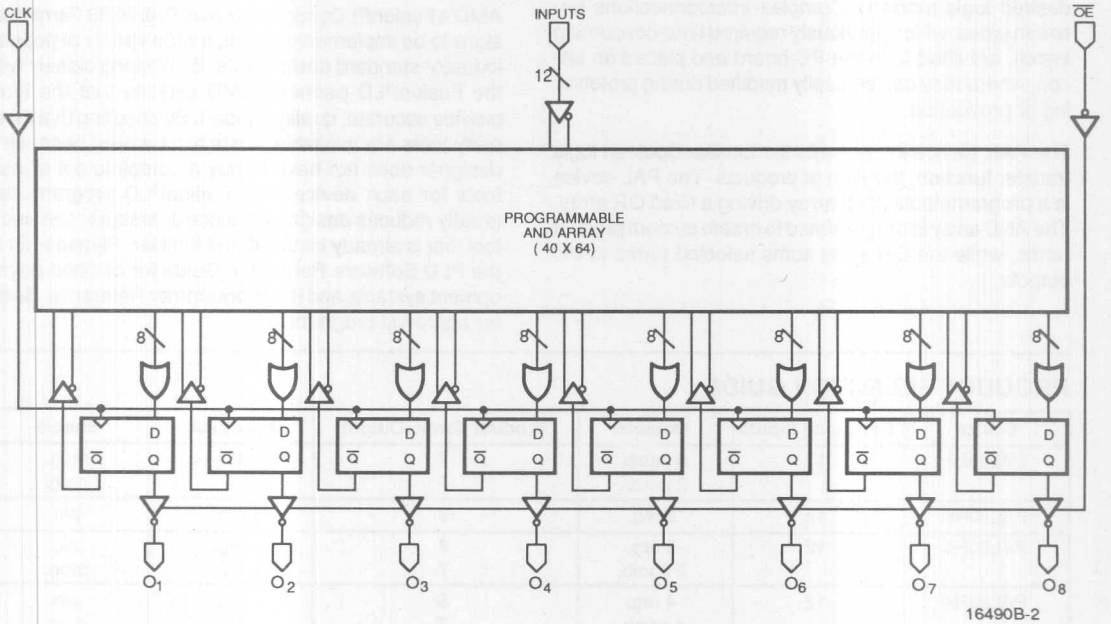
BLOCK DIAGRAMS

PAL20L8



16490B-1

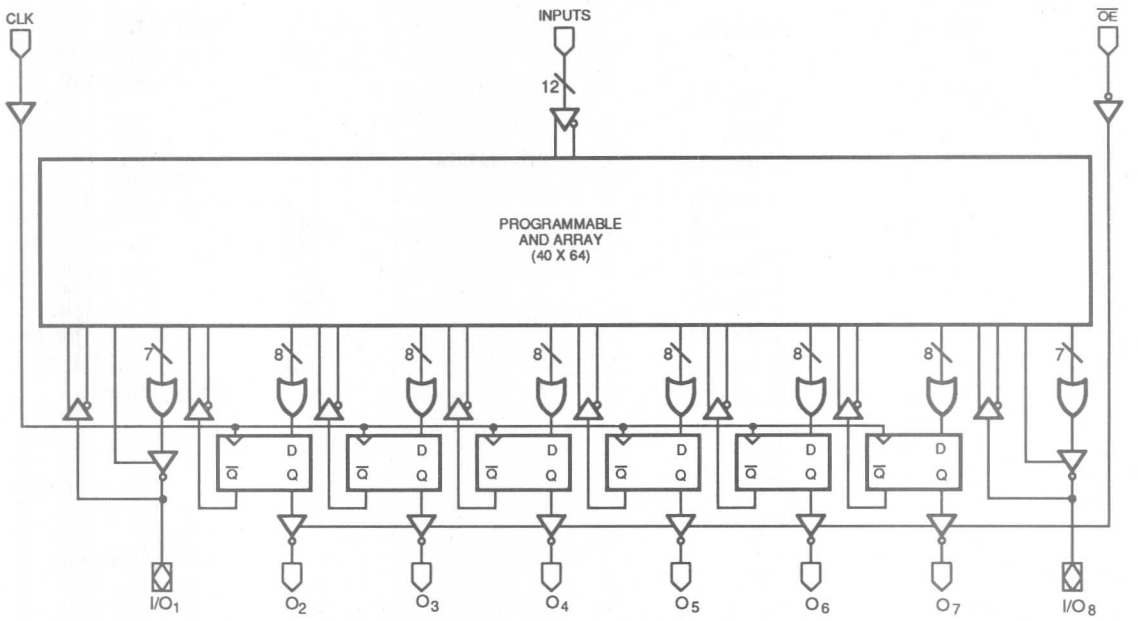
PAL20R8



16490B-2

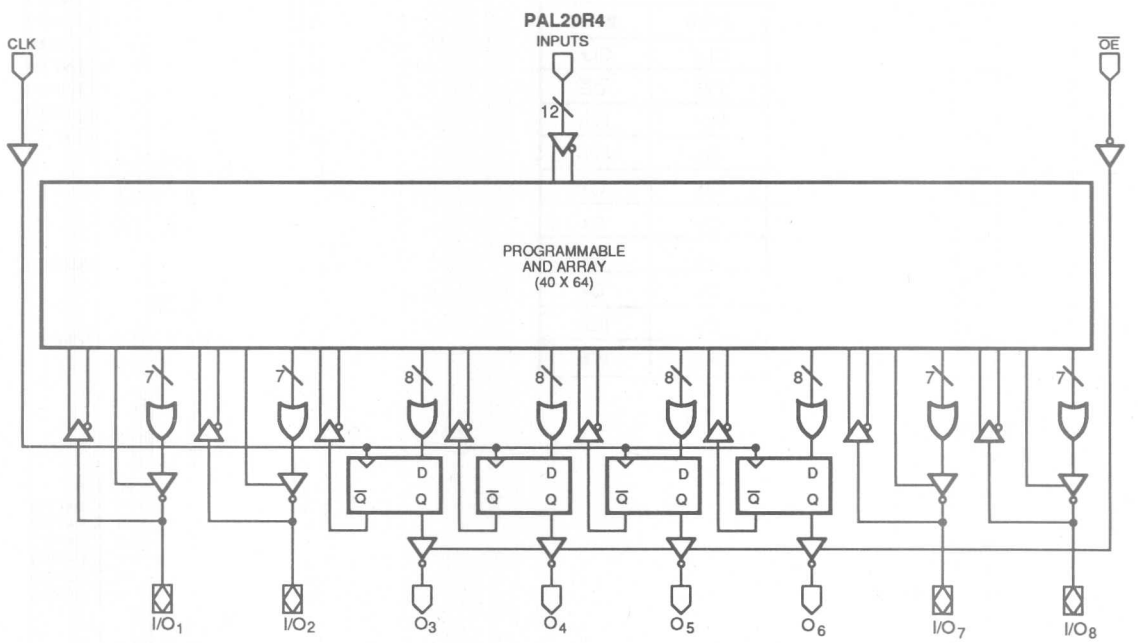
BLOCK DIAGRAMS

PAL20R6



16490B-3

PAL20R4

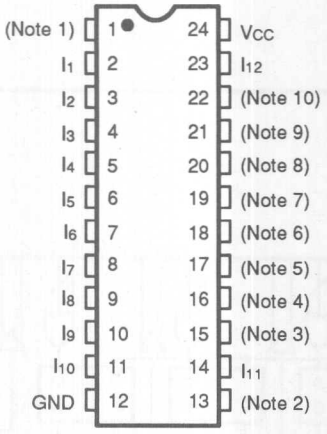


16490B-4

CONNECTION DIAGRAMS

Top View

SKINNYDIP/FLATPACK

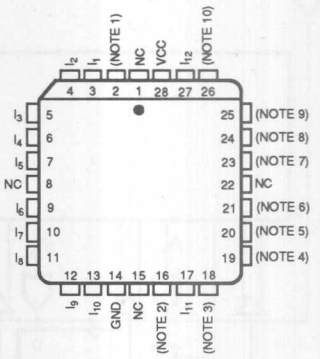


16490B-5

Note: *Pin 1 is marked for orientation.*

PLCC/LCC

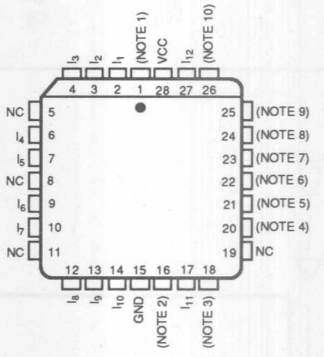
JEDEC: Applies to -5, -7(-12/10 mil), -10(-15 mil), B-2 Series Only



16490B-6

PLCC

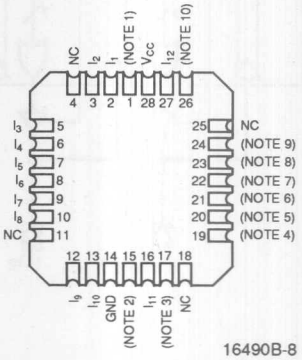
Applies to B and A Series Only



16490B-7

LCC

Applies to B and A Series Only



16490B-8

Note	20L8	20R8	20R6	20R4
1	I_0	CLK	CLK	CLK
2	I_{13}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

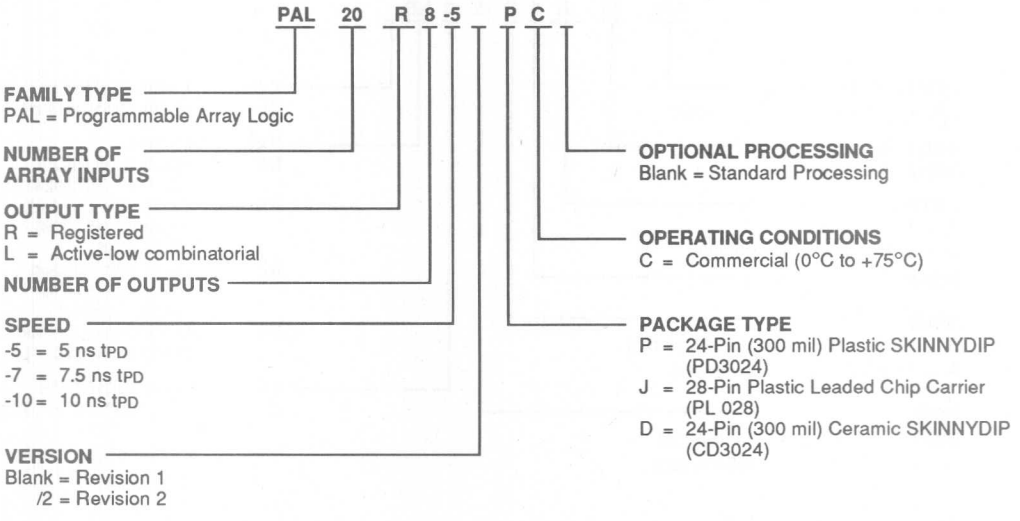
PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
O	=	Output
$\overline{OE}$	=	Output Enable
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL20L8-5	PC, JC
PAL20R8-5	
PAL20R6-5	
PAL20R4-5	
PAL20L8-10/2	
PAL20R8-10/2	
PAL20R6-10/2	
PAL20R4-10/2	
PAL20L8-7	PC, JC, DC
PAL20R8-7	
PAL20R6-7	
PAL20R4-7	

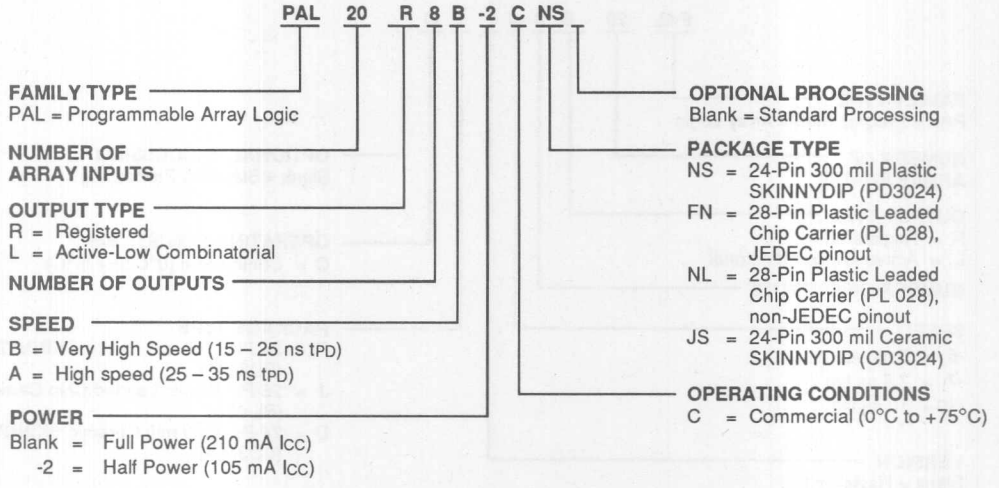
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Commercial Products (MMI Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL20L8	B-2	CNS, CFN, CJS
PAL20R8	B, A	CNS, CNL, CJS
PAL20R6		
PAL20R4		

Valid Combinations

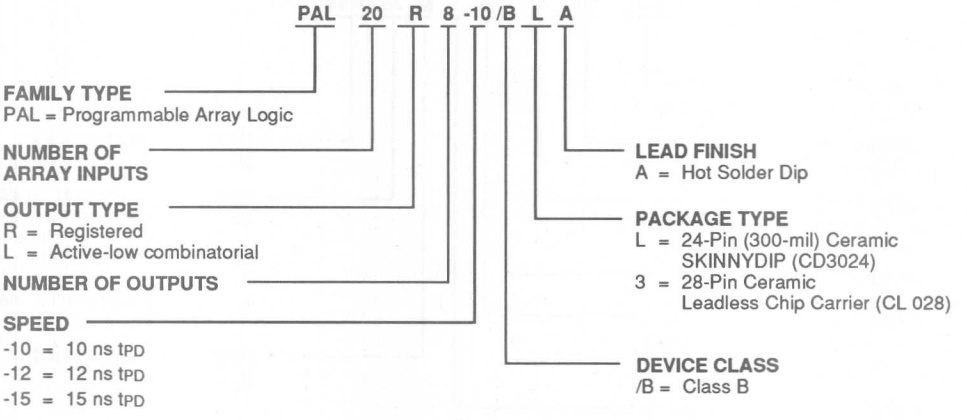
Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

***Note**: Marked with MMI logo.*

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL20L8	-10, -12, -15	/BLA, /B3A
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

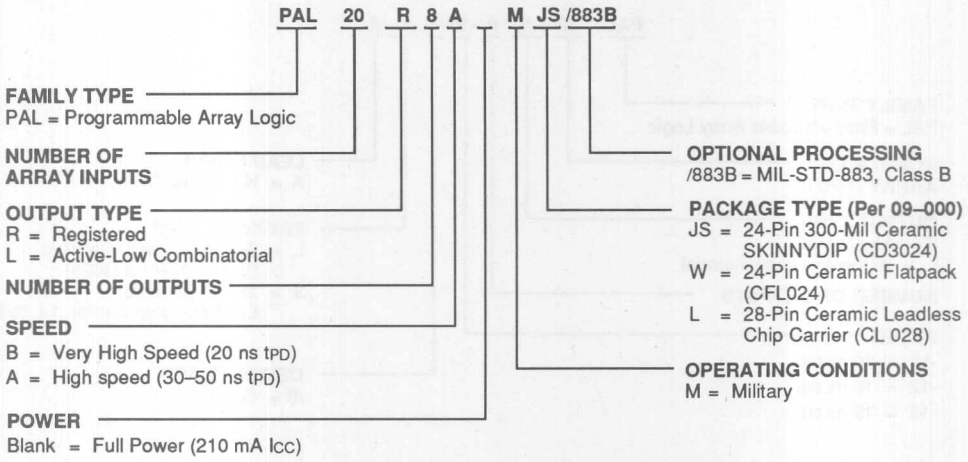
Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL20L8		
PAL20R4		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult

Note: *Marked with MMI logo.*

Group A Tests

Group A Tests consist of Subgroups:
1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Standard 24-Pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Using any of a number of development packages, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL20R8 Family can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is intact.

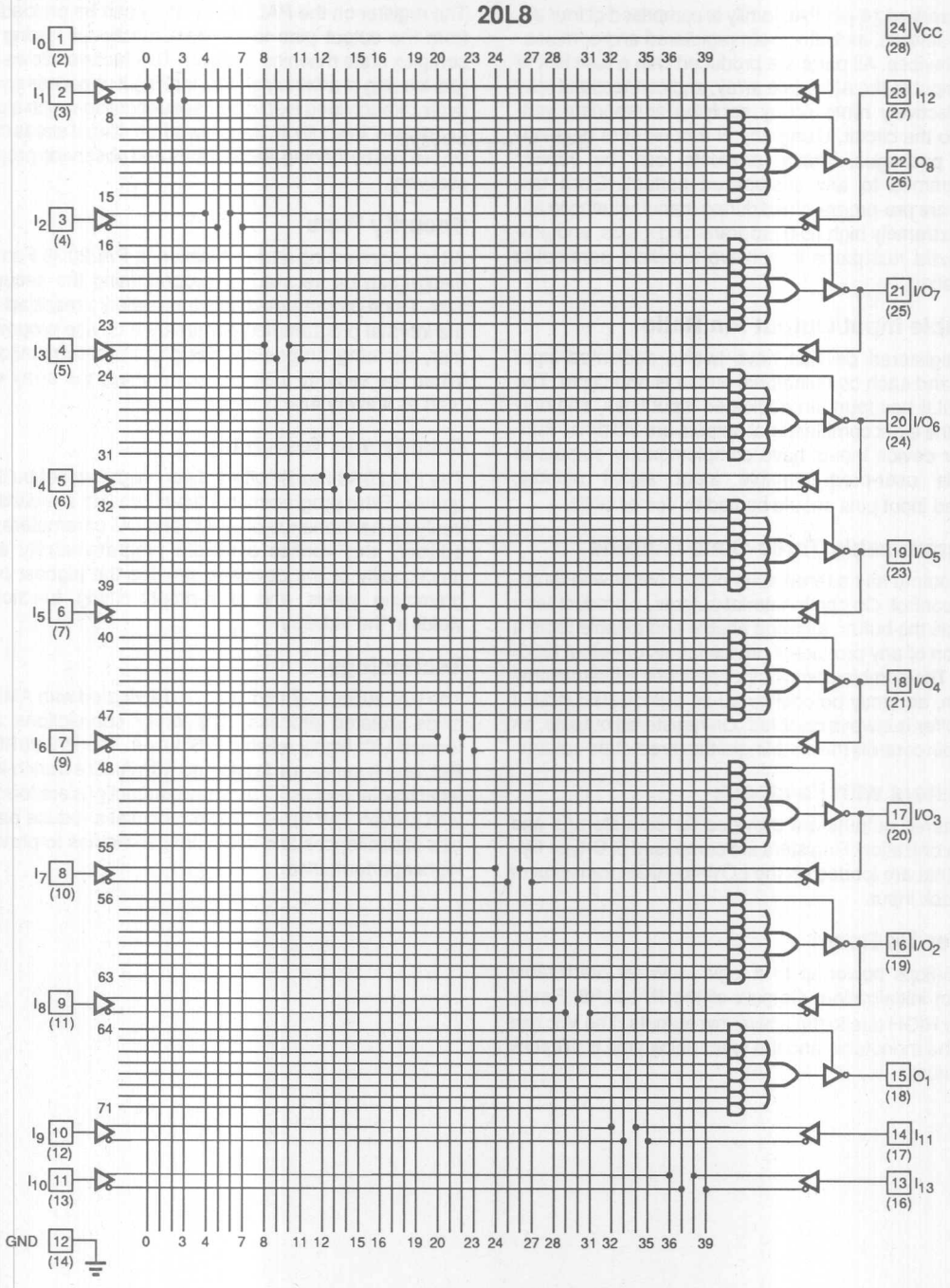
Quality and Testability

The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL20R8-5, -7 and 10/2 are fabricated with AMD's oxide isolated process. The array connections are formed with highly reliable PtSi fuses. The PAL20R8B, B-2, and A series are fabricated with AMD's trench-isolated bipolar process. The array connections are formed with proven TiW fuses. These processes reduce parasitic capacitances and minimum geometries to provide higher performance.

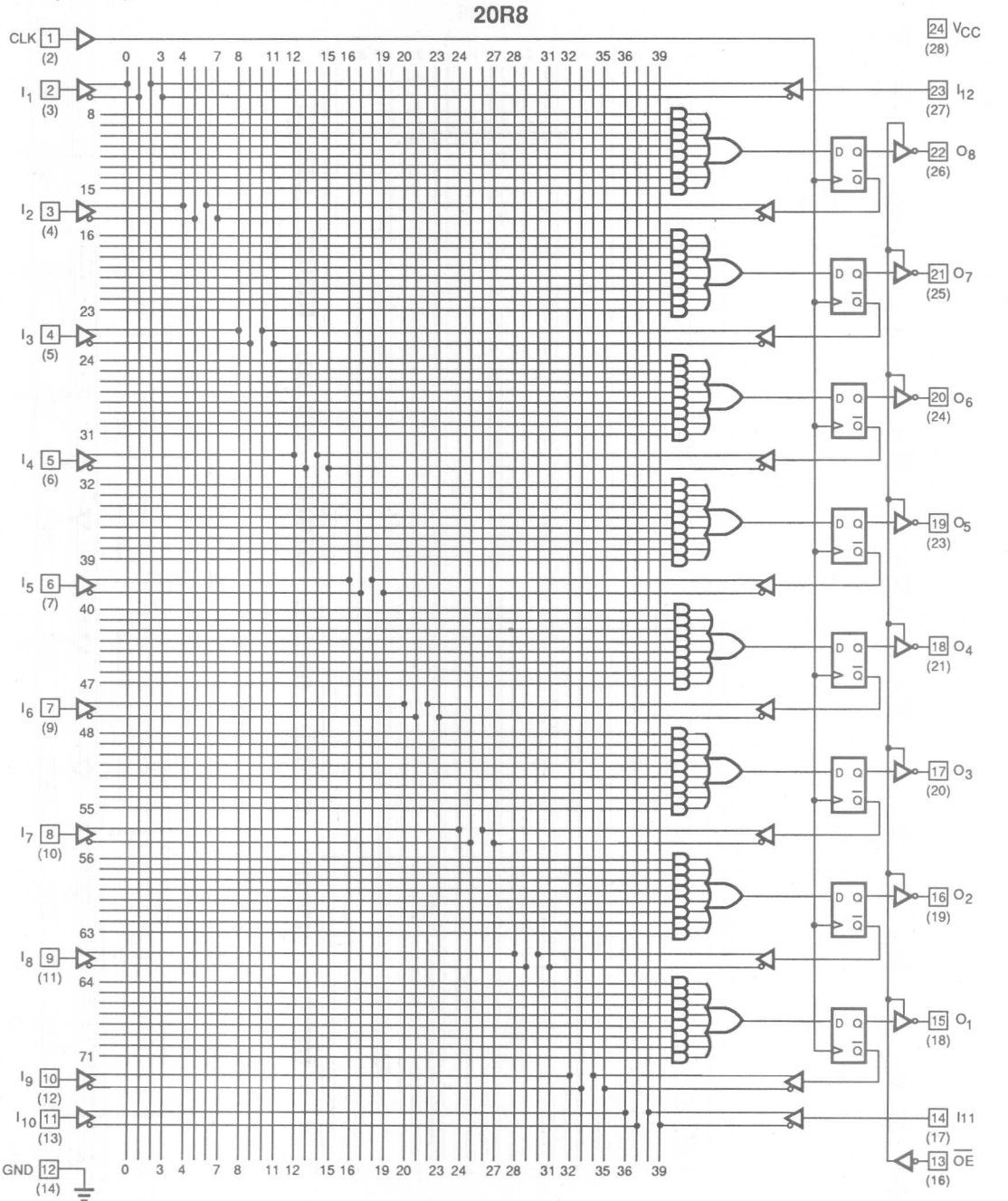
LOGIC DIAGRAM
DIP (PLCC) Pinouts



16490B-9

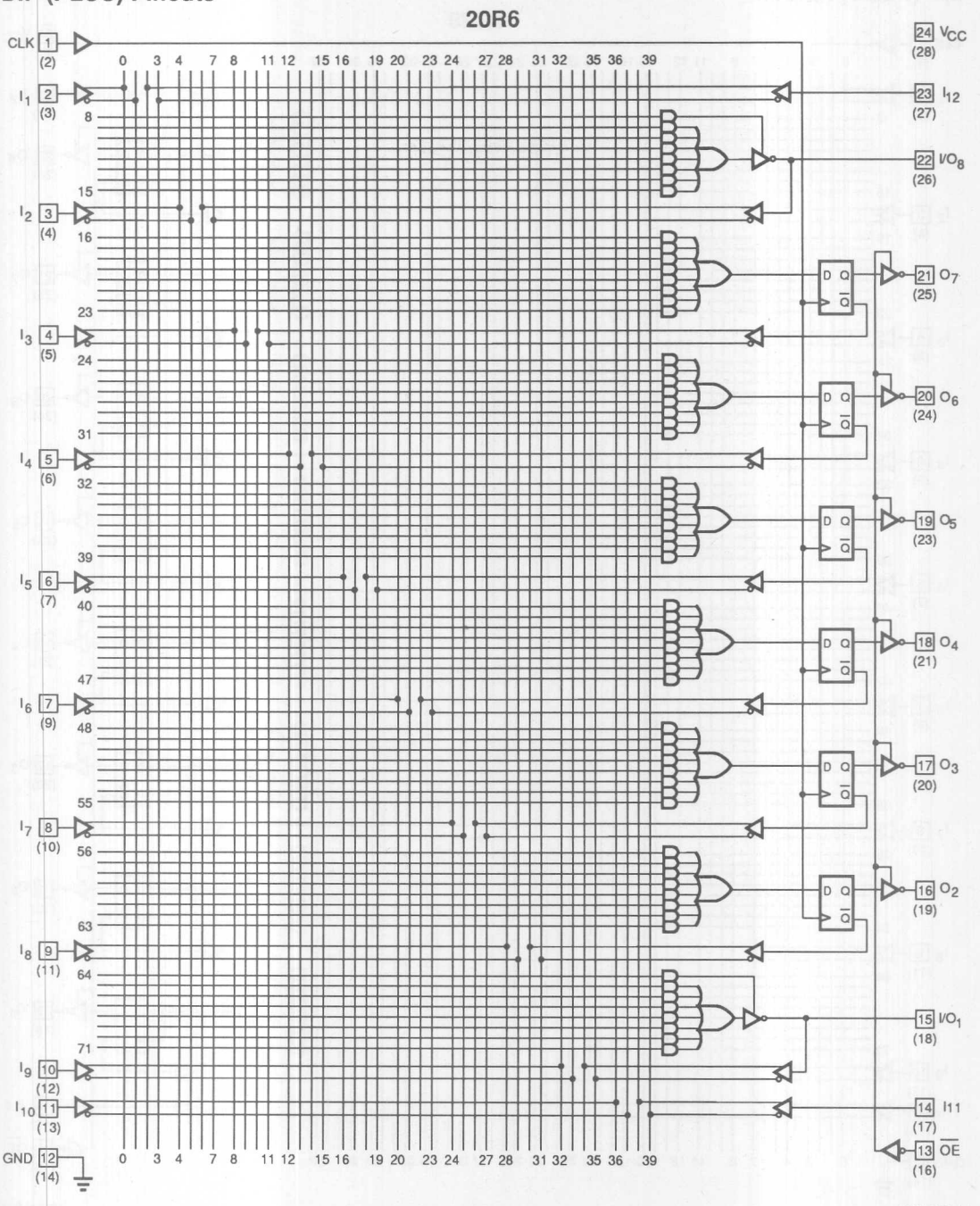
LOGIC DIAGRAM

DIP (PLCC) Pinouts



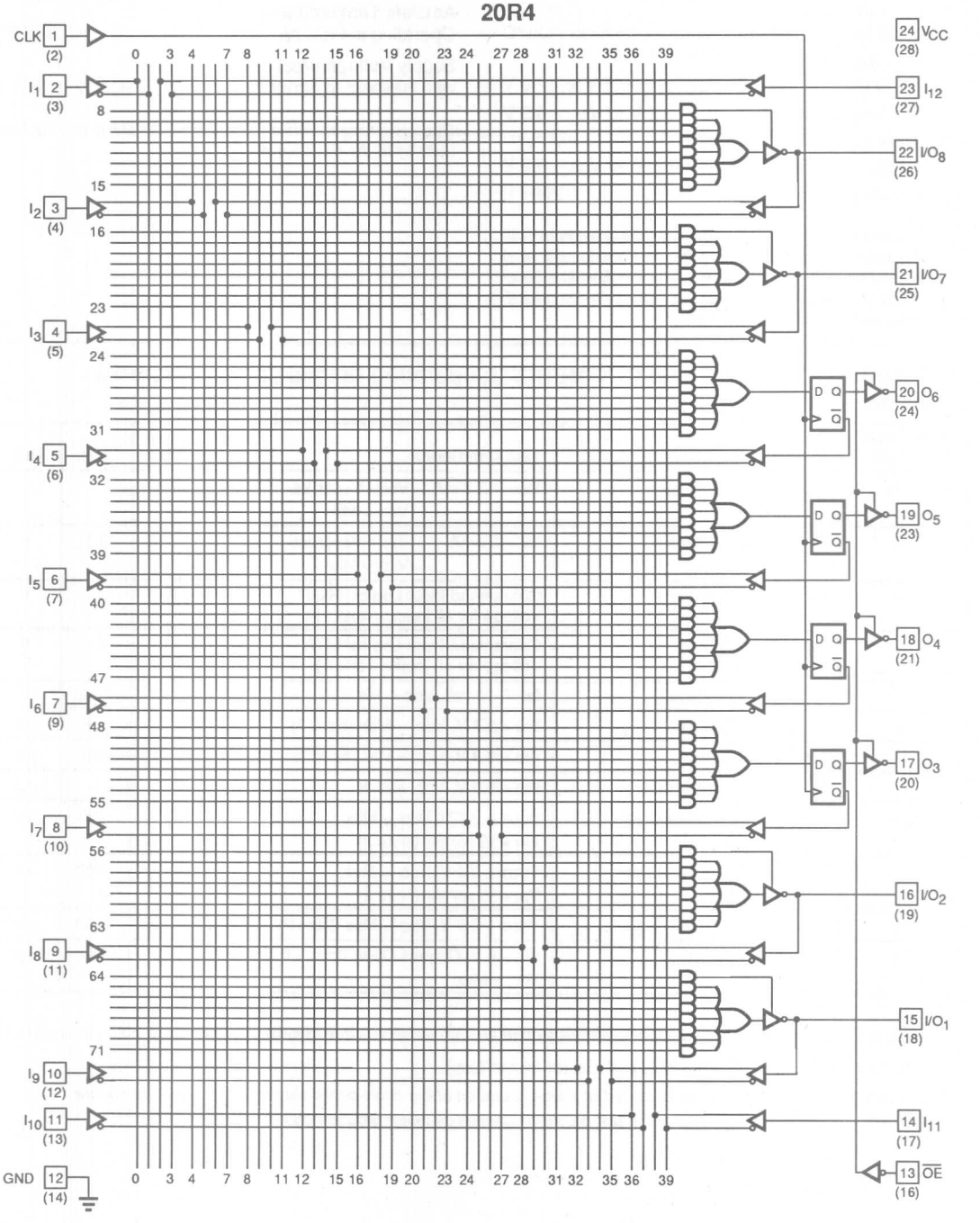
16490B-10

LOGIC DIAGRAM
DIP (PLCC) Pinouts



16490B-11

LOGIC DIAGRAM
DIP (PLCC) Pinouts



16490B-12

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –1.2 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... 4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		210	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	CLK, $\overline{OE}$	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	8	pF
		$I_1 - I_{12}$			5	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	1	5	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	4.5		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				1	4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)					1	ns
t_{WL}	Clock Width	LOW			4		ns
t_{WH}		HIGH			4		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		117		MHz
		Internal Feedback (f_{CNT})			125		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	6.5	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4	2	6.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				2	5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{EA} and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.2 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
With Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		210	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	7.5	ns
		1 Output Switching			3	7	
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	7		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				1	6.5	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1	ns
t_{WL}	Clock Width	LOW			5		ns
t_{WH}		HIGH			5		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		74		MHz
		Internal Feedback (f_{CNT})			100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	8	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA} and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Skew is measured with all outputs switching in the same direction.*
5. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where the frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ... –0.5 V to V_{CC} Max

DC Input Current ..... –30 mA to 5 mA

Static Discharge Voltage ..... 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		210	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	8	ns
t_{WL}	Clock Width	LOW			7		ns
t_{WH}		HIGH			7		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		55.5		MHz
		Internal Feedback (f_{CNT})			58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		71.4		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA} and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		210	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		15	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					12	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		45		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					12	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4		18	ns
t_{ER}	Input to Output Disable Using Product Term Control					15	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		105	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *Calculated from measured f_{MAX} internal.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with
Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		210	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock				25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output			20R8, 20R6,		15	ns
t_{WL}	Clock Width	LOW		20R4	15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6,		25	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4		25	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *Calculated from measured f_{MAX} internal.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

Ambient Temperature
With Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –1.2 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

Operating Case (T_C)
Temperature ..... –55°C to +125°C

Supply Voltage (V_{CC})
with Respect to Ground ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. *Military products are 100% tested at T_C = +25°C, +125°C, and –55°C.*

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		210	mA

Notes:

2. *For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		10	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				-10 Min (Note 3)	-10 Max	-12 Min (Note 3)	-12 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	10	3	12	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	10		12		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output				3	10	3	12	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1		1	ns
t_{WL}	Clock Width	LOW			8		10		ns
t_{WH}		HIGH			8		10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		50		41.7		MHz
		Internal Feedback	(f_{CNT})		62.5		50		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		62.5		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 5)				3	12	3	15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 5)				3	12	3	15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)			20L8, 20R6, 20R4	3	12	3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				3	12	3	15	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{EA} and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Skew is measured with all outputs switching in the same direction.*
5. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} Max

DC Input Current ..... –30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... +125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. *Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.*

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		210	mA

Notes:

2. *For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	CLK, $\overline{OE}$	12	pF
				Other Inputs	7	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		Outputs	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	15	ns
t_S	Setup Time from Input or Feedback to Clock			20L8, 20R6, 20R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	13	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		35.7		MHz
		Internal Feedback (f_{CNT})			37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 6)				3	15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 6)				3	15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 6)			20L8, 20R6, 20R4	3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 6)				3	15	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.*
4. *Calculated from measured f_{MAX} internal.*
5. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –1.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... +125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Note:

1. *Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.*

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		210	mA

Notes:

2. *For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		20	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	20		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6, 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					20	ns

Notes:

1. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –1.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... 5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... +125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. *Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.*

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max		210	mA

Notes:

2. *For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

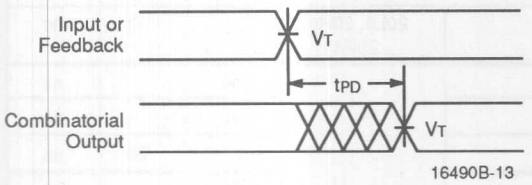
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6, 20R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					30	ns

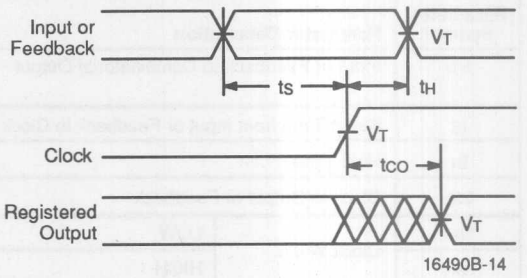
Notes:

1. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
2. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

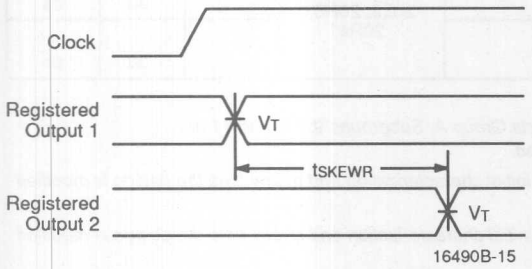
SWITCHING WAVEFORMS



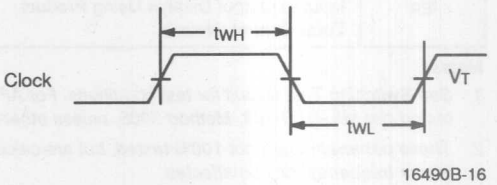
Combinatorial Output



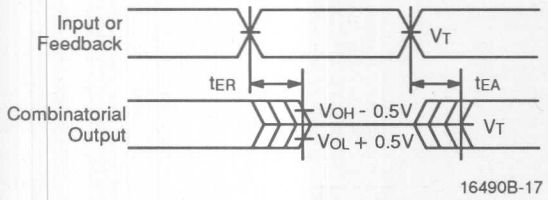
Registered Output



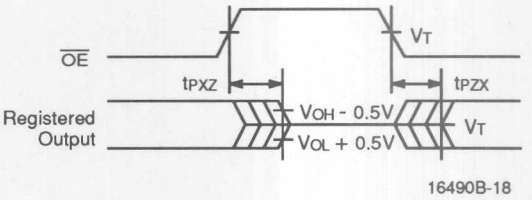
Registered Output Skew



Clock Width



Input to Output Disable/Enable



OE to Output Disable/Enable

Notes:

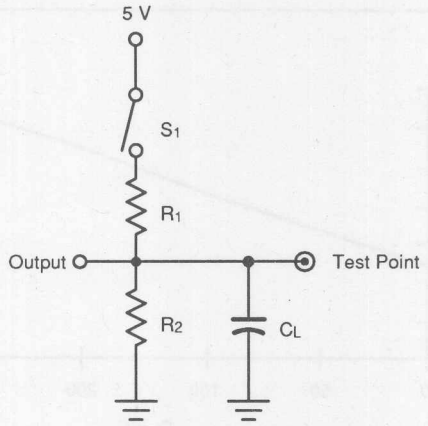
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns – 3 ns typical*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

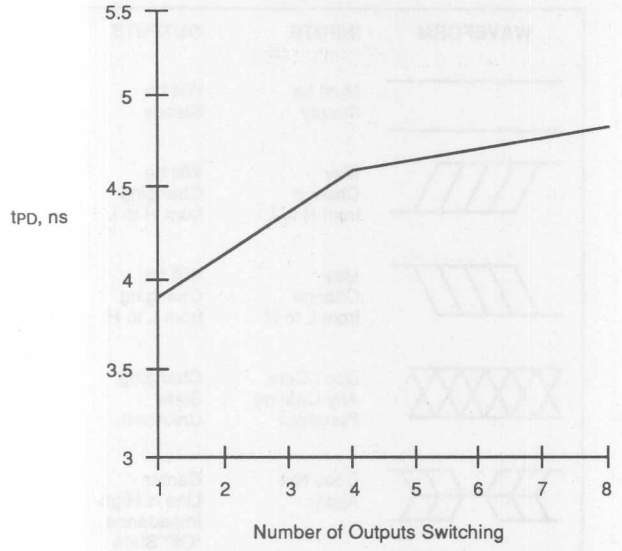
SWITCHING TEST CIRCUIT



16490B-19

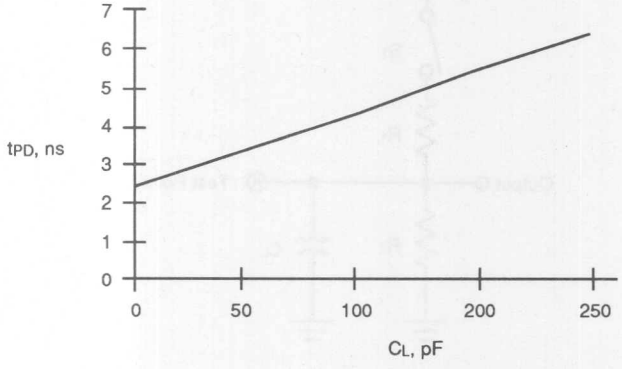
Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	For -5: 200 Ω For rest 390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

MEASURED SWITCHING CHARACTERISTICS FOR THE PAL20R8-5



t_{PD} vs. Number of Outputs Switching
V_{CC} = 4.75 V, T_A = 75°C (Note 1)

16490B-20



t_{PD} vs. Load Capacitance
V_{CC} = 5.0 V, T_A = 25°C

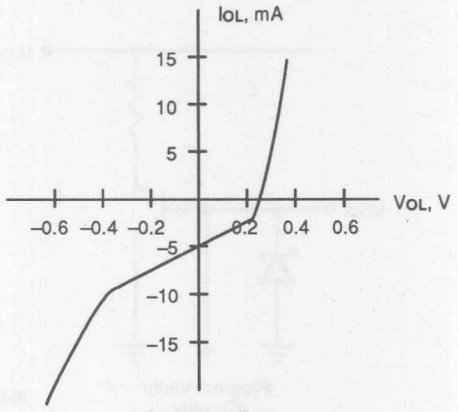
16490B-21

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.*

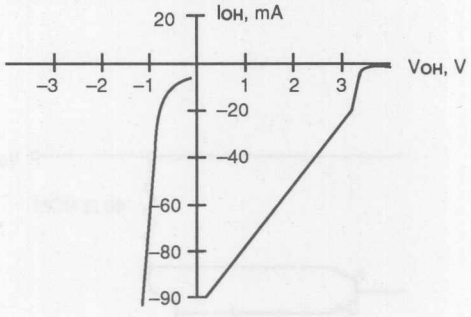
CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS FOR THE PAL20R8-5

V_{CC} = 5.0 V, T_A = 25°C



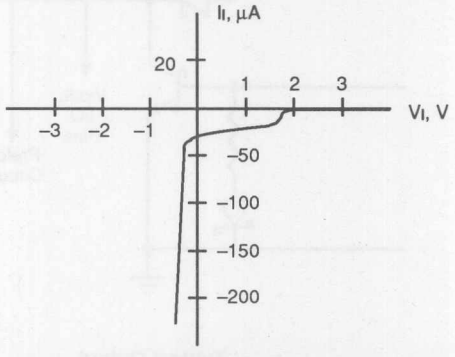
Output, LOW

16490B-22



Output, HIGH

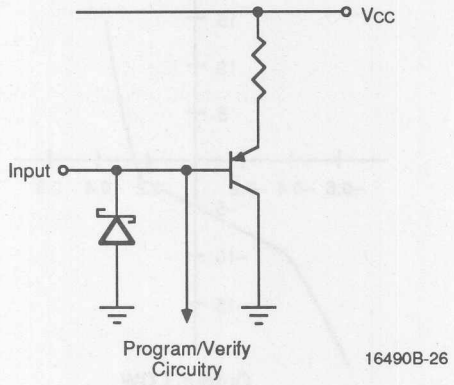
16490B-23



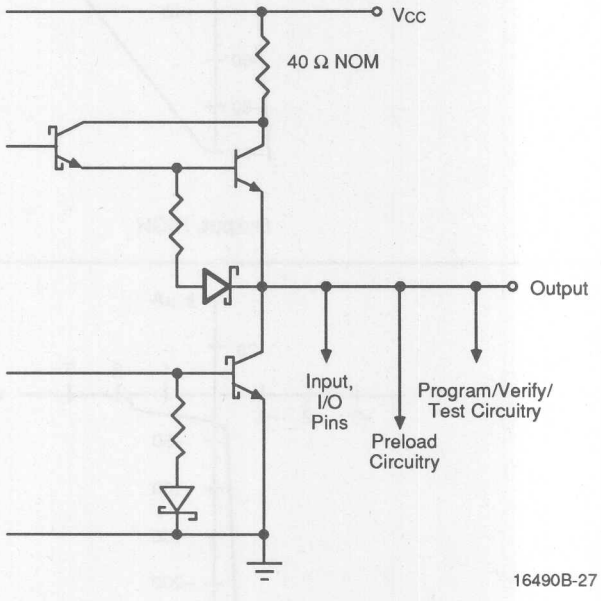
Input

16490B-24

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



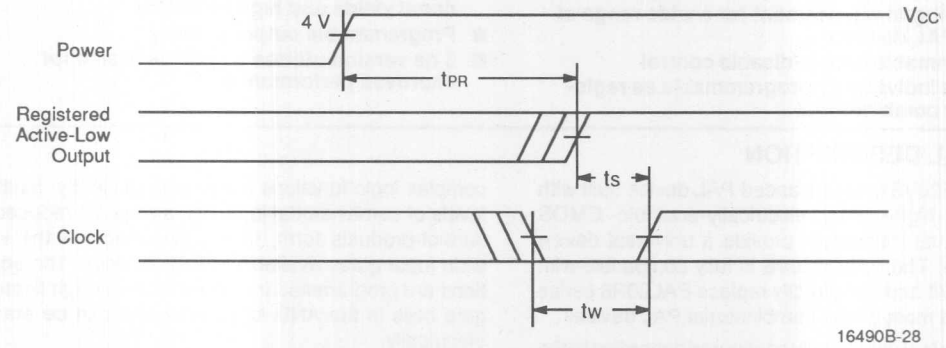
Typical Output

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PALCE20V8 Family

EE CMOS 24-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin, function and fuse-map compatible with all GAL 20V8/As**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - 5 ns propagation delay for "-5" version
  - 7.5 ns propagation delay for "-7" version
- **Direct plug-in replacement for a wide range of 24-pin PAL devices**
- **Programmable enable/disable control**
- **Outputs individually programmable as registered or combinatorial**
- **Preloadable output registers for testability Automatic register reset on power-up**
- **Cost-effective 24-pin plastic SKINNYDIP and 28-pin PLCC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**
- **Programmable output polarity**
- **5 ns version utilizes a split leadframe for improved performance**

GENERAL DESCRIPTION

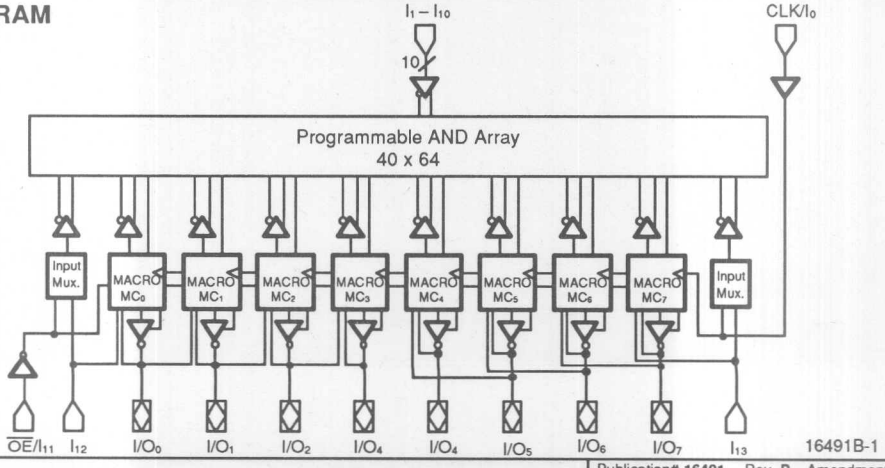
The PALCE20V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture. The PALCE20V8 is fully compatible with the GAL20V8 and can directly replace PAL20R8 series devices and most 24-pin combinatorial PAL devices.

Device logic is automatically configured according to the user's design specification. A design is implemented using any of a number of popular design software packages, allowing automatic creation of a programming file based on Boolean or state equations. Design software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE20V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

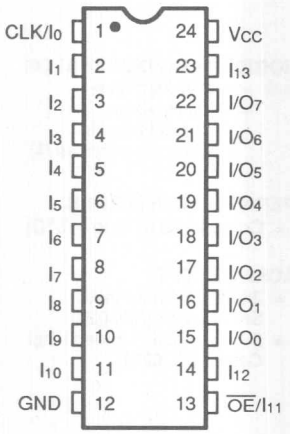
BLOCK DIAGRAM



Publication# 16491 Rev. B Amendment/0
Issue Date: June 1993

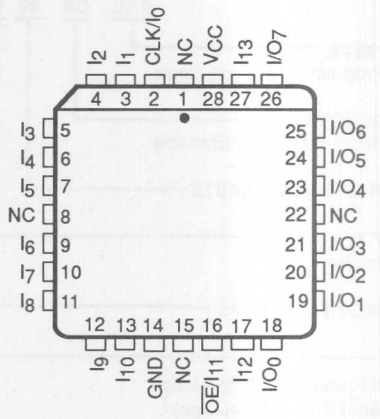
CONNECTION DIAGRAMS
(Top View)

SKINNYDIP



16491B-2

PLCC/LCC



16491B-3

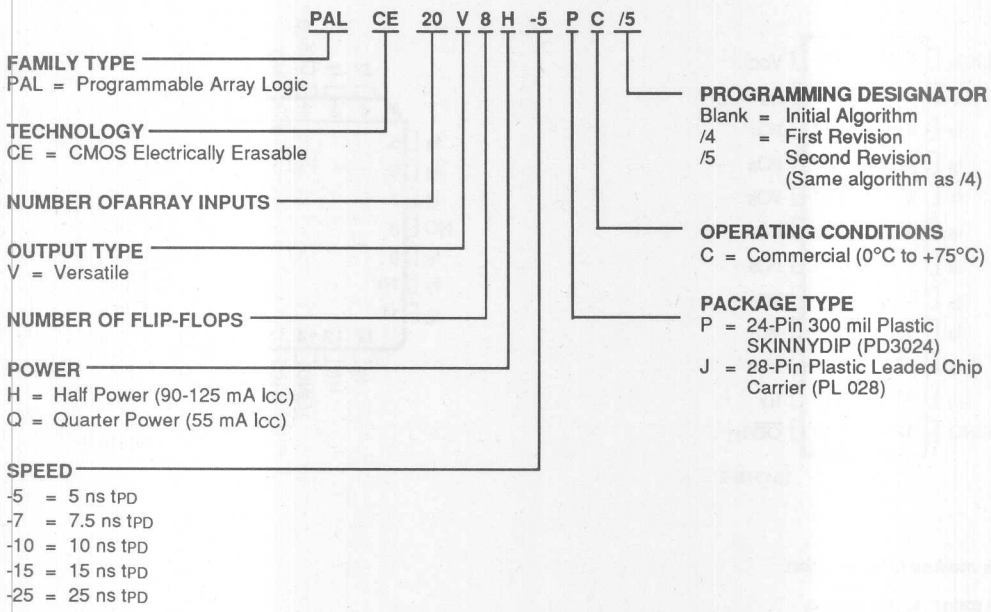
Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
$\overline{OE}$ = Output Enable
Vcc = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE20V8H-5	JC	/5
PALCE20V8H-7	PC, JC	
PALCE20V8H-10		Blank, /4
PALCE20V8Q-10		/5
PALCE20V8H-15		Blank, /4
PALCE20V8Q-15		
PALCE20V8H-25		
PALCE20V8Q-25		

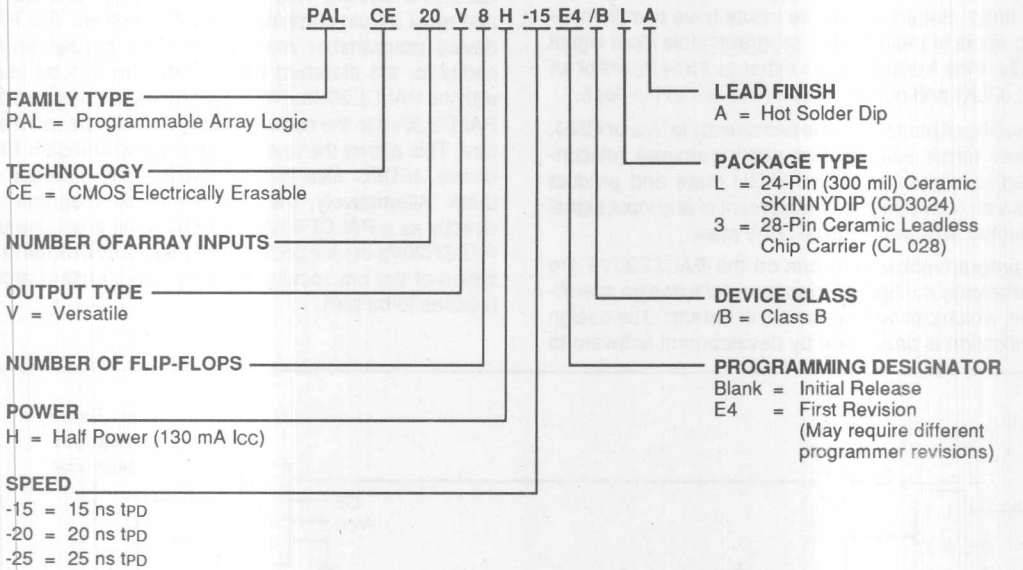
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE20V8H-15	E4	/BLA, /B3A
PALCE20V8H-20	Blank, E4	
PALCE20V8H-25		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

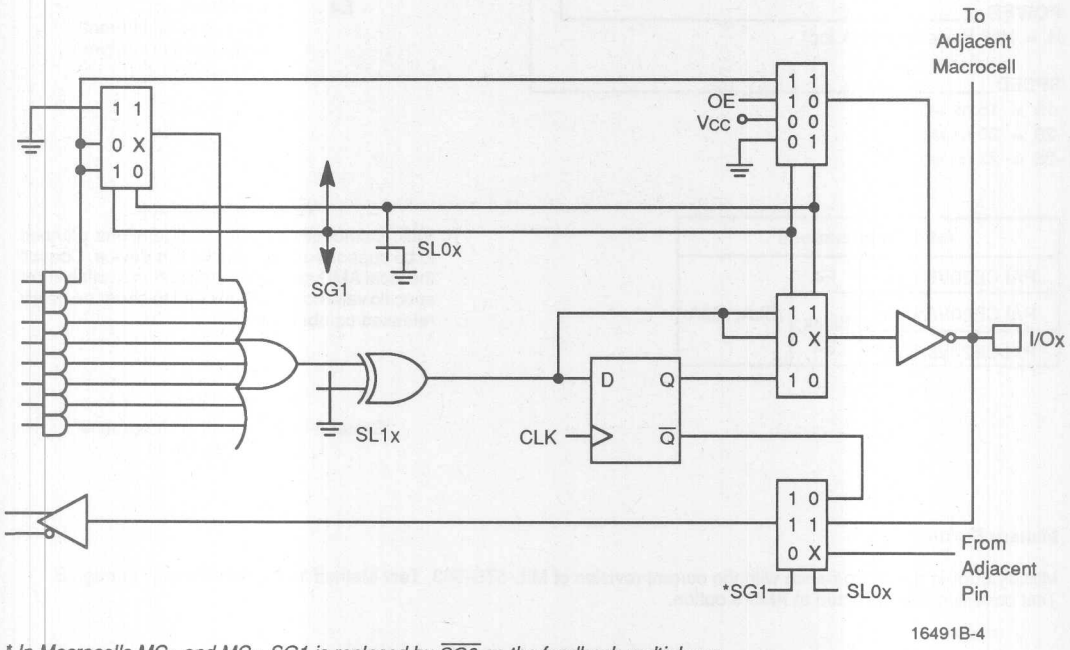
FUNCTIONAL DESCRIPTION

The PALCE20V8 is a universal PAL device. It has eight independently configurable macrocells ($MC_0..MC_7$). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 13 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE20V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE20V8. First, it can be programmed as an emulated PAL device. This includes the PAL20R8 series and most 24-pin combinatorial PAL devices. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE20V8. The programmer will program the PALCE20V8 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE20V8. Here the user must use the PALCE20V8 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



** In Macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

Figure 1. PALCE20V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled. A macrocell configured as a dedicated input derives the input signal from an adjacent I/O.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE20V8 will emulate a PAL20R8 family or a combinatorial device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE20V8 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins may be available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE20V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 18(21) and 19(23). Pins 18(21) and 19(23) do not use feedback in this mode.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is an adjacent I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0,SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

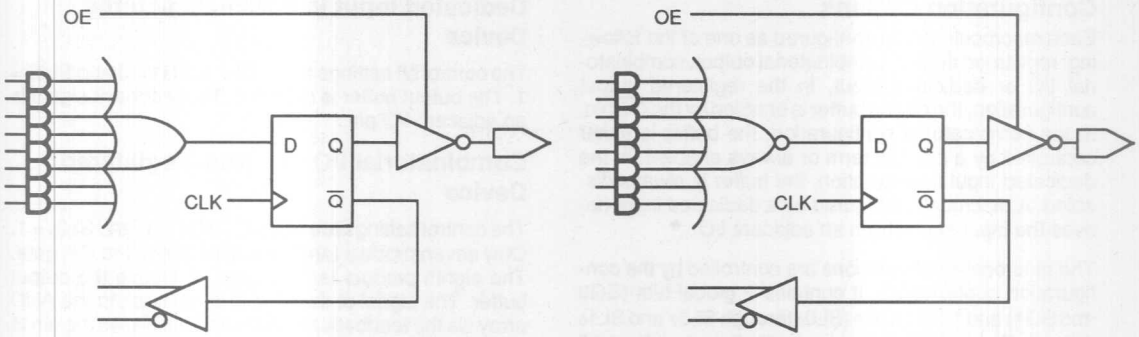
Table 1. Macrocell Configurations

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
Device has registers				
0	1	0	Registered Output	PAL20R8, 20R6, 20R4
0	1	1	Combinatorial I/O	PAL20R6, 20R4
Device has no registers				
1	0	0	Combinatorial Output	PAL20L2, 18L4,16L6,14L8
1	0	1	Dedicated Input	PAL20L2,18L4, 16L6
1	1	1	Combinatorial I/O	PAL20L8

Programmable Output Polarity

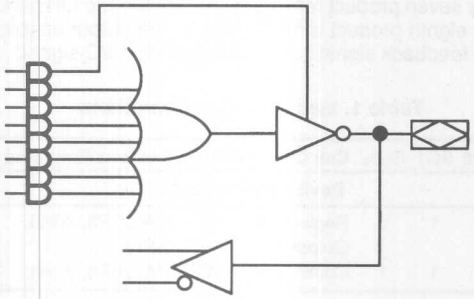
The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is made through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is a 0 and active low if $SL1_x$ is a 1.

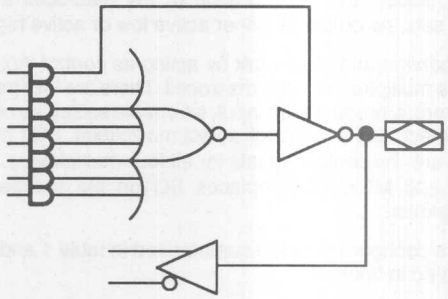


Registered Active Low

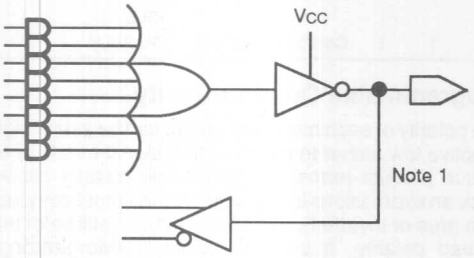
Registered Active High



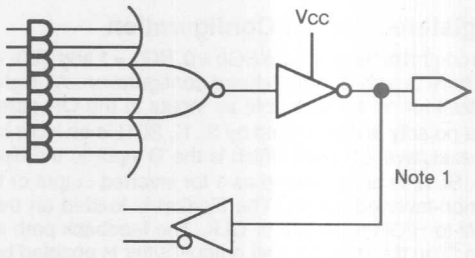
Combinatorial I/O Active Low



Combinatorial I/O Active High



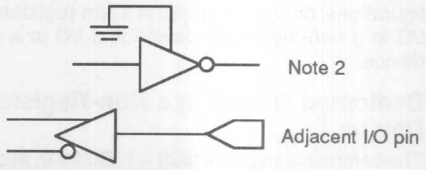
Combinatorial Output Active Low



Combinatorial Output Active High

Notes:

1. *Feedback is not available on pins 18 (21) and 19 (23) in the combinatorial output mode.*
2. *This macrocell configuration is not available on pins 18 (21) and 19 (23).*



Dedicated Input

16491B-5

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE20V8 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE20V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE20V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE20V8. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE20V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

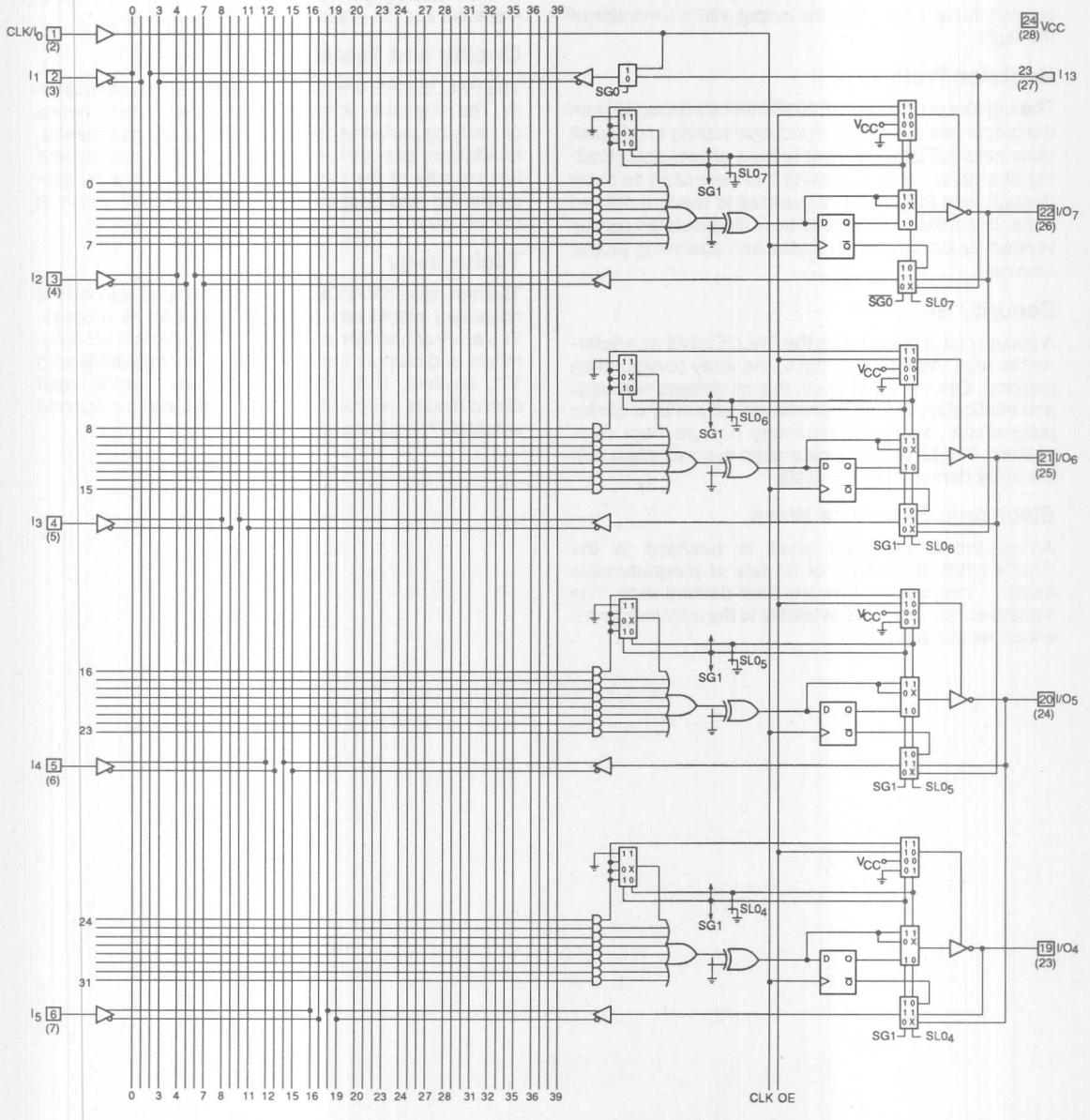
The PALCE20V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming and post-programming functional yields in the industry.

Technology

The high-speed PALCE20V8H is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

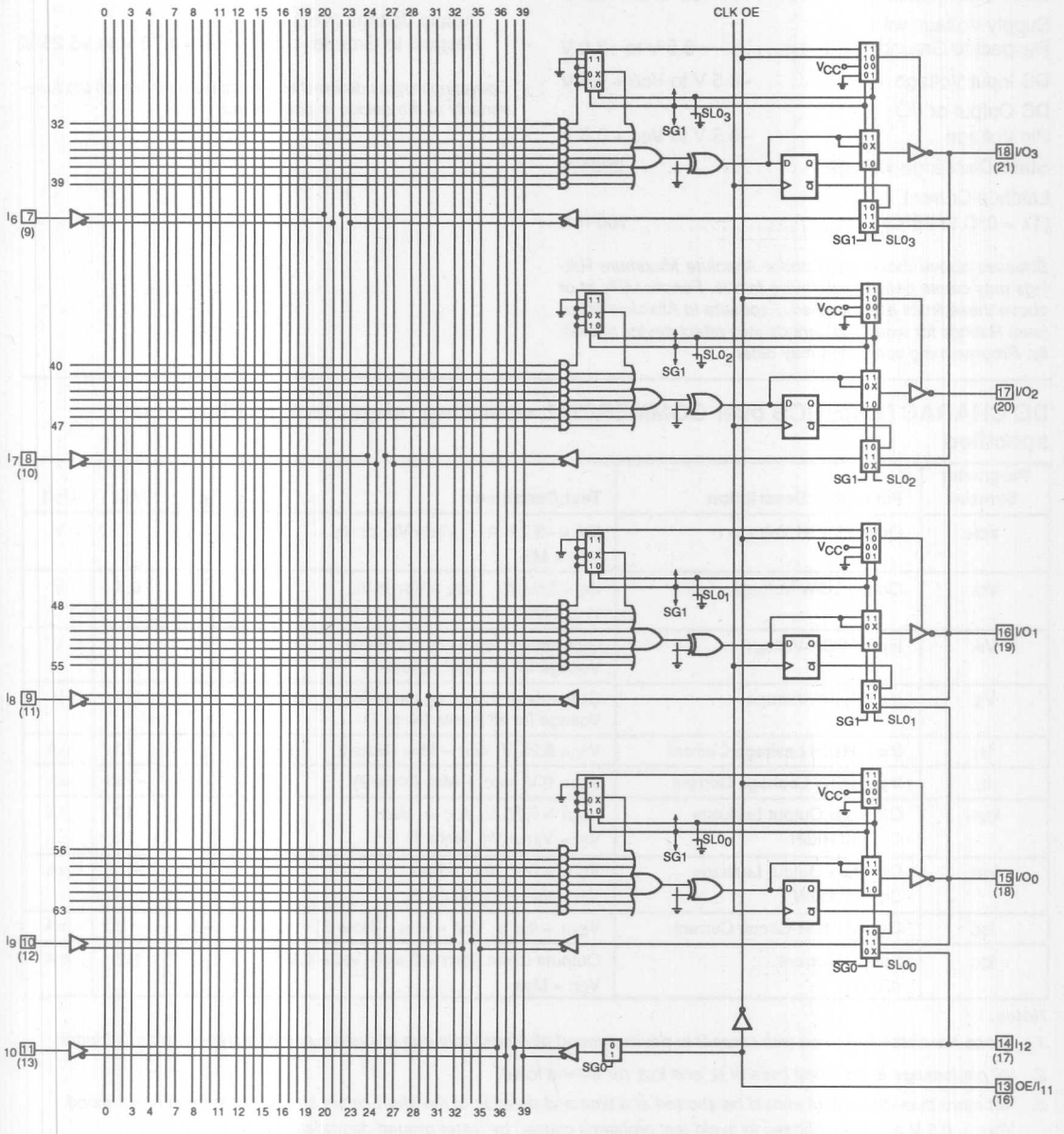
LOGIC DIAGRAM

SKINNYDIP (PLCC and LCC) Pinouts



16491B-6

LOGIC DIAGRAM (continued)
SKINNYDIP (PLCC and LCC) Pinouts



16491B-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Static)	Outputs Open (I_{OUT} = 0 mA), V_{IN} = 0 V V_{CC} = Max		125	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 5)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	5	ns
t_S	Setup Time from Input or Feedback to Clock			3		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		3		ns
t_{WH}		HIGH		3		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT})		166		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	166		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			2	6	ns
t_{ER}	Input to Output Disable Using Product Term Control			2	5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output		8 Outputs Switching	3	7.5	ns
			1 Output Switching	3	7	ns
t_S	Setup Time from Input or Feedback to Clock			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	100		MHz
		Internal Feedback (f_{CNT})		125		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	6	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	9	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})		71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	PRELIMINARY Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			PRELIMINARY Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})		71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback (f_{CNT})		50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_C = –55°C to +125°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C) ..... –55°C to +125°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Note:

1. *Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.*

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = 25°C (Note 5)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		130	mA

Notes:

2. *For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min (Note 5)	-15 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	15	ns
t_S	Setup Time from Input or Feedback to Clock			12		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	12	ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	41.6		MHz
		Internal Feedback (f_{CNT})		45.5		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	50.0		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			3	15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			3	15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)			3	15	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_C = –55°C to +125°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C) ..... –55°C to +125°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Note:

1. *Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.*

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = 25°C (Note 5)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		130	mA

Notes:

2. *For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

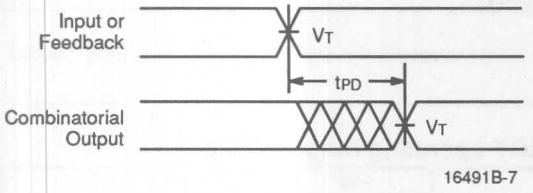
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			–20 Min	–20 Max	–25 Min	–25 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input or Feedback to Clock			15		20		ns
t_H	Hold Time (Note 5)			0		0		ns
t_{CO}	Clock to Output				15		20	ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	33.3		25		MHz
		Internal Feedback (f_{CNT})		35.7		26.3		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	41.7		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				18		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				18		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				20		25	ns

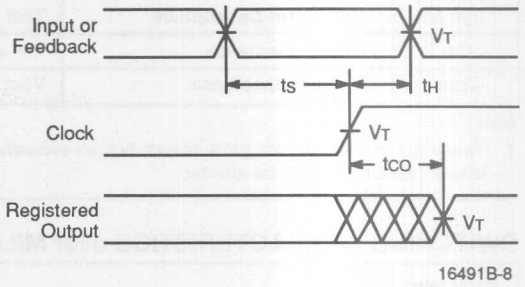
Notes:

2. *See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

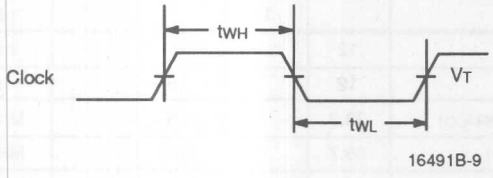
SWITCHING WAVEFORMS



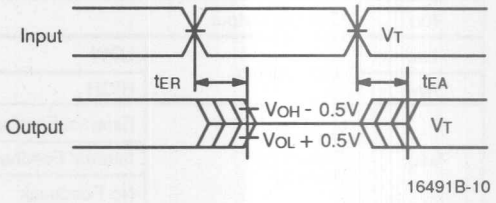
Combinatorial Output



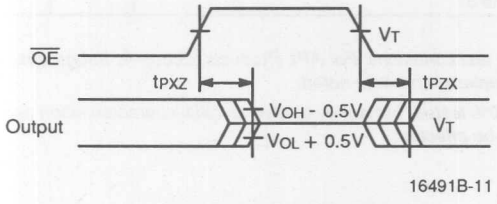
Registered Output



Clock Width



Input to Output Disable/Enable



OE to Output Disable/Enable

Notes:

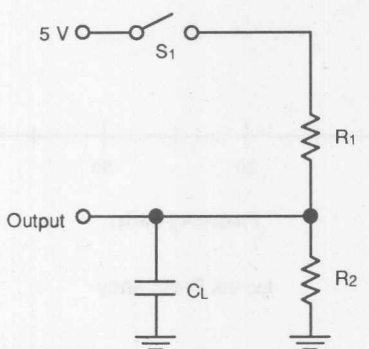
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

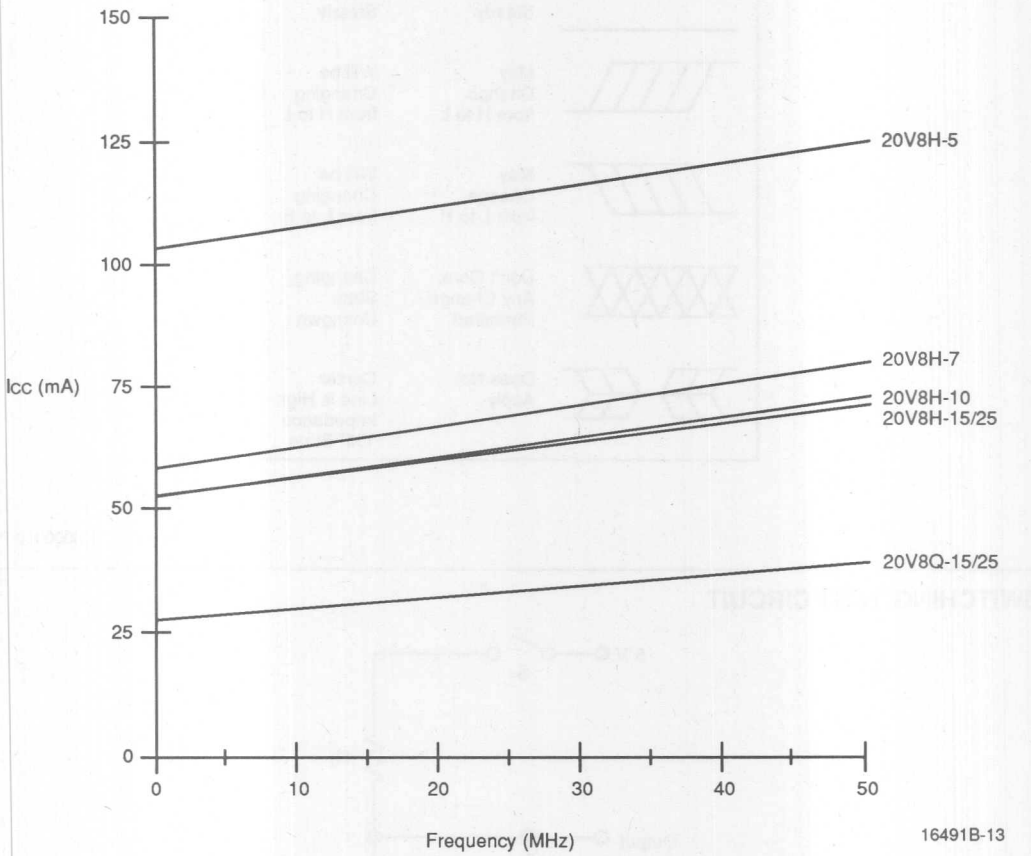


16491B-12

Switching Test Circuit

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Military R_1	Military R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω H-5: 200 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	50 pF					1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5.0 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

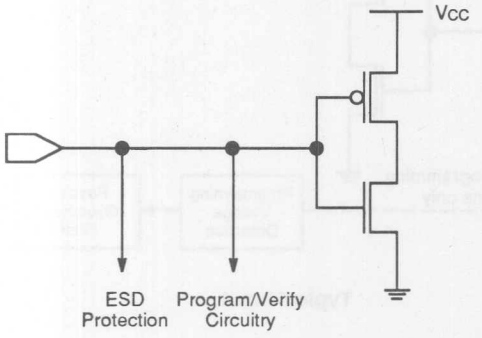
ENDURANCE CHARACTERISTICS

The PALCE20V8 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

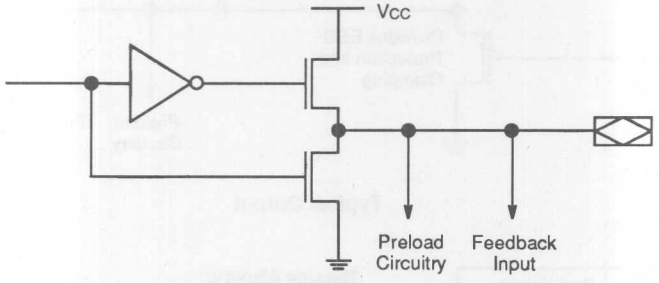
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

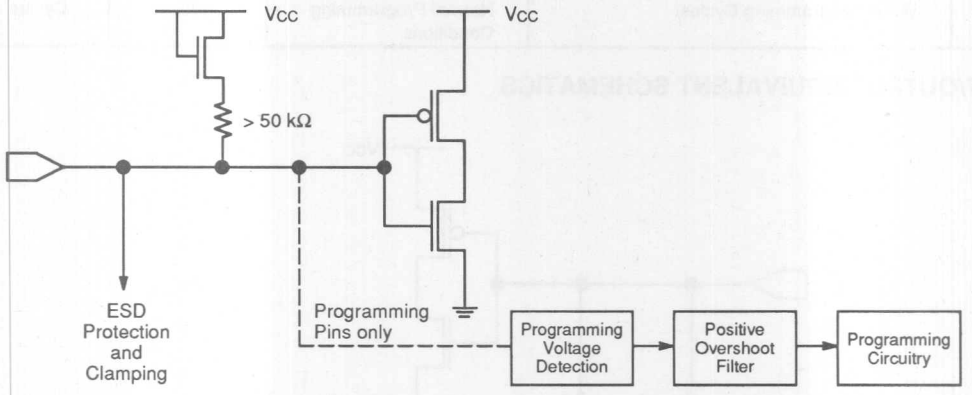
16491B-14

ROBUSTNESS FEATURES

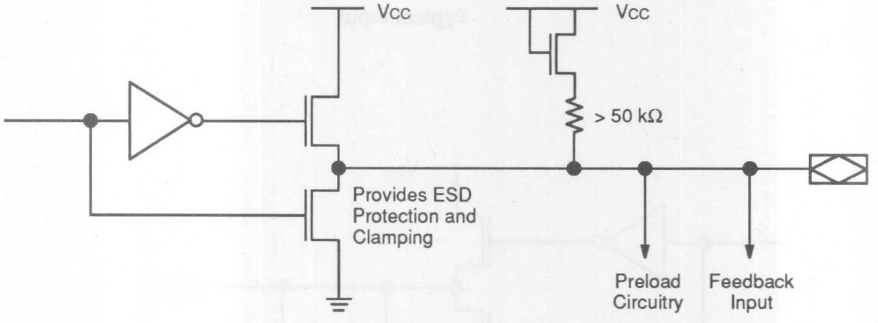
The PALCE20V8X-X/5 have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 versions.

Selected /4 devices are also being retrofitted with these robustness features. See the chart below for device listings.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSION AND SELECTED /4 VERSIONS*



Typical Input



Typical Output

16491B-15

*

Device	Rev Letter
PALCE20V8H-10	K
PALCE20V8H-15	K, J
PALCE20V8Q-15	J
PALCE20V8H-25	J
PALCE20V8Q-25	J

Topside Marking:

AMD CMOS PLD's are marked on top of the package in the following manner:

PALCEXXXX
Datecode (3 numbers) Lot ID (4 characters)– –(Rev Letter)

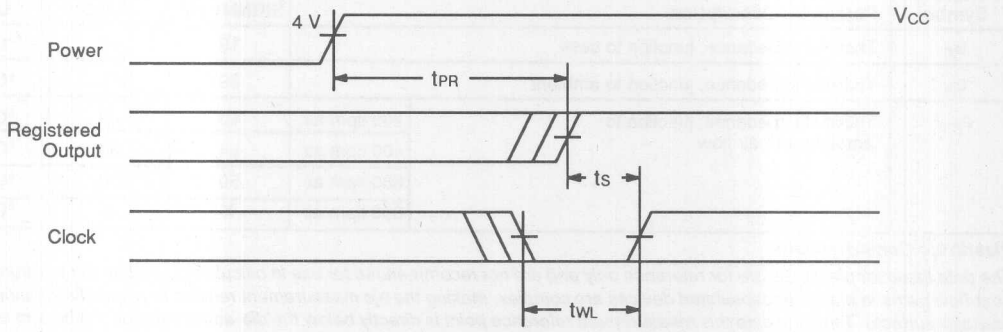
The Lot ID and Rev Letter are separated by two spaces.

POWER-UP RESET

The PALCE20V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveforms

TYPICAL THERMAL CHARACTERISTICS

/4 Devices (PALCE20V8H-10/4)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. SKINNYDIP	Typ. PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		19	19	°C/W
θ_{ja}	Thermal impedance, junction to ambient		73	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	61	45	°C/W
		400 lfpm air	53	41	°C/W
		600 lfpm air	50	38	°C/W
		800 lfpm air	47	36	°C/W

/5 Devices (PALCE20V8H-7/5)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. SKINNYDIP	Typ. PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		18	16	°C/W
θ_{ja}	Thermal impedance, junction to ambient		69	51	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	60	42	°C/W
		400 lfpm air	54	37	°C/W
		600 lfpm air	50	36	°C/W
		800 lfpm air	X	X	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.


IMPORTANT
NOTES

FINAL | COM'L: -20 IND: -20

PALCE20RA10H-20

24-Pin Asynchronous EE CMOS Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Low power at 90 mA I_{CC}
- As fast as 20 ns maximum propagation delay and 37 MHz f_{MAX} (external)
- Individually programmable asynchronous clock, preset, reset, and enable
- Registered or combinatorial outputs
- Programmable polarity
- Programmable replacement for high-speed CMOS or TTL logic
- TTL-level register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP and 28-pin PLCC packages save space

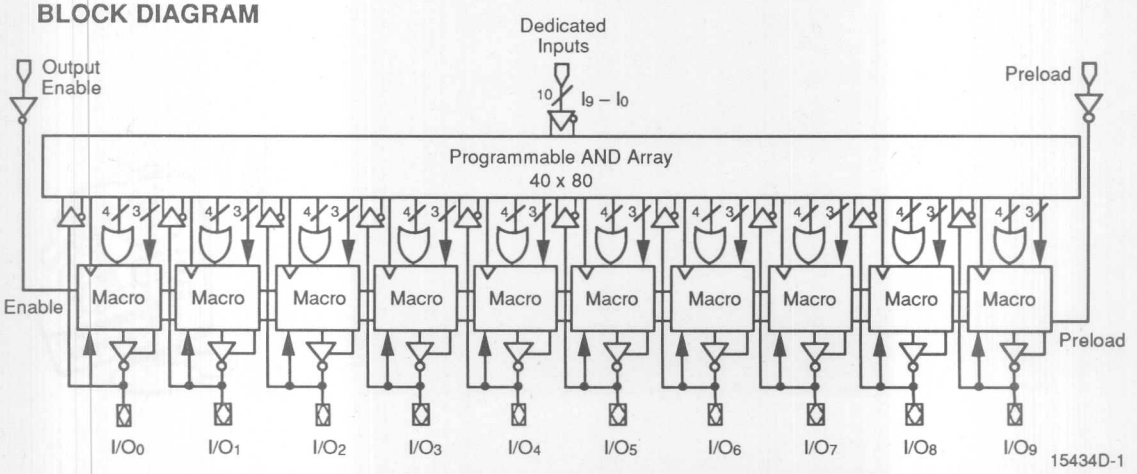
GENERAL DESCRIPTION

The PALCE20RA10 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. The PALCE20RA10 offers asynchronous clocking for each of the ten flip-flops in the device. The ten macrocells feature programmable clock, preset, reset, and enable, and all can operate asynchronously to other macrocells in the same device. The PALCE20RA10 also has flip-flop bypass, allowing any combination of registered and combinatorial outputs.

The PALCE20RA10 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

AMD's FusionPLD program allows PALCE20RA10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software reference guide for certified development systems and the Programmer reference guide for approved programmers.

BLOCK DIAGRAM

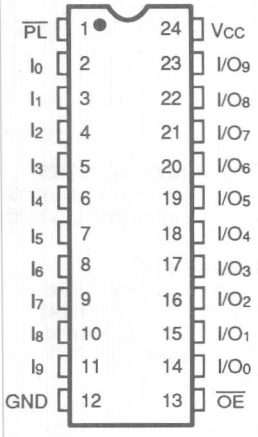


Publication# 15434 Rev. D Amendment/0
Issue Date: June 1993

CONNECTION DIAGRAMS

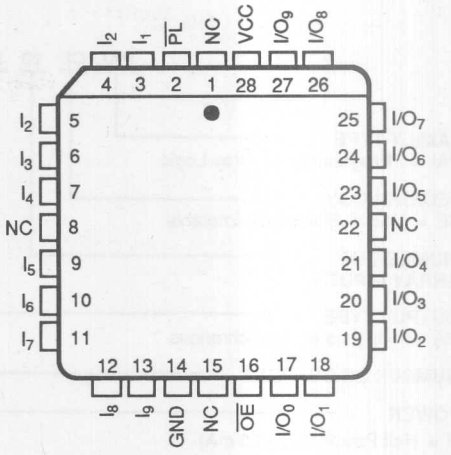
Top View

SKINNYDIP/FLATPACK



15434D-2

PLCC



15434D-3

Note: *Pin 1 is marked for orientation.*

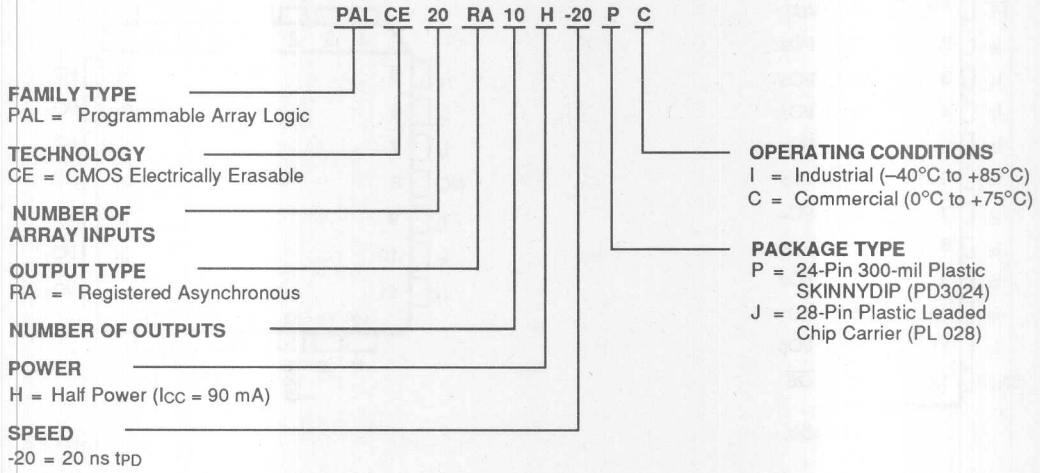
PIN DESIGNATIONS

GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
$\overline{OE}$	=	Output Enable
$\overline{PL}$	=	Preload
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE20RA10H-20	PC, JC, PI, JI

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

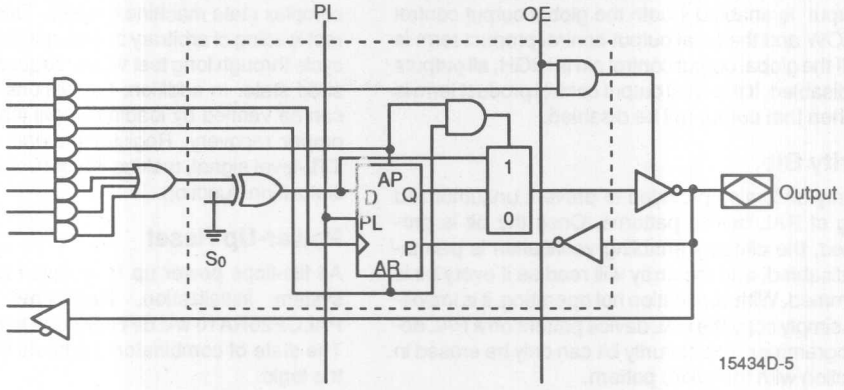


Figure 1. PALCE20RA10 Macrocell

FUNCTIONAL DESCRIPTION

The PALCE20RA10 has ten dedicated input lines and ten programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. Pin 1 serves as global register preload and pin 13 serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PALCE20RA10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes a logic 1 and the output pin will be a logic 0. If the reset product line is HIGH, the Q output of the register becomes a logic 0 and the output pin will be logic 1. The operation of the programmable preset and reset overrides the clock.

Combinatorial/Registered Outputs

If both the preset and reset product lines are HIGH, the flip-flop is bypassed and the output becomes combinatorial. Otherwise, the output is from the register. Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flip-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

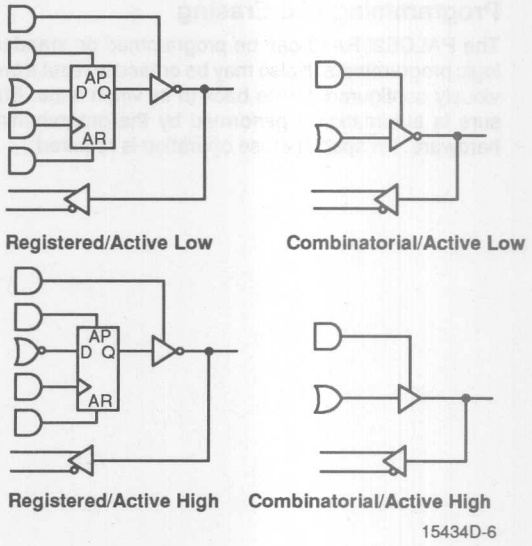


Figure 2. Macrocell Configurations

Three-State Outputs

The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Bit

A security bit is also provided to prevent unauthorized copying of PAL device patterns. Once the bit is programmed, the circuitry enabling verification is permanently disabled, and the array will read as if every bit is programmed. With verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer. The security bit can only be erased in conjunction with the entire pattern.

Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PALCE20RA10 logic diagram. When the output polarity bit is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity bit is unprogrammed, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programming and Erasing

The PALCE20RA10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Register Preload

The register on the PALCE20RA10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transistions from illegal states can be verified by loading illegal states and observing proper recovery. Register preload is controlled by a TTL-level signal, making it a convenient board-level initialization function.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Registered outputs of the PALCE20RA10 will be HIGH due to the output inverter. The state of combinatorial outputs will be a function of the logic.

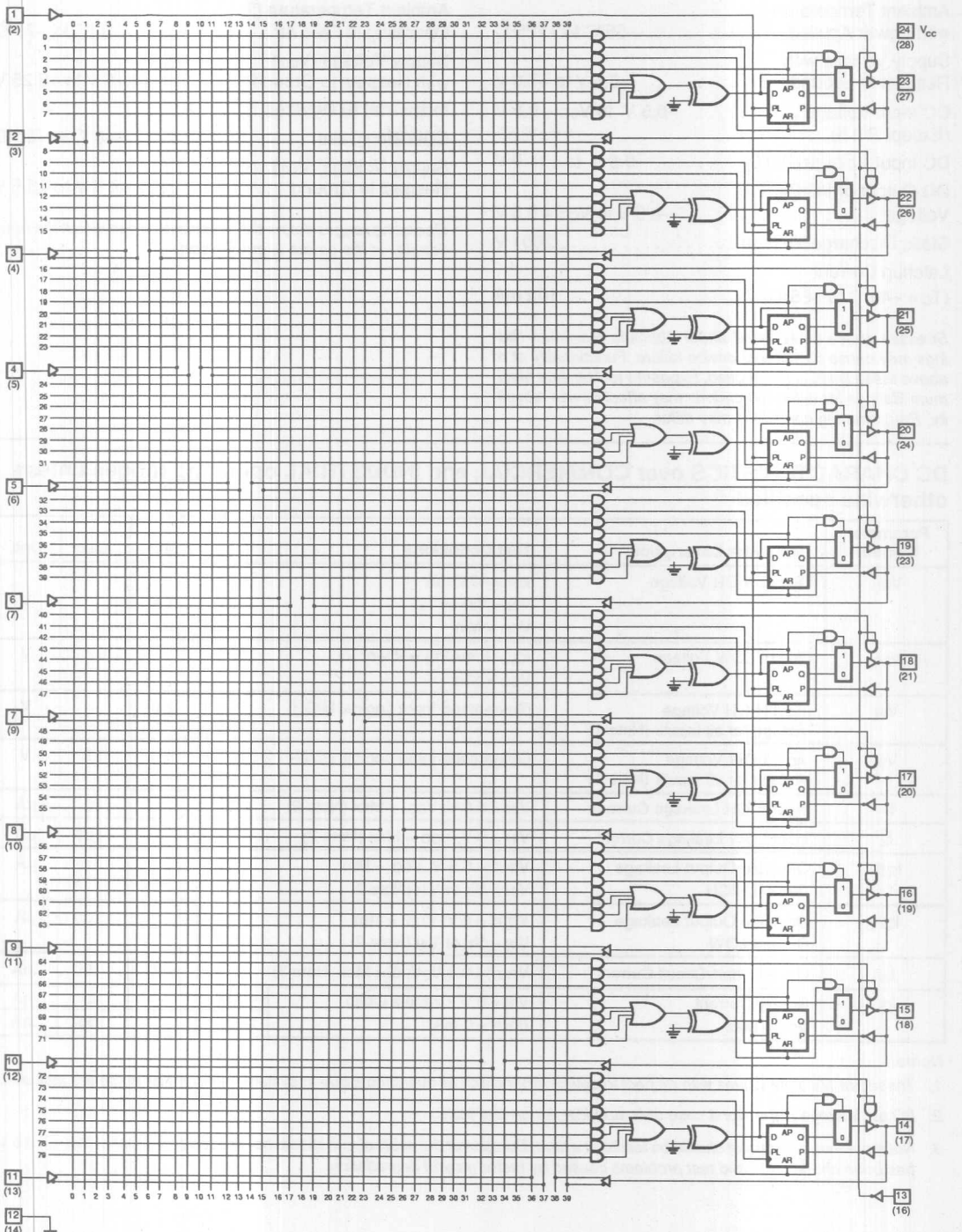
Quality and Testability

The PALCE20RA10 offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE20RA10H-20 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
DIP (PLCC JEDEC) Pinouts



15434D-7

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V (Except Pin 5)

DC Input Voltage (Pin 5) ..... –0.6 V to +11.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_C = –40°C to +85°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mAV_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage Voltage for all Inputs (Note 1)	Guaranteed Input Logical HIGH		2.0		V
V_{IL}	Input LOW Voltage Voltage for all Inputs (Note 1)	Guaranteed Input Logical LOW			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current V_{CC} = Max	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA)	COM'L		90	mA
			IND		130	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	Inputs	V_{IN} = 2.0 V	V_{CC} = 5.0 V	5	pF
		$\overline{OE}$		T_A = +25°C	9	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

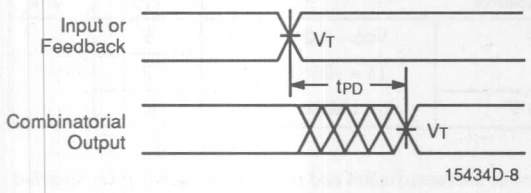
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20 Min (Note 3)	-20 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20	ns
t_S	Setup Time from Input, Feedback or SP to Clock			7		ns
t_H	Hold Time			4		ns
t_{CO}	Clock to Output or Feedback				20	ns
t_{AP}	Asynchronous Preset to Registered Output				20	ns
t_{APW}	Asynchronous Preset Width			12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				12	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				12	ns
t_{WL}	Clock Width	LOW		12		ns
t_{WH}		HIGH		12		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$	37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15	ns
t_{EA}	Input to Output Enable Using Product Term Control				20	ns
t_{ER}	Input to Output Disable Using Product Term Control				20	ns

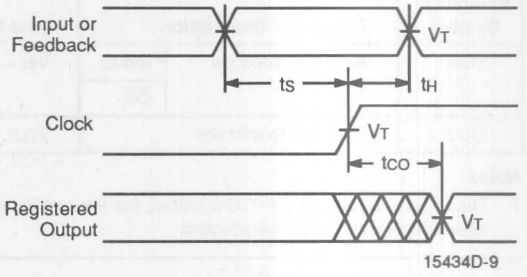
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums are measured under best-case conditions.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*
5. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.*

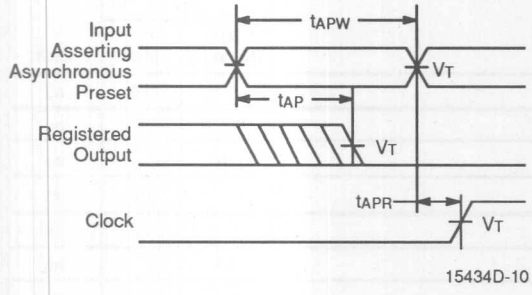
SWITCHING WAVEFORMS



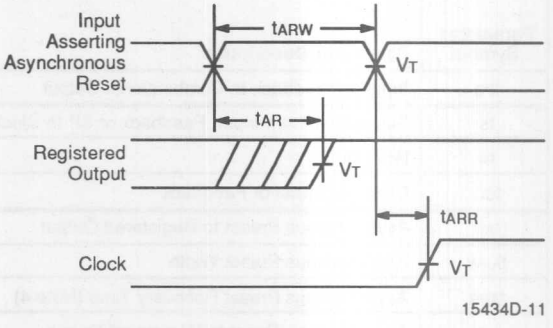
Combinatorial Output



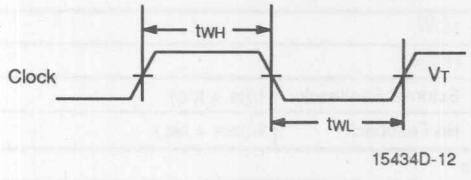
Registered Output



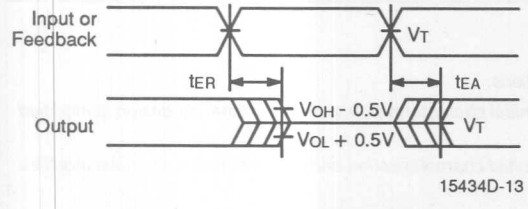
Asynchronous Preset



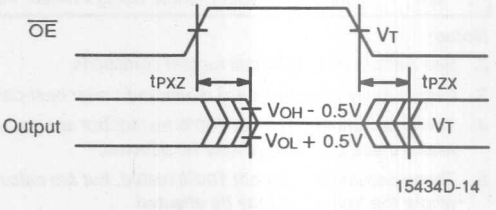
Asynchronous Reset



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

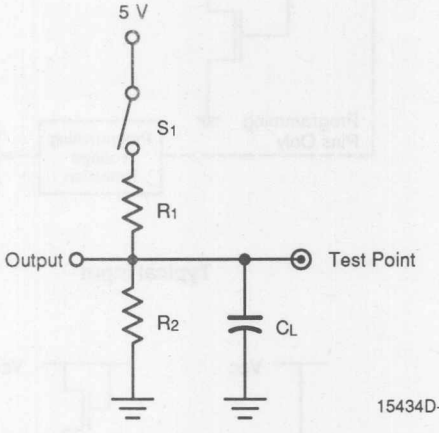
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



15434D-15

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	560 Ω	1.1 kΩ	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

ENDURANCE CHARACTERISTICS

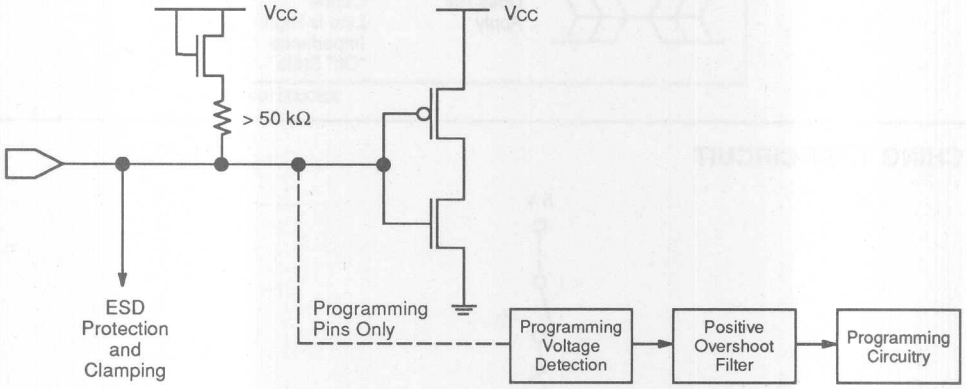
The PALCE20RA10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

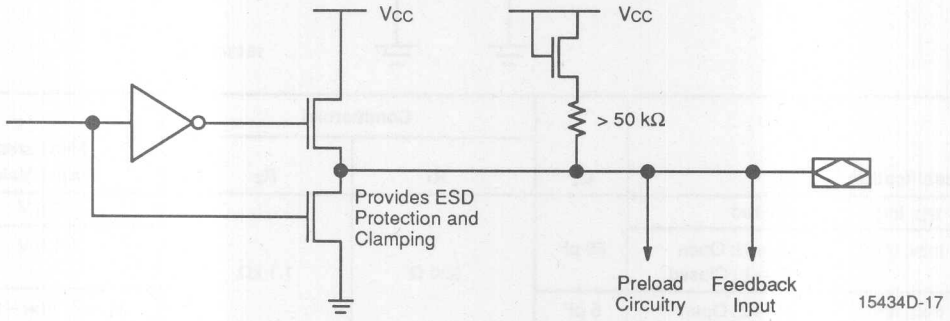
Robustness

The PALCE20RA10H-20 has been designed with some unique features that make it extremely robust, even when operating in high-speed design environments. Pull-up resistors on the inputs and I/Os cause unconnected pins to default to the HIGH state. Input-clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



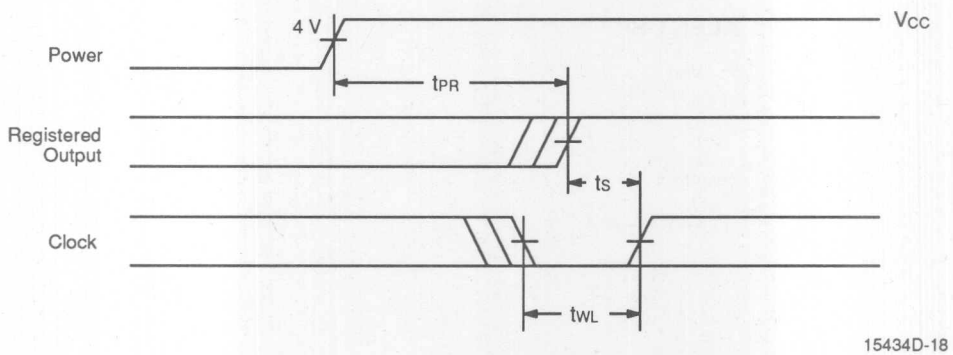
Typical Output

POWER-UP RESET

The PALCE20RA10 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform


IMPORTANT
NOTES

FINAL COM'L

AmPAL22P10B/AL/A

24-Pin Combinatorial TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 15 ns maximum propagation delay**
- **Universal combinatorial architecture**
- **Programmable output polarity**
- **Programmable replacement for high-speed TTL logic**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The AmPAL22P10 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL22P10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

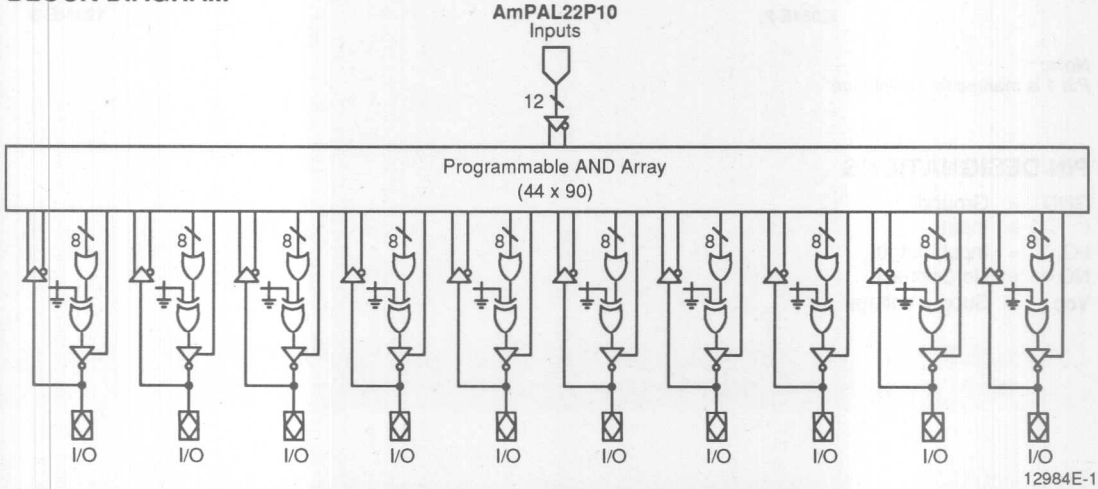
— Variable input/output pin ratio

— Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

BLOCK DIAGRAM



12984E-1

Publication# 12984 Rev. E Amendment/0
Issue Date: January 1992

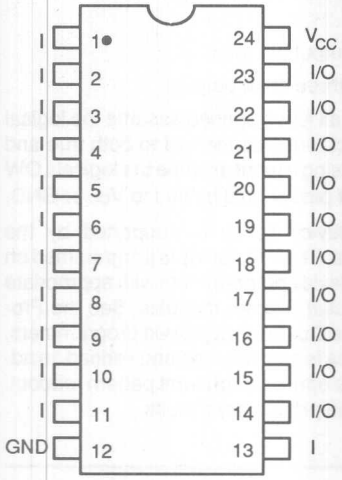
PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max)	I_{CC} mA (Max)	I_{OL} mA (Min)
Very High Speed ("B") Versions	15	210	24
High Speed ("A") Versions	25	210	24
High Speed, Half Power ("AL") Versions	25	105	24

CONNECTION DIAGRAMS

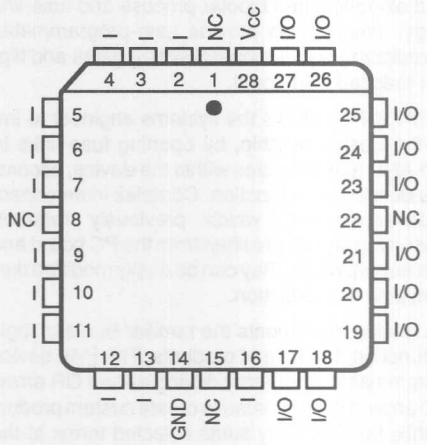
Top View

SKINNYDIP



12984E-2

PLCC



12984E-3

Note:
Pin 1 is marked for orientation

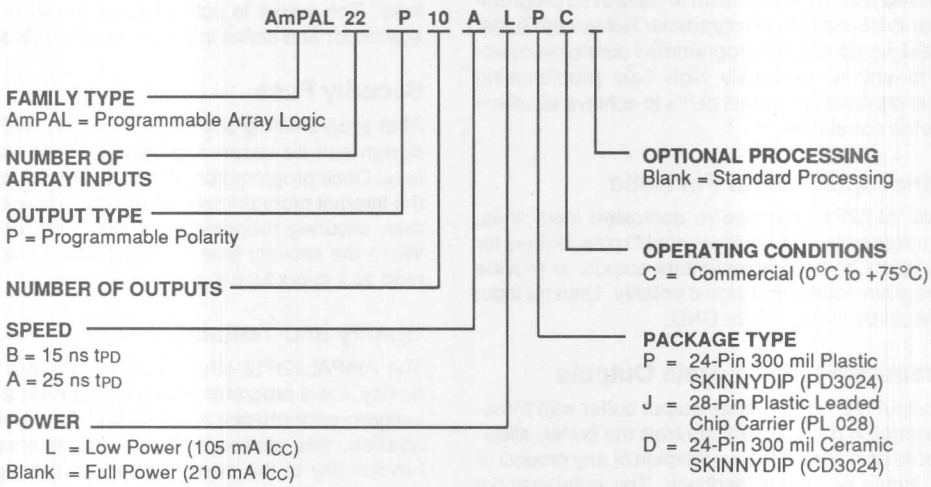
PIN DESIGNATIONS

GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
AmPAL22P10	B, AL, A	PC, JC, DC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: *Marked with AMD logo.*

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL22P10 has twelve dedicated input lines, and all ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL22P10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The AmPAL22P10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

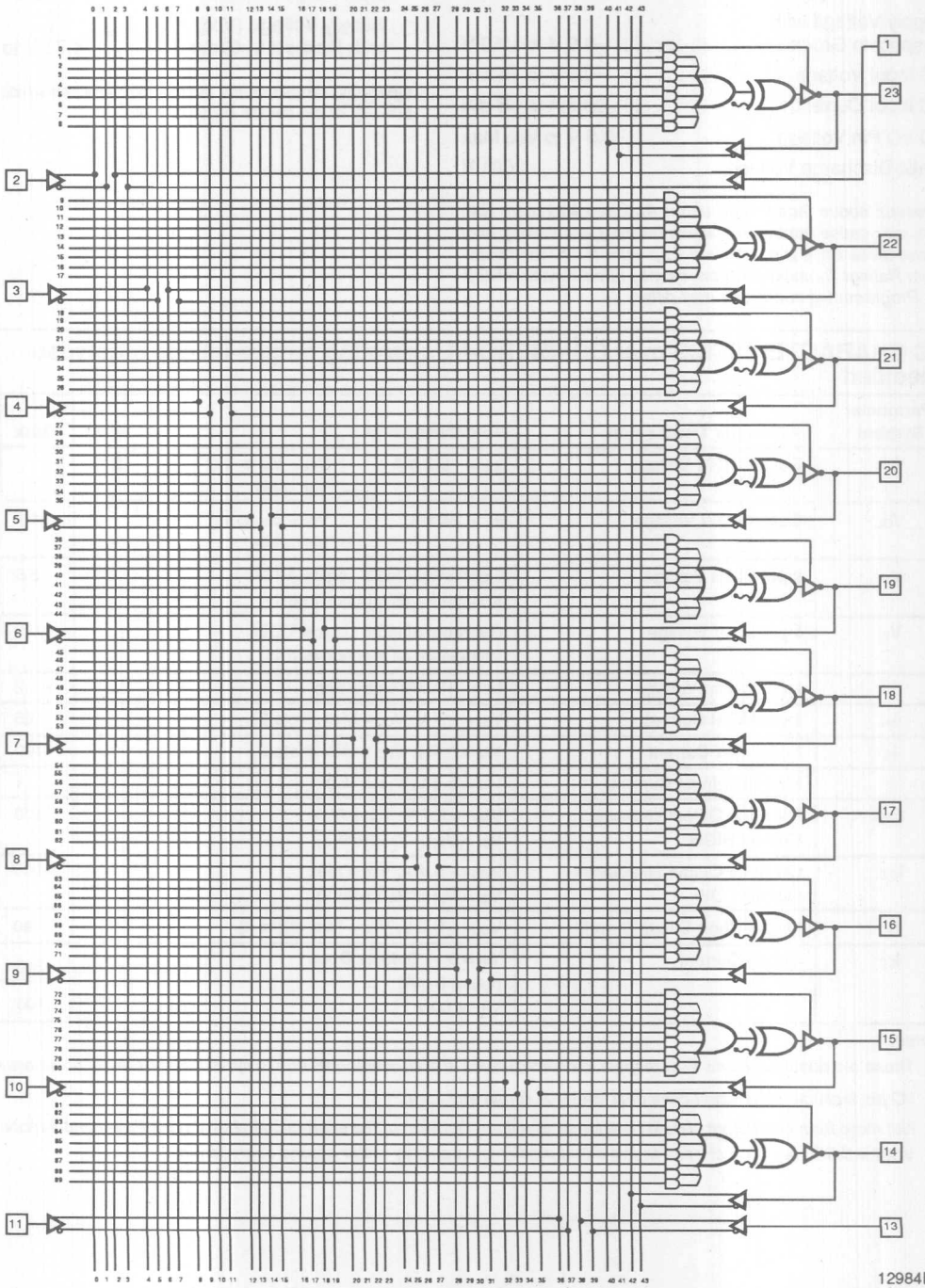
Technology

The AmPAL22P10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM

AmPAL22P10

Inputs (0–43)



12984E-4

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
With Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to +5.5 V

DC Input Current . . . . . –30 mA to +5 mA

DC I/O Pin Voltage . . . . . –0.5 V to V_{CC} Max

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	B, A		210	mA
			AL		105	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

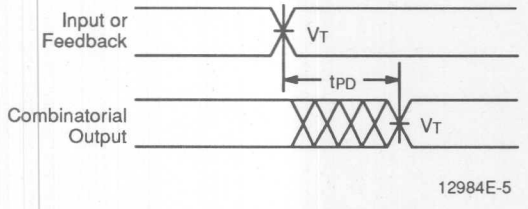
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		Unit
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output		15		25	ns
t_{EA}	Input to Output Enable Using Product Term Control		18		25	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25	ns

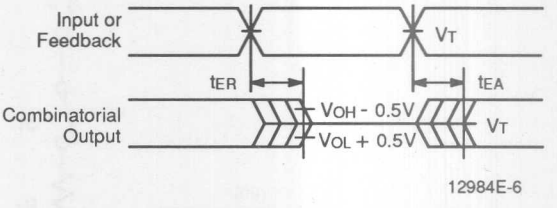
Note:

2. *See Switching Test Circuit for test conditions.*

SWITCHING WAVEFORMS



Combinatorial Output



Input to Output Disable/Enable

Notes:

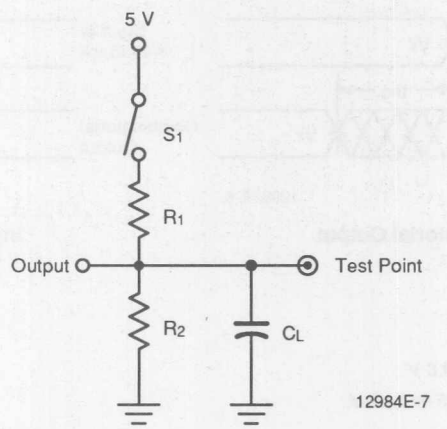
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

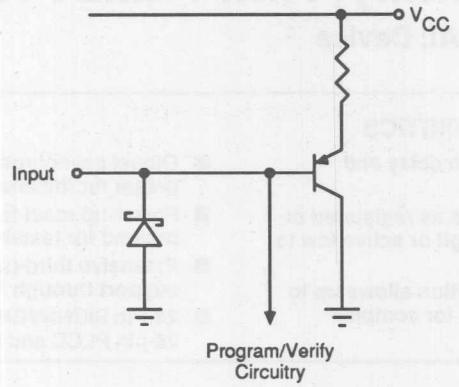
KS000010-PAL

SWITCHING TEST CIRCUIT

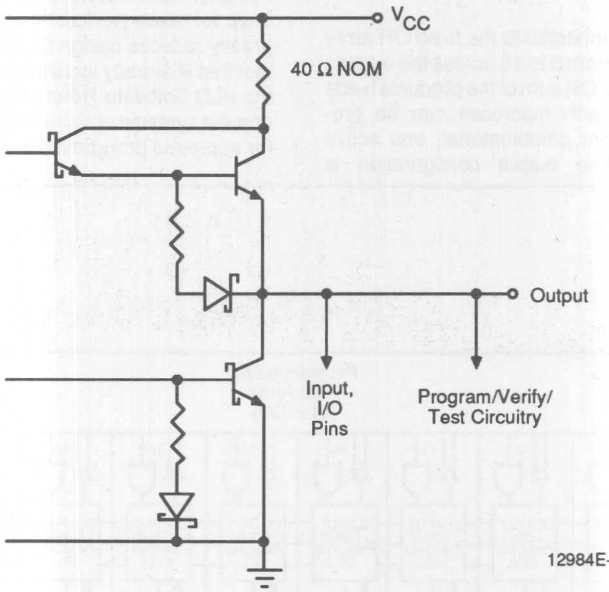


Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input 12984E-8



12984E-9

Typical Output

PAL22V10 Family, AmPAL22V10/A

24-Pin TTL Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns propagation delay and 91 MHz f_{MAX} (external)
- 10 Macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-Pin SKINNYDIP, 24-pin Flatpack and 28-pin PLCC and LCC packages save space

GENERAL DESCRIPTION

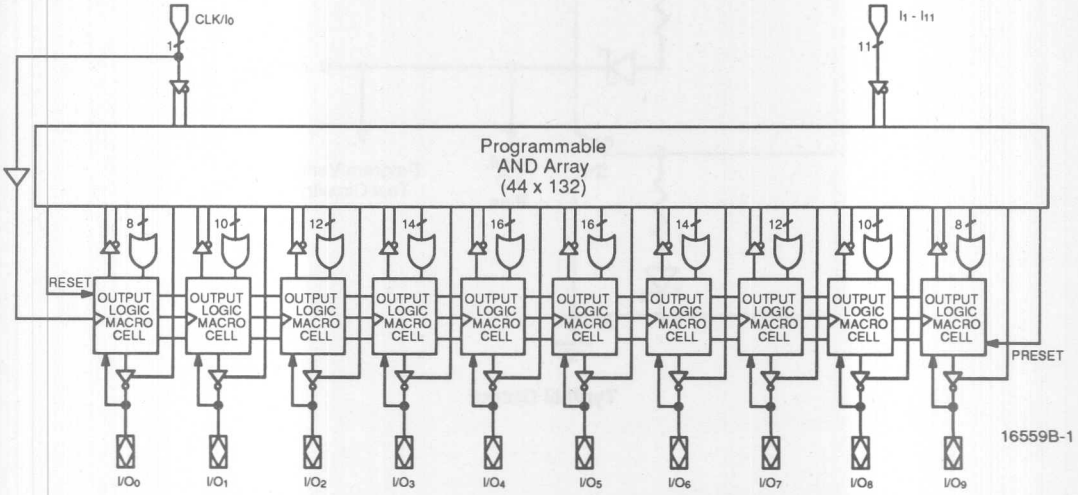
The PAL22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL22V10 device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two fuses controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PAL22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

BLOCK DIAGRAM

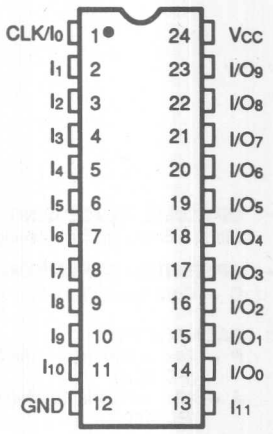


Publication# 16559 Rev. B Amendment /0
Issue Date: June 1993

CONNECTION DIAGRAMS

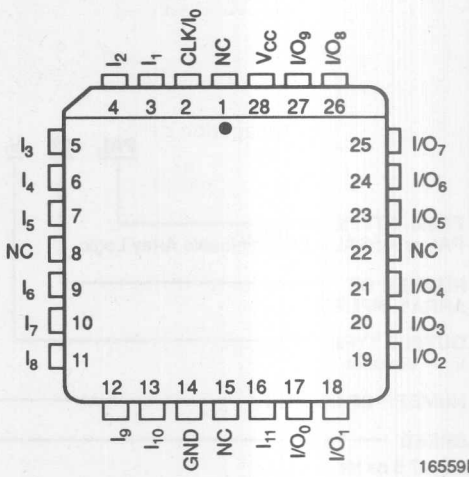
Top View

SKINNYDIP/FLATPACK



16559B-2

PLCC/LCC



16559B-3

Note:
Pin 1 is marked for orientation.

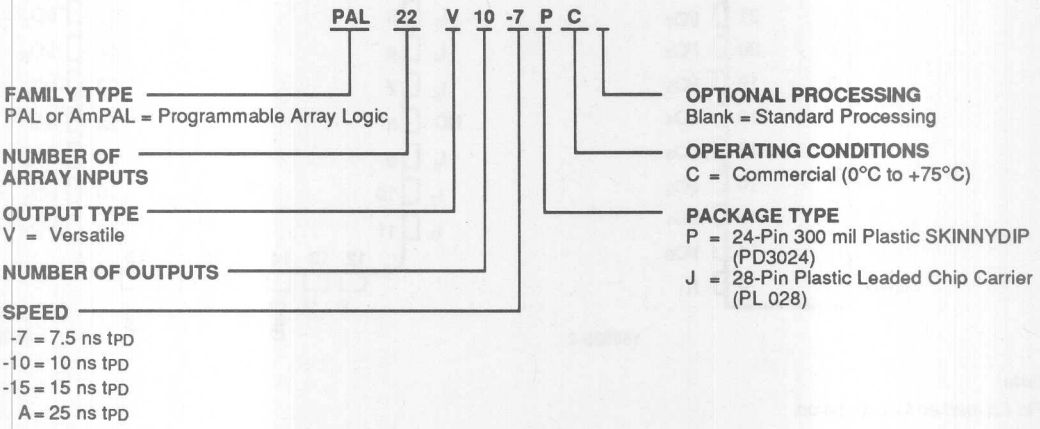
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL22V10-7	PC, JC
PAL22V10-10	
PAL22V10-15	
AmPAL22V10A	

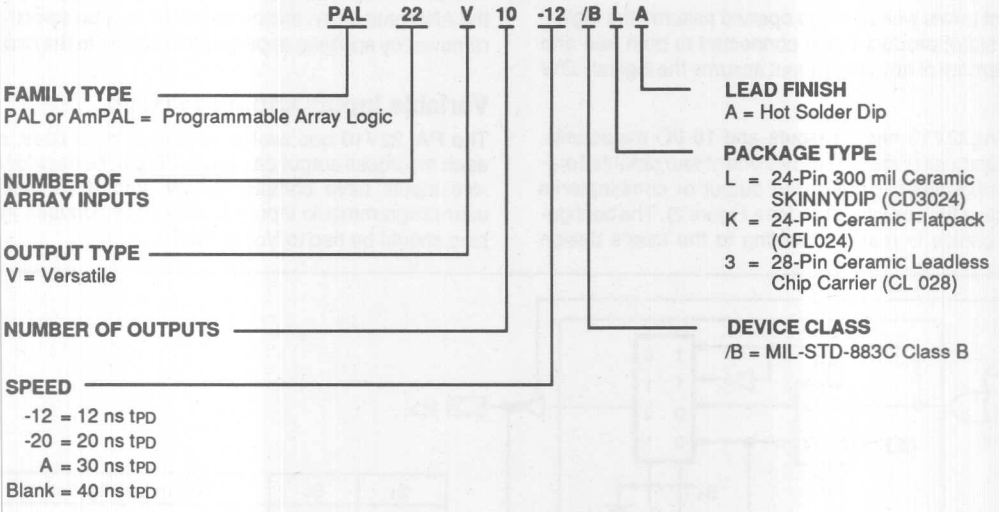
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL22V10-12	/BLA, /BKA, /B3A
PAL22V10-20	
AmPAL22V10A	
AmPAL22V10	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PAL22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

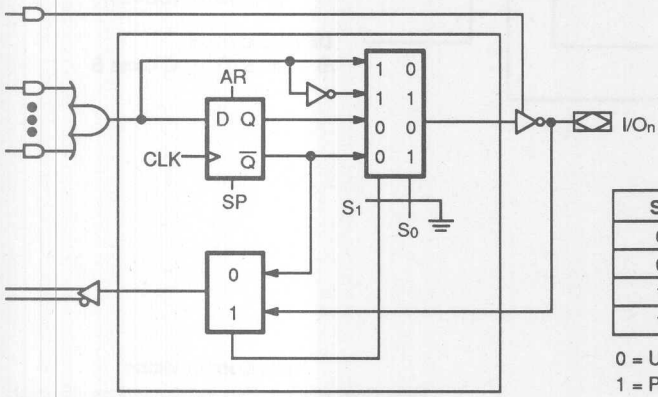
Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PAL22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 – S_1. Multiplexer controls initially are connected to ground (0) through a programmable fuse, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Variable Input/Output Pin Ratio

The PAL22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Unprogrammed fuse
1 = Programmed fuse

16659B-4

Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PAL22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

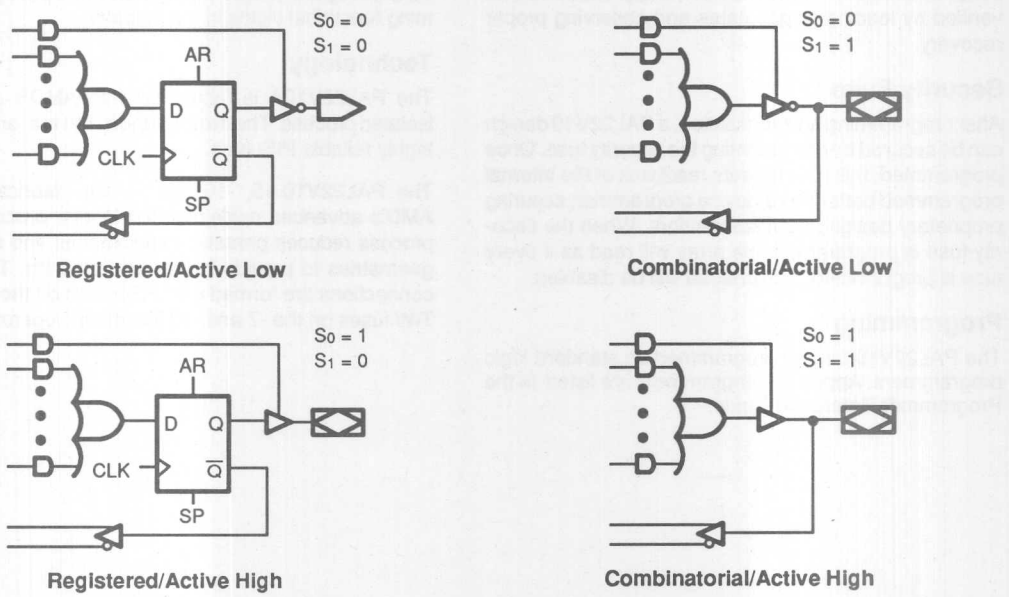


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions.

Preset/Reset

For initialization, the PAL22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL22V10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed, and preload will be disabled.

Programming

The PAL22V10 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

Quality and Testability

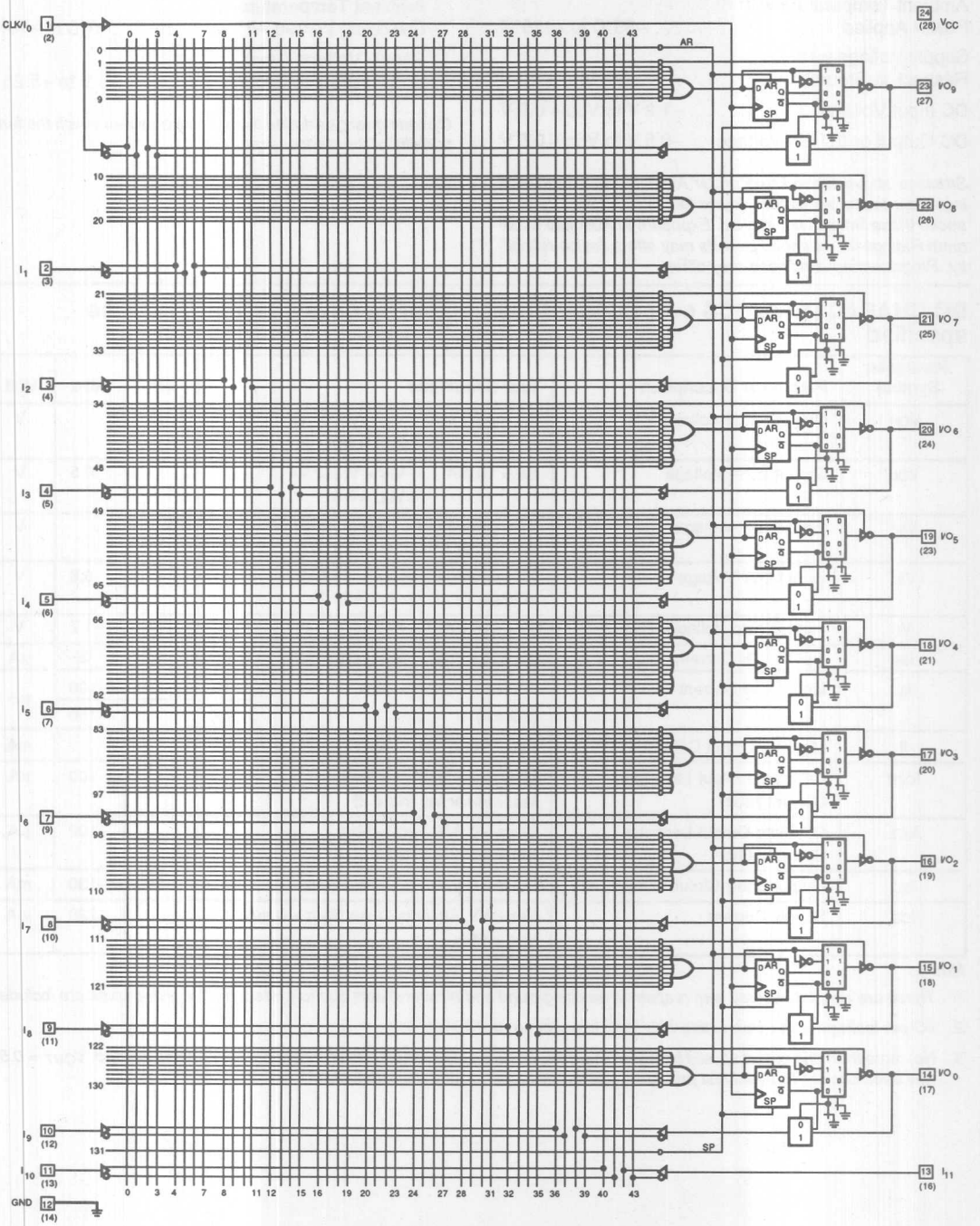
The PAL22V10 offers a very high level of built-in quality. Extra programmable fuses, test words and test columns provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL22V10A is fabricated with AMD's Junction-isolated process. The array connections are formed with highly reliable PtSi fuse.

The PAL22V10-15, -10 and -7 are fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with PtSi fuses on the -15, and TiW fuses on the -7 and -10 for reliable operation.

LOGIC DIAGRAM
SKINNYDIP (PLCC/LCC) Pinouts



16559B-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.2 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)	Input		–100	µA
			CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max			220	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		5	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	7.5	ns
t_S	Setup Time from Input, Feedback or SP to Clock			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	6	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 5)				1	ns
t_{AR}	Asynchronous Reset to Registered Output				12	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			5		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	91		MHz
		Internal Feedback (f_{CNT})		100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				8	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums are measured under best-case conditions.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *Skew is measured with all outputs switching in the same direction.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –1.2 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)	Input		–100	µA
			CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max			180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		5	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	10	ns
t_S	Setup Time from Input, Feedback or SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	7	ns
t_{AR}	Asynchronous Reset to Registered Output				15	ns
t_{ARW}	Asynchronous Reset Width			10		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		5		ns
t_{WH}		HIGH		5		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	71		MHz
		Internal Feedback (f_{CNT})		80		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	100		MHz
t_{EA}	Input to Output Enable Using Product Term Control				11	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums are measured under best-case conditions.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Input Current . . . . . –30 mA to +5 mA

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		6	
				5	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 3)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			15		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		80		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Output delay minimums are measured under best-case conditions.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to +5.5 V

DC Input Current ..... –30 mA to +5 mA

DC Output or I/O Pin Voltage ... –0.5 V to V_{CC} Max

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		180	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		6	
				9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			20		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				30	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			35		ns
t_{SPR}	Synchronous Preset Recovery Time			20		ns
t_{WL}	Clock Width	LOW		15		ns
t_{WH}		HIGH		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	28.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –1.2 V to +7.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to +7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 4)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)	Input		–100	µA
			CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max			200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				12	ns
t_S	Setup Time from Input or Feedback to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			10		ns
t_{SPR}	Synchronous Preset Recovery Time (Note 4)			10		ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)				15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)				12.5	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to +7.0 V

DC Input Current ..... –30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Note:

1. *Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.*

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		200	mA

Notes:

2. *For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		6	
				9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20	ns
t_S	Setup Time from Input or Feedback to Clock			17		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			20		ns
t_{SPR}	Synchronous Preset Recovery Time (Note 4)			20		ns
t_{WL}	Clock Width	LOW		15		ns
t_{WH}		HIGH		15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	31.2		MHz
		Internal Feedback (f_{CNT})		33.3		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)				20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)				20	ns

Notes:

2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to +5.5 V

DC Output or I/O Pin Voltage ... –0.5 V to V_{CC} Max

DC Input Current ..... –30 mA to +5 mA

Output Sink Current ..... 100 mA (Note 6)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air ..... –55°C Min

Operating Case (T_C) Temperature ..... 125°C Max

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.50 V to +5.50 V

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max (Note 4)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 5)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	11	pF
		Others			6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V		9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

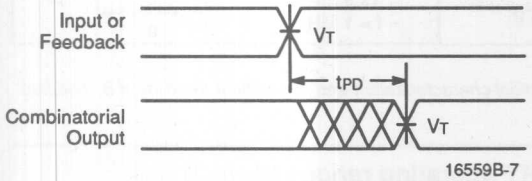
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			A		Std		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				30		40	ns
t_S	Setup Time from Input or Feedback to Clock			25			35	ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				20		25	ns
t_{AR}	Asynchronous Reset to Registered Output				35		45	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			30		40		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			30		40		ns
t_{WL}	Clock Width	LOW		20		30		ns
t_{WH}		HIGH		20		30		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	22		16.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)				30		40	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				30		40	ns

Notes:

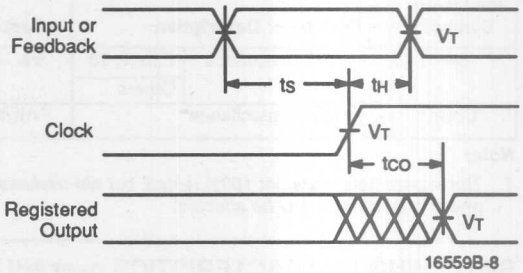
2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.*
4. *These parameters are not 100% tested, but are calculated at initial charzation ond at any time the design is modified where frequency may be affected.*
5. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

SWITCHING WAVEFORMS



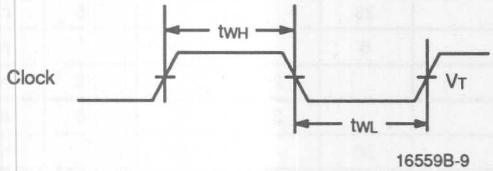
16559B-7

Combinatorial Output



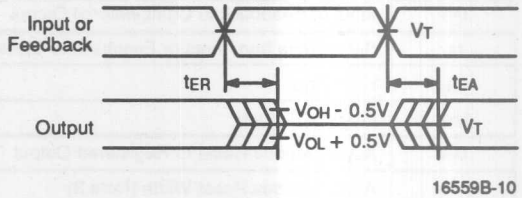
16559B-8

Registered Output



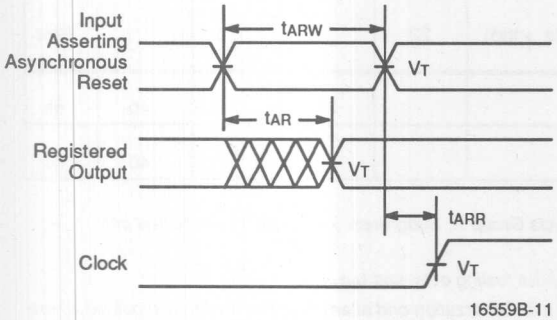
16559B-9

Clock Width



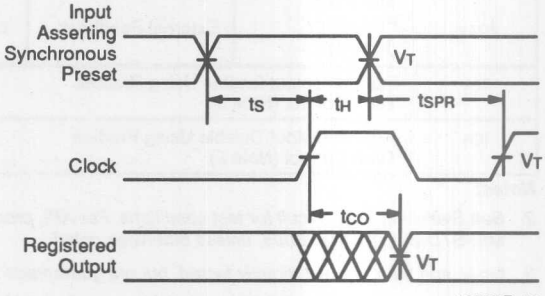
16559B-10

Input to Output Disable/Enable



16559B-11

Asynchronous Reset



16559B-12

Synchronous Preset

Notes:

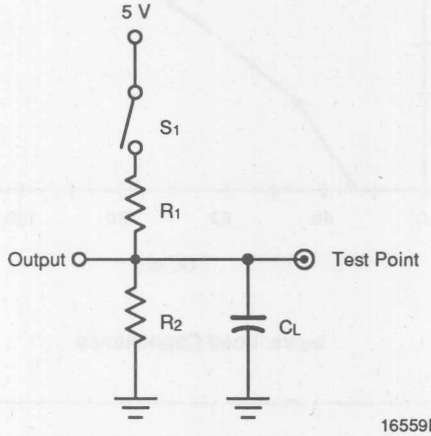
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

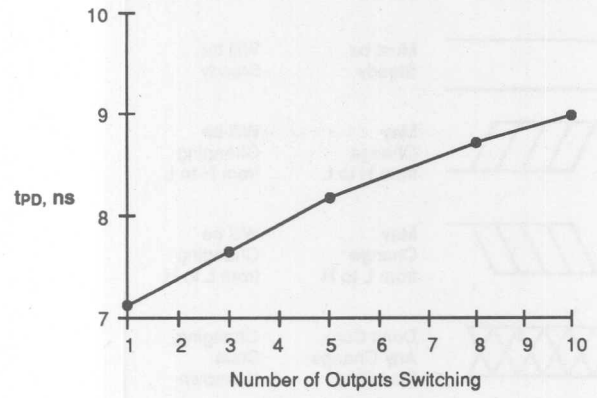


16559B-13

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	All except –7: 390 Ω	390 Ω	750 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF		–7: 300 Ω			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

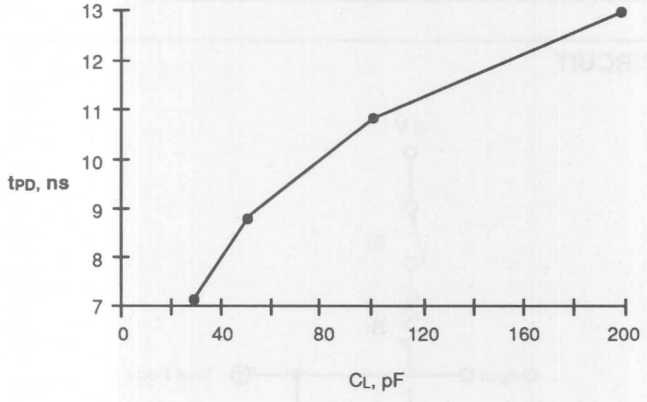
MEASURED SWITCHING CHARACTERISTICS for the PAL22V10-10

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

16559B-14



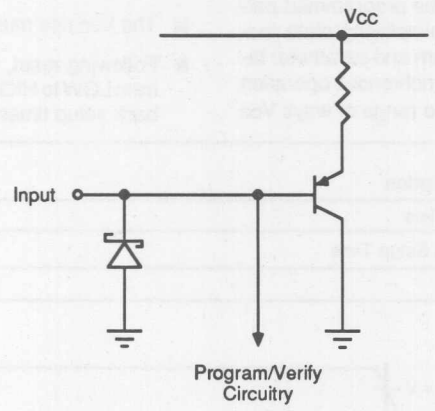
t_{PD} vs. Load Capacitance

16559B-15

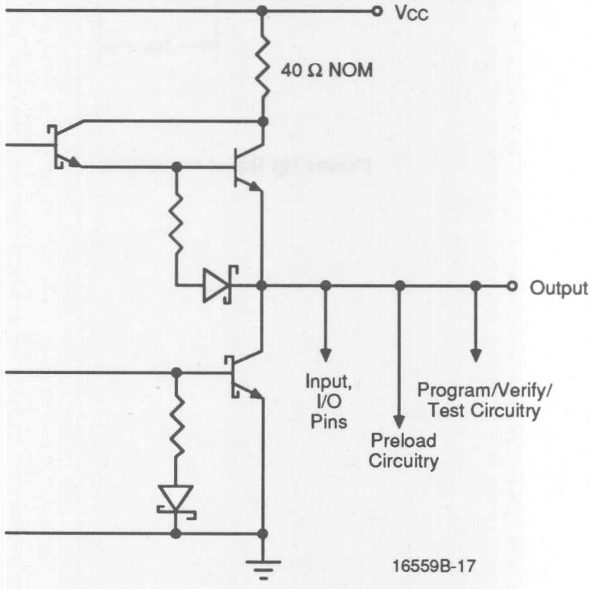
Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.*

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



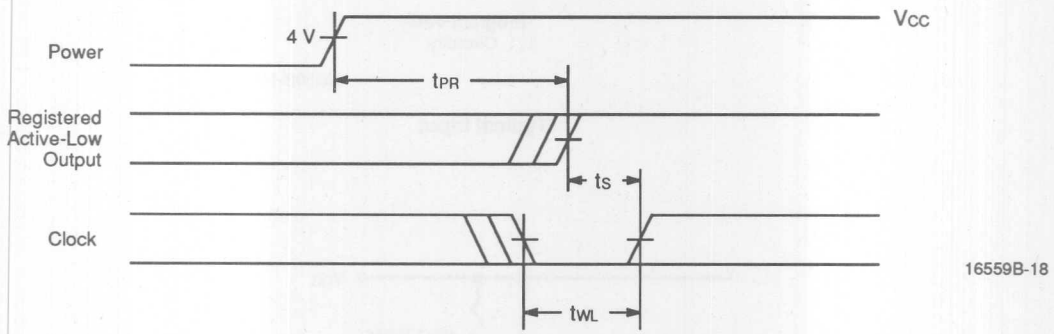
Typical Output

POWER-UP RESET

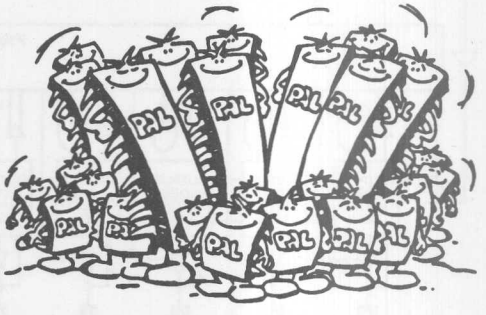
The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The Vcc rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform


PAL
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PALCE22V10 Family

24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 5 ns propagation delay and 142.8 MHz f_{MAX} (external)
- Low-power EE CMOS
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP, 24-pin SOIC, 24-pin Flat-pack and 28-pin PLCC and LCC packages save space
- 5 ns and 7.5 ns versions utilize split leadframes for improved performance

GENERAL DESCRIPTION

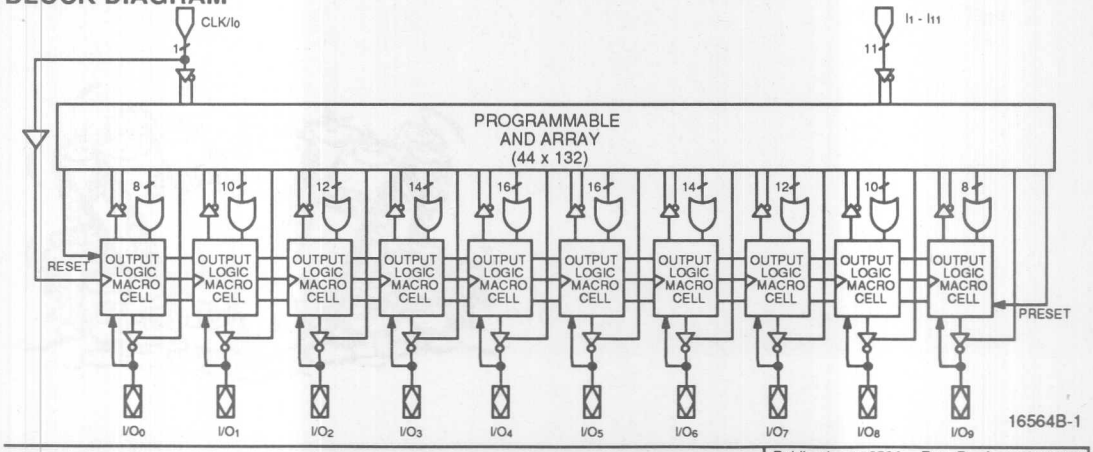
The PALCE22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

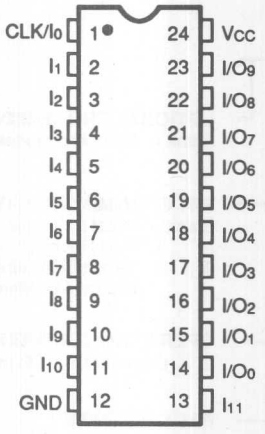
BLOCK DIAGRAM



Publication# 16564 Rev. B Amendment/0
Issue Date: June 1993

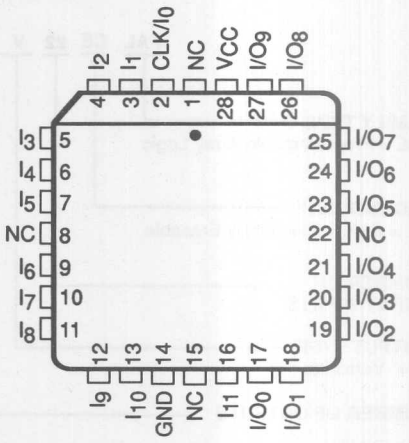
CONNECTION DIAGRAMS
Top View

SKINNYDIP/SOIC/FLATPACK



16564B-2

PLCC/LCC



16564B-3

Note:
Pin 1 is marked for orientation.

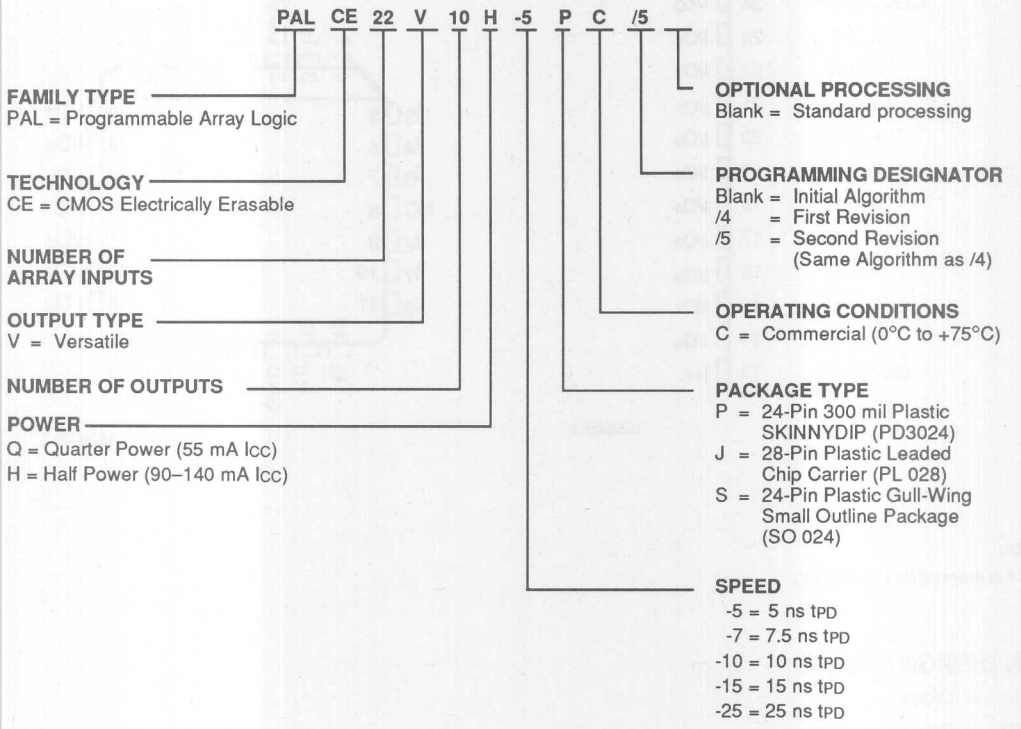
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10-5	JC	/5
PALCE22V10H-7	PC, JC, SC	
PALCE22V10H-10		
PALCE22V10Q-10		
PALCE22V10H-15		Blank, /4
PALCE22V10Q-15	PC, JC	/5
PALCE22V10H-25	PC, JC, SC	Blank, /4
PALCE22V10Q-25	PC, JC	

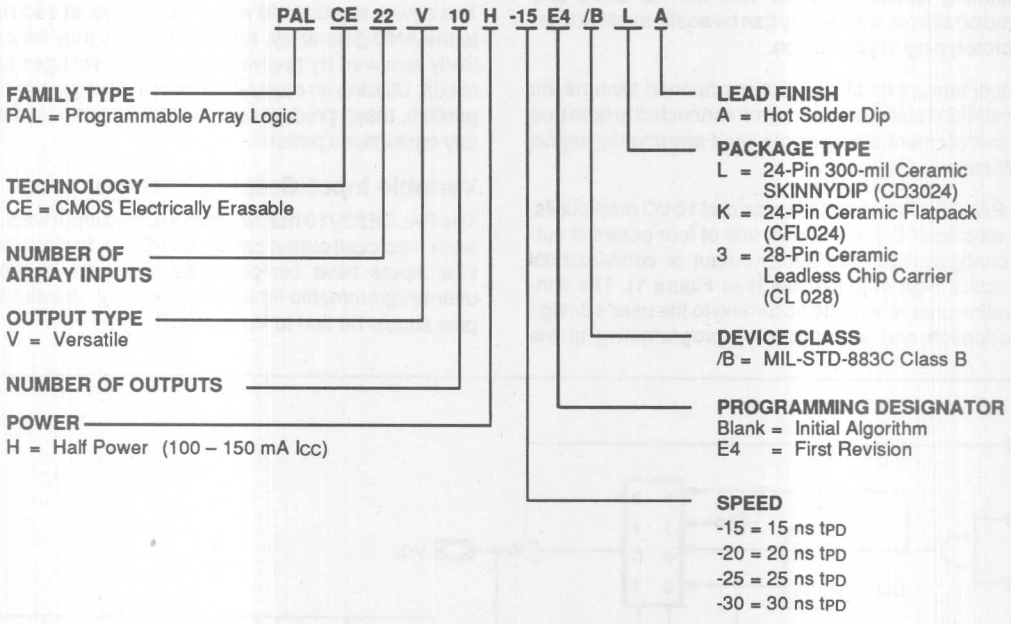
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10H-15	E4	/BLA, /BKA, /B3A
PALCE22V10H-20	Blank, E4	
PALCE22V10H-25		
PALCE22V10H-30		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PALCE22V10 allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

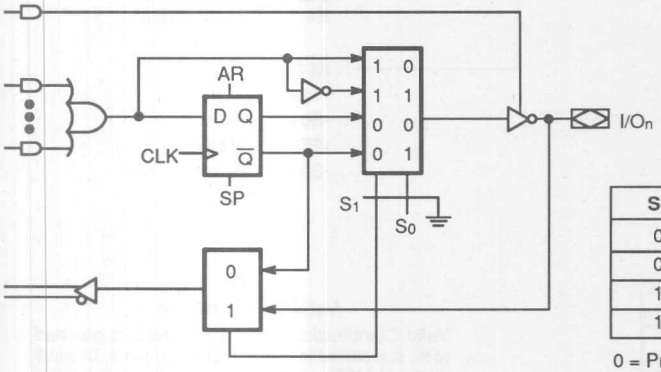
Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10 has 12 inputs and 10 I/O macrocells. The macrocell Figure 1allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 1). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

The PALCE22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

16564B-4

Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PALCE22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

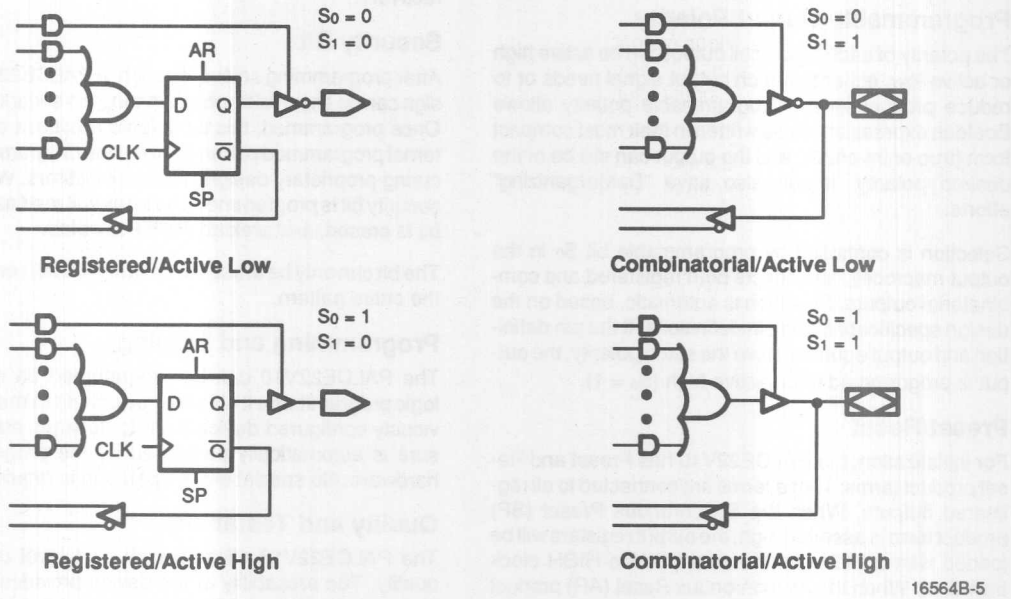


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

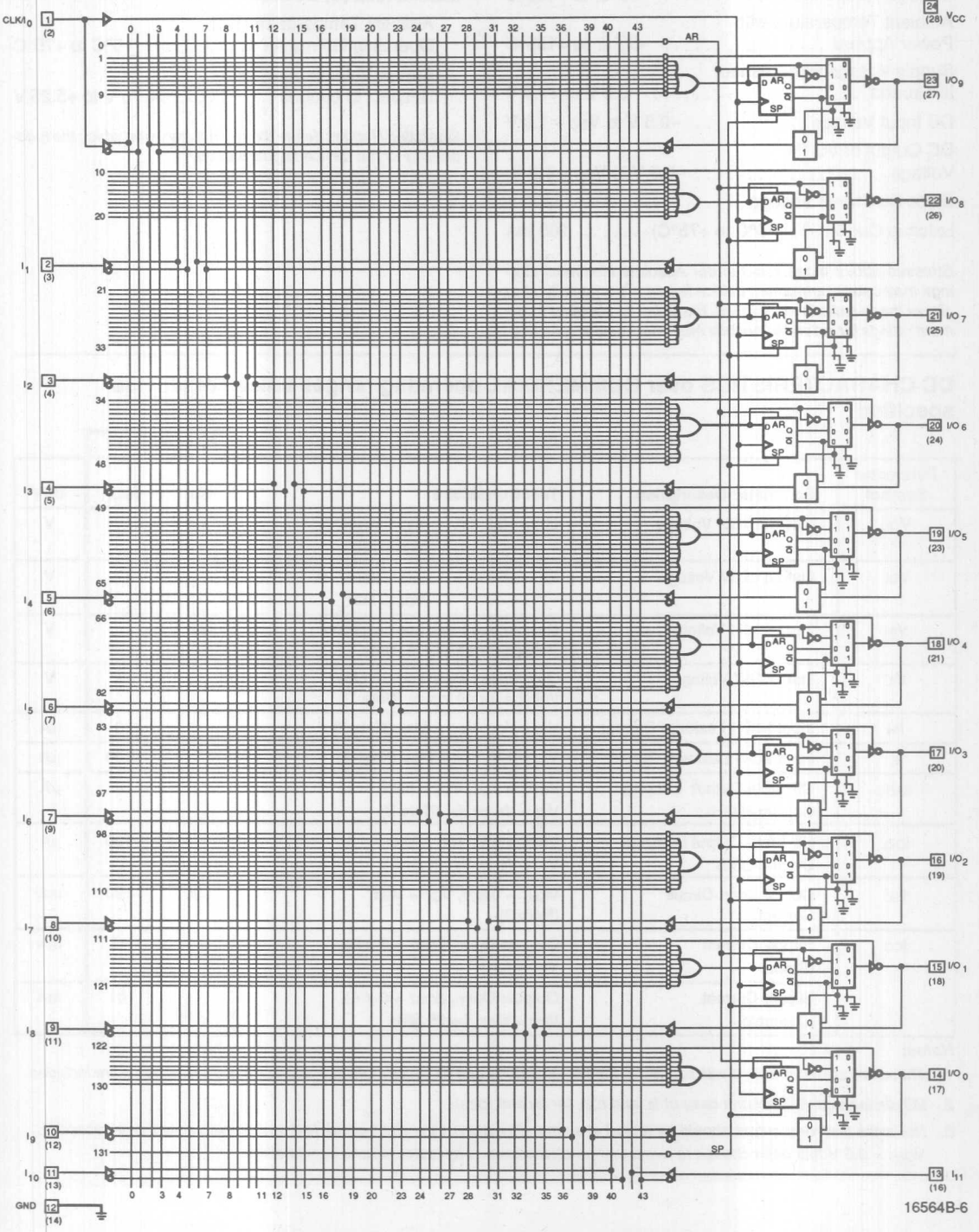
Quality and Testability

The PALCE22V10 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE22V10 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

LOGIC DIAGRAM
SKINNYDIP/SOIC/FLATPACK (PLCC/LCC) Pinouts



16564B-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	PRELIMINARY Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC}	Supply Current (Static)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		115	mA
	Supply Current (Dynamic)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

				PRELIMINARY -5		
Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	5.0	ns
t_{S1}	Setup Time from Input or Feedback			3.0		ns
t_{S2}	Setup Time from SP to Clock			4.0		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	4.0	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				1	ns
t_{AR}	Asynchronous Reset to Registered Output				7.5	ns
t_{ARW}	Asynchronous Reset Width			4.5		ns
t_{ARR}	Asynchronous Reset Recovery Time			4.5		ns
t_{SPR}	Synchronous Preset Recovery Time			4.5		ns
t_{WL}	Clock Width	LOW		2.5		ns
t_{WH}		HIGH		2.5		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT})		150		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	200		MHz
t_{EA}	Input to Output Enable Using Product Term Control				5.0	ns
t_{ER}	Input to Output Disable Using Product Term Control				5.0	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Skew is measured with all outputs switching in the same direction.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max T_A = 25°C (Note 3)	–30	–130	mA
I_{CC}	Supply Current (Static)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		115	mA
	Supply Current (Dynamic)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7 PDIP Min	-7 PDIP Max	-7 PLCC Min	-7 PLCC Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	7.5	1	7.5	ns
t_{S1}	Setup Time from Input or Feedback			5		4.5		ns
t_{S2}	Setup Time from SP to Clock			6		6		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output			1	5	1	4.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				1		1	ns
t_{AR}	Asynchronous Reset to Registered Output				10		10	ns
t_{ARW}	Asynchronous Reset Width			7		7		ns
t_{ARR}	Asynchronous Reset Recovery Time			7		7		ns
t_{SPR}	Synchronous Preset Recovery Time			7		7		ns
t_{WL}	Clock Width	LOW		3.5		3.0		ns
t_{WH}		HIGH		3.5		3.0		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	100		111		MHz
		Internal Feedback (f_{CNT})		125		133		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	142.8		166		MHz
t_{EA}	Input to Output Enable Using Product Term Control				7.5		7.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5		7.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Skew is measured with all outputs switching in the same direction.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max T_A = 25° C (Note 3)	–30	–130	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		120	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_{S1}	Setup Time from Input or Feedback			6		ns
t_{S2}	Setup Time from SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83.3		MHz
		Internal Feedback (f_{CNT})		110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	PRELIMINARY Min	PRELIMINARY Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V, T_A = 25°C (Note 3)	–30	–130	mA
I_{CC}	Supply Current (Static)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		55	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			PRELIMINARY -10 Min	PRELIMINARY -10 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input, Feedback or SP to Clock			6		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83		MHz
		Internal Feedback (f_{CNT})		110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-15) .. +4.75 V to +5.25 V

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-25) .... +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		25		ns
t_{SPR}	Synchronous Preset Recovery Time			10		25		ns
t_{WL}	Clock Width	LOW		8		13		ns
t_{WH}		HIGH		8		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		33.3		MHz
		Internal Feedback (f_{CNT})		58.8		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = –55°C to +125°C) ... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C) ..... –55°C to +125°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Note:

1. *Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.*

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 5)		–50	–135	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	-15/-20		120	mA
			-25/-30		100	

Notes:

2. *For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

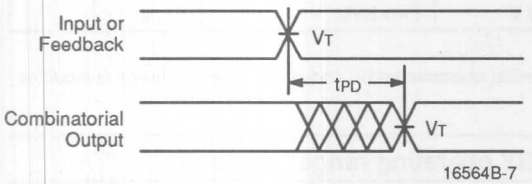
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		-15		-20		-25		-30		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output			15		20		25		30	ns
t_S	Setup Time from Input, Feedback or SP to Clock		12		15		18		20		ns
t_H	Hold Time (Note 3)		0		0		0		0		ns
t_{CO}	Clock to Output			8		15		20		20	ns
t_{AR}	Asynchronous Reset to Registered Output			20		25		25		30	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		25		30		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		25		30		ns
t_{SPR}	Synchronous Preset Recovery Time		15		20		25		30		ns
t_{WL}	Clock Width	LOW	8		10		15		15		ns
t_{WH}		HIGH	8		10		15		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback $1/(t_S + t_{CO})$	50		33.3		26.3		25		MHz
		Internal Feedback (f_{CNT})	53		40		32.2		25		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			15		20		25		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)			15		20		25		25	ns

Notes:

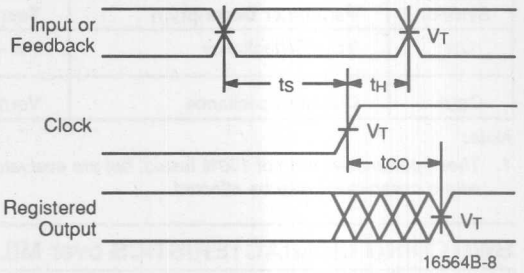
2. *See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 7, 8, 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

SWITCHING WAVEFORMS



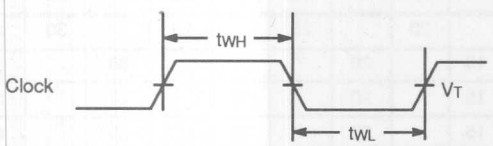
16564B-7

Combinatorial Output



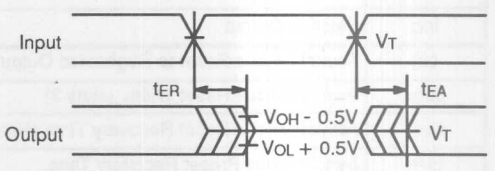
16564B-8

Registered Output



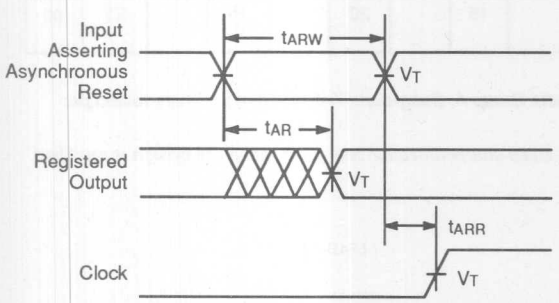
16564B-9

Clock Width



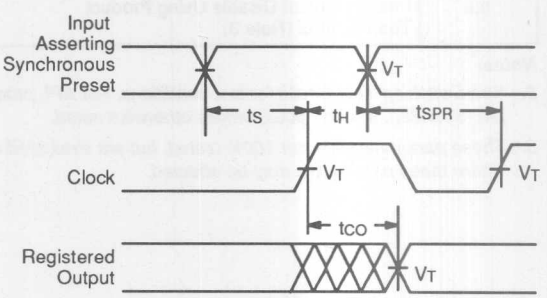
16564B-10

Input to Output Disable/Enable



16564B-11

Asynchronous Reset



16564B-12

Synchronous Preset

Notes:

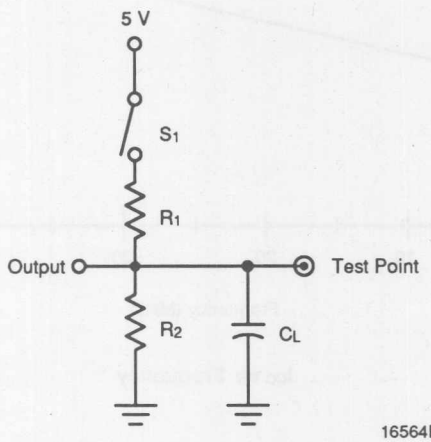
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

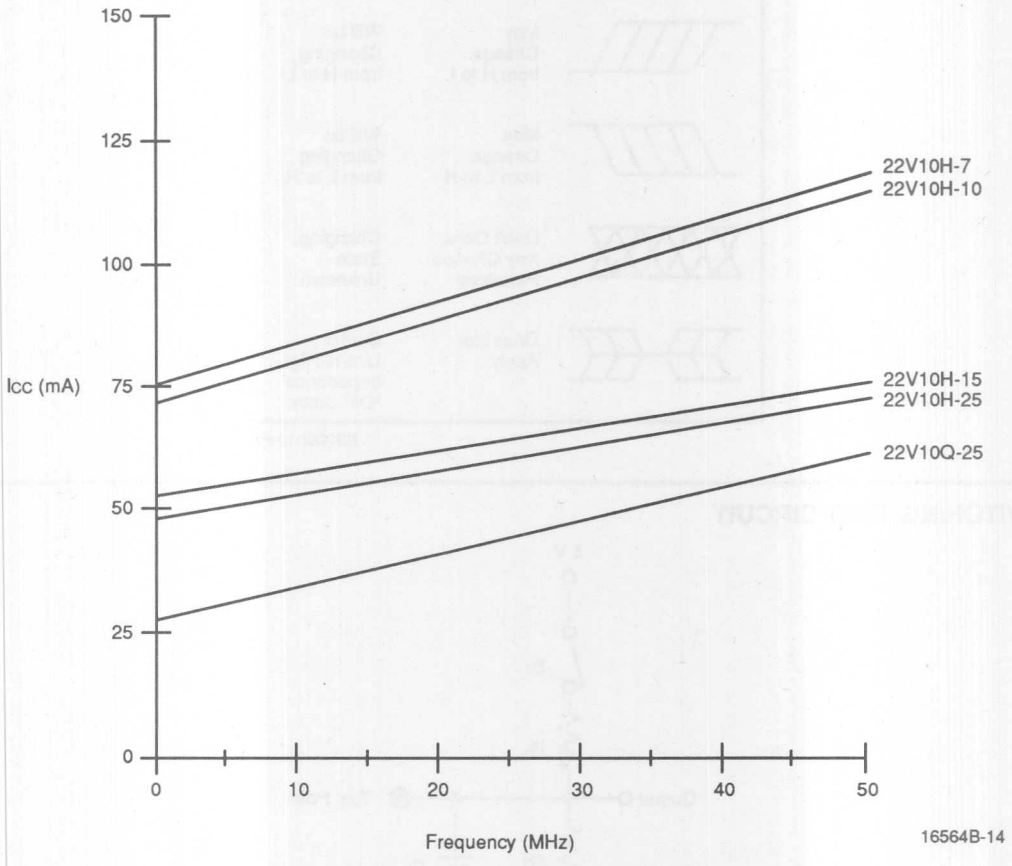


16564B-13

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Military R_1	Military R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	All except H-5/7: 390 Ω	390 Ω	750 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF		H-5/7: 300 Ω			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

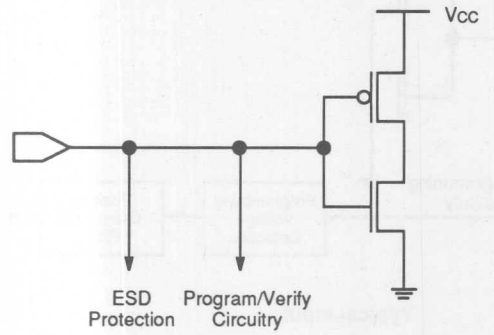
ENDURANCE CHARACTERISTICS

The PALCE22V10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

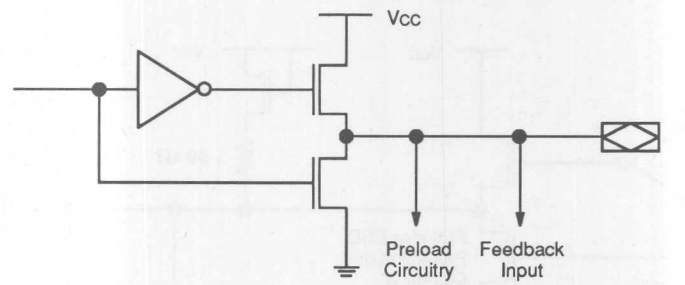
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature (Military)	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



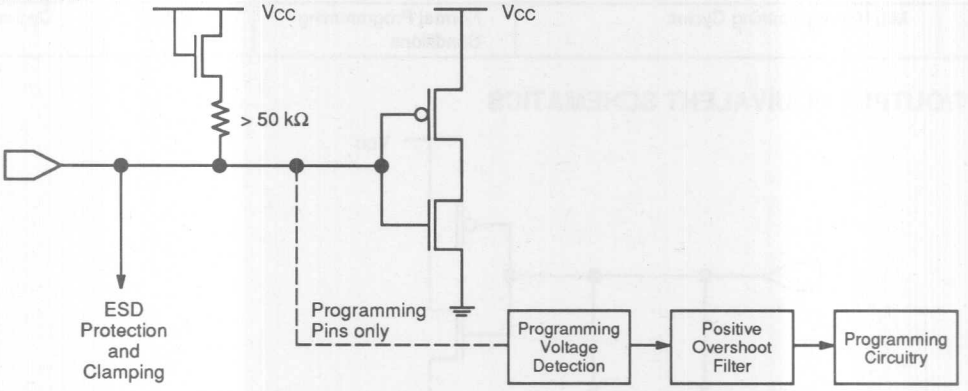
Typical Output

ROBUSTNESS FEATURES

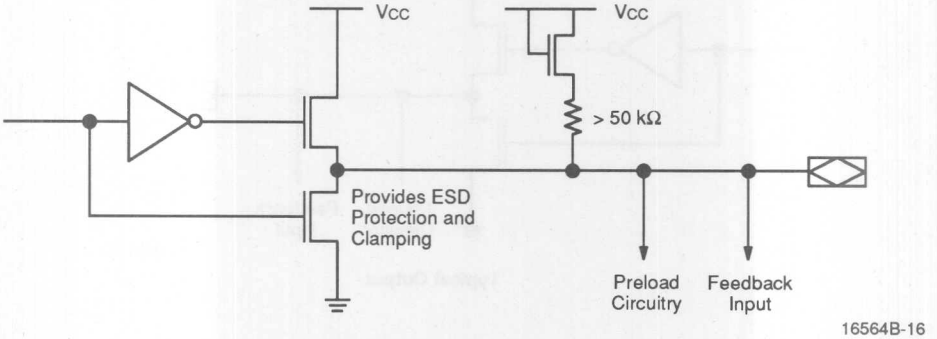
The PALCE22V10X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing.

A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 version. Selected /4 devices are also being retrofitted with these robustness features. See the chart below for device listing.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSION AND SELECTED /4 DEVICES*



Typical Input



Typical Output

*

Device	Rev Letter
PALCE22V10H-15	D
PALCE22V10H-25	D
PALCE22V10Q-25	B

Topside Marking:

AMD CMOS PLD's are marked on top of the package in the following manner:

PALCEXXXX
Datecode (3 numbers) Lot ID (4 characters)– –(Rev Letter)

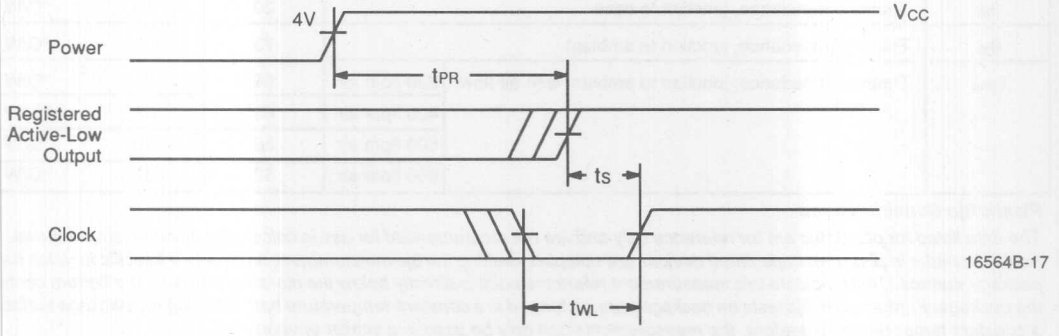
The Lot ID and Rev Letter are separated by two spaces.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

Parameter Symbol	Parameter Description		Typ SKINNYDIP	Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		15	16	°C/W
θ_{ja}	Thermal impedance, junction to ambient		72	54	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	67	49	°C/W
		400 lfpm air	60	43	°C/W
		600 lfpm air	53	37	°C/W
		800 lfpm air	46	31	°C/W

PALCE22V10/5 (PALCE22V10H-10)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ SKINNYDIP	Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		20	18	°C/W
θ_{ja}	Thermal impedance, junction to ambient		73	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	66	48	°C/W
		400 lfpm air	61	43	°C/W
		600 lfpm air	55	40	°C/W
		800 lfpm air	52	37	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PALCE22V10Z Family

Zero-Power 24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero-power CMOS technology**
  - 15 µA standby current
  - As fast as 15 ns first-access propagation delay and 50 MHz f_{MAX} (external)
- **Unused product term disable for reduced power consumption**
- **Available in Industrial operating range**
  - T_C = –40°C to +85°C
  - V_{CC} = +4.5 V to +5.5 V
- **HC- and HCT-compatible inputs and outputs**
- **Electrically-erasable technology provides reconfigurable logic and full testability**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PALCE22V10Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE22V10Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALCE22V10Z allows battery powered operation for an extended period.

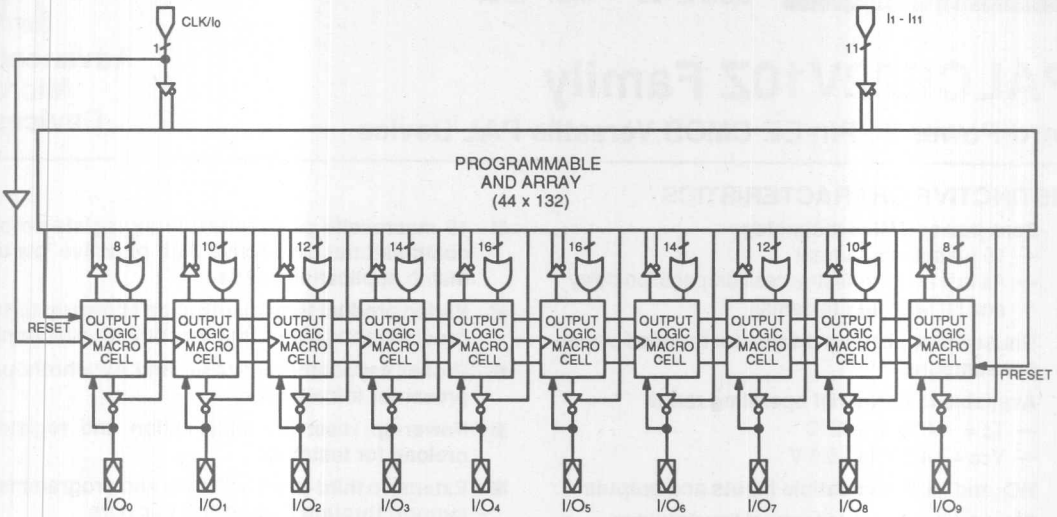
The ZPAL™ device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the Software Reference Guide to PLD Compliers for certified development systems, and the Programmer Reference Guide for approved programmers.

Publication# 15700 Rev. C Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM

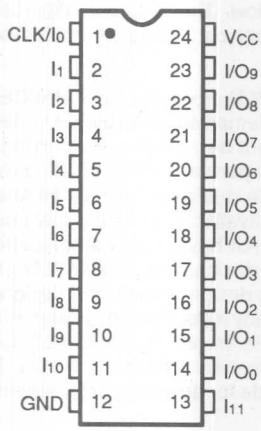


15700C-1

CONNECTION DIAGRAMS

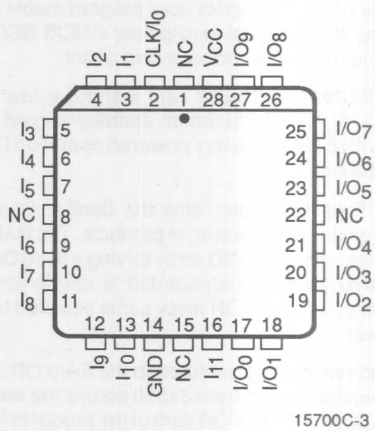
Top View

SKINNYDIP/SOIC



15700C-2

PLCC



15700C-3

Note:

Pin 1 is marked for orientation.

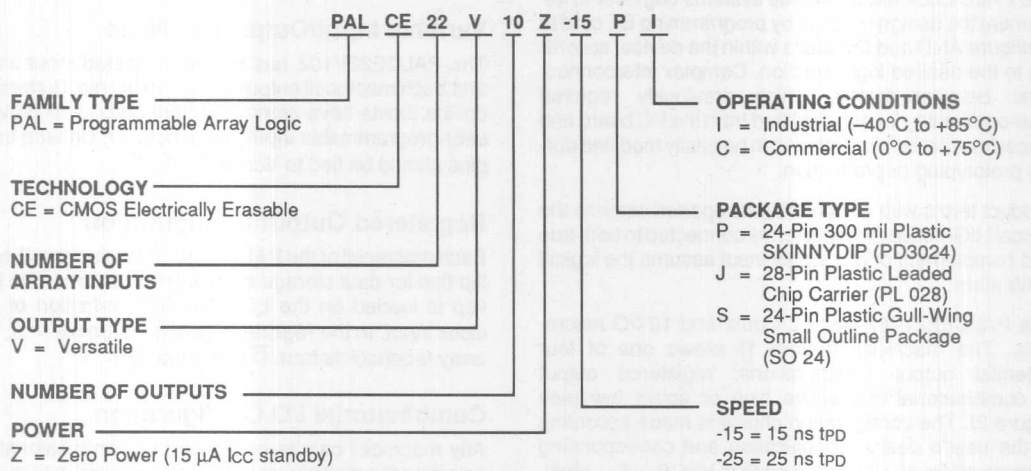
PIN DESCRIPTION

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
PALCE22V10Z-15	PI, JI, SI,
PALCE22V10Z-25	PC, JC, SC, PI, JI, SI

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10Z is the zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALCE22V10Z has zero standby power and unused product term disable.

The PALCE22V10Z allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10Z has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

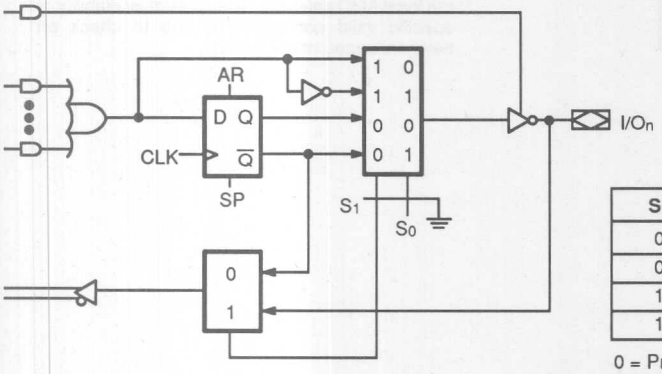
The PALCE22V10Z has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALCE22V10Z includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

15700C-4

Figure 1. Output Logic Macrocell

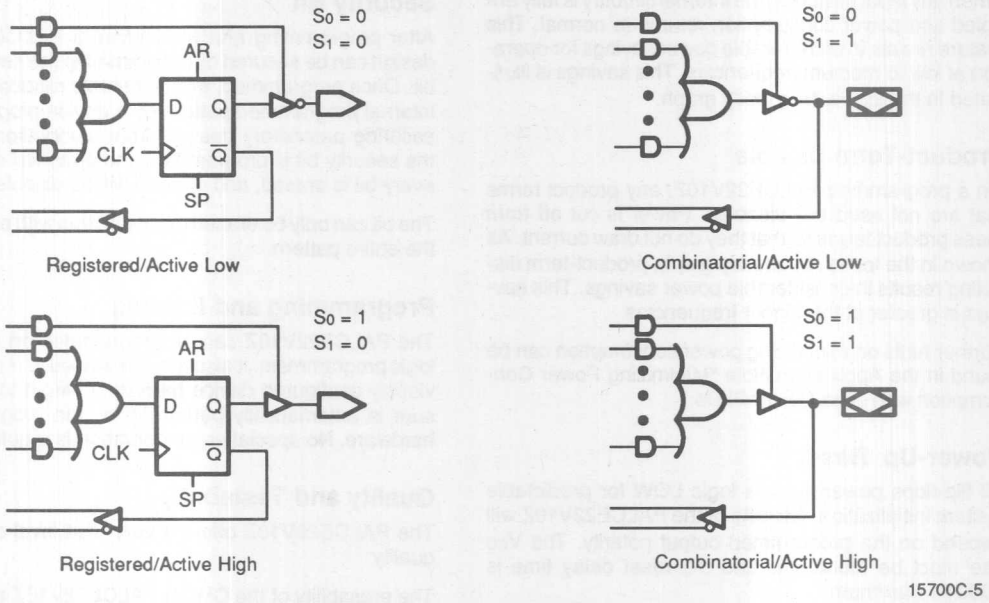


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10Z has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Zero-Standby Power Mode

The PALCE22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 15\ \mu A$). The outputs will maintain the states held before the device went into the standby mode.

trated in the Icc vs. frequency graph.

Product-Term Disable

On a programmed PALCE22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the Icc vs. frequency graph, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note "Minimizing Power Consumption with Zero-Power PLDs."

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10Z will depend on the programmed output polarity. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The registers on the PALCE22V10Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

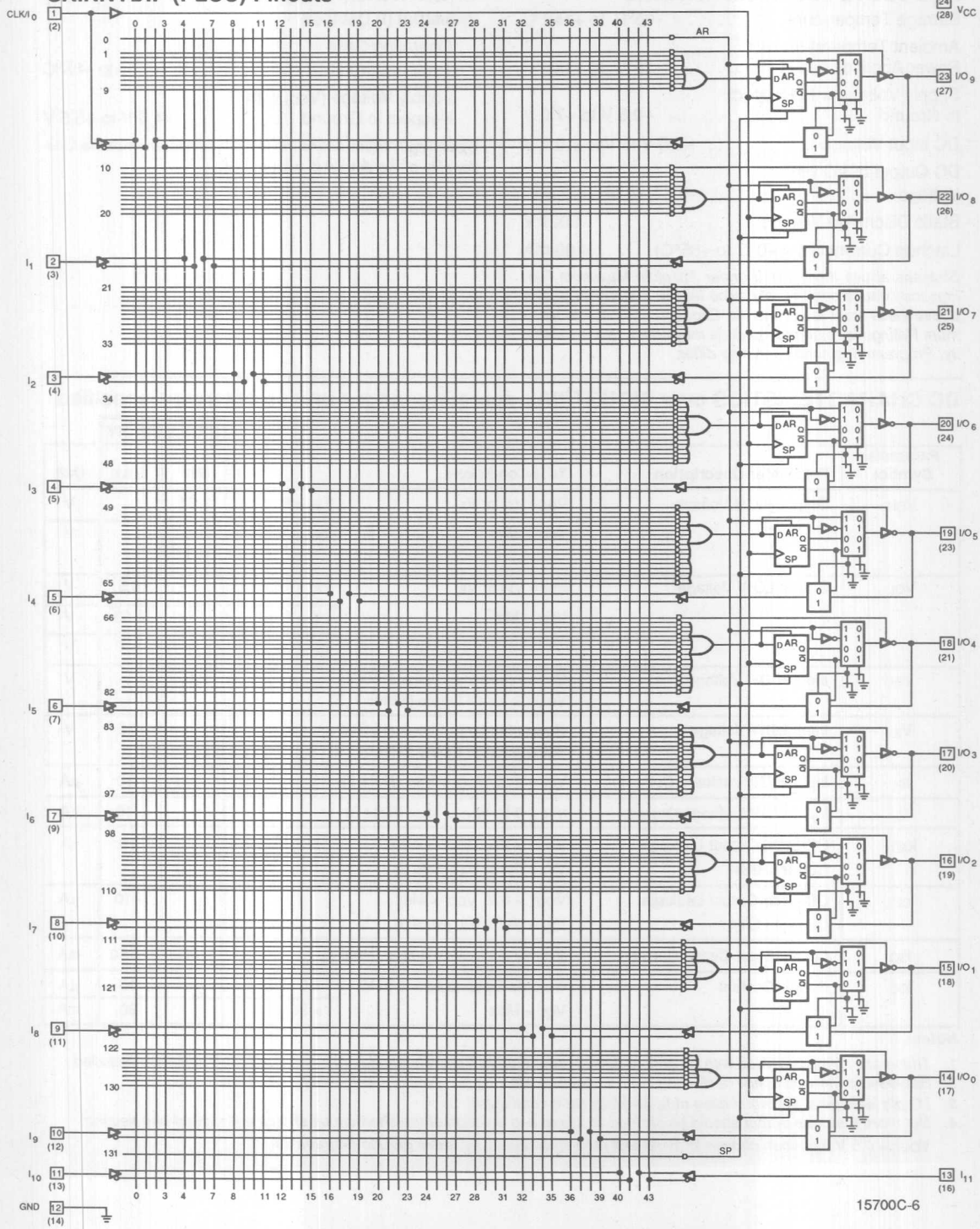
The PALCE22V10Z offers a very high level of built-in quality.

The erasability of the CMOS PALCE22V10Z allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALCE22V10Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts



15700C-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_C = 40°C to +85°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case Temperature (T_C) ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

				PRELIMINARY		
Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min	I_{OH} = 20 µA	V_{CC}– 0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		15	µA
		V_{CC} = Max	f = 25 MHz		90	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			PRELIMINARY Min	PRELIMINARY Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			15		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_C = –40°C to +85°C) .... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case Temperature (T_C) ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min	I_{OH} = 20 µA	V_{CC}– 0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		15	µA
		V_{CC} = Max	f = 25 MHz		120	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

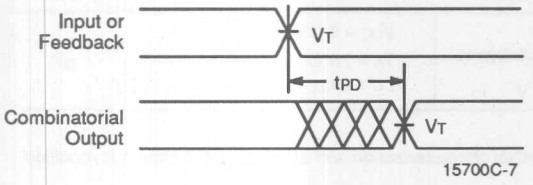
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})		35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

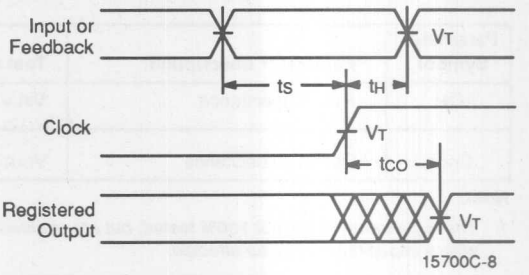
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 5 ns faster.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

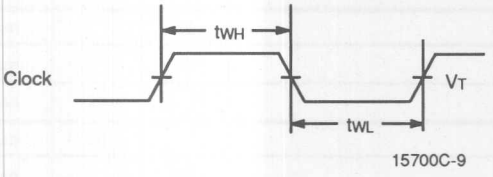
SWITCHING WAVEFORMS



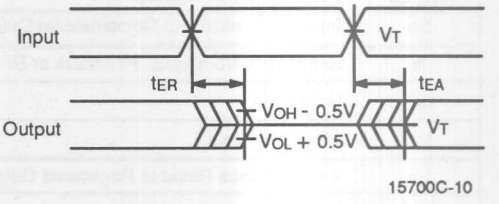
Combinatorial Output



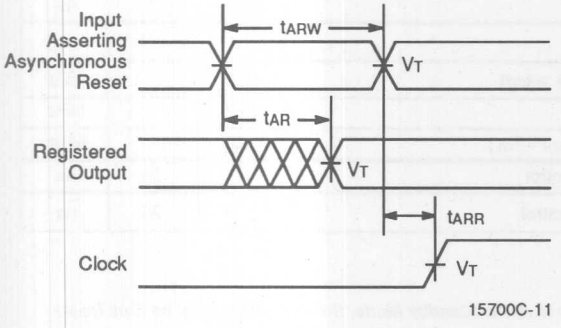
Registered Output



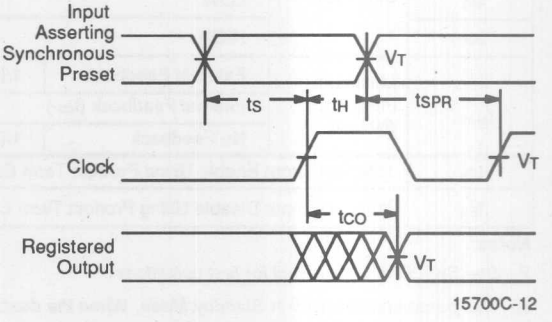
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Notes:

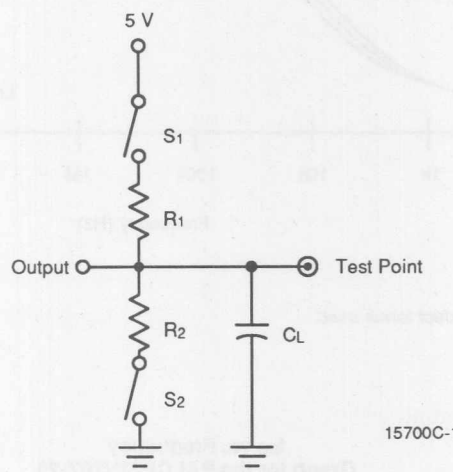
1. *V_T = 1.5 V for Input Signals and 2.5 V for Output Signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

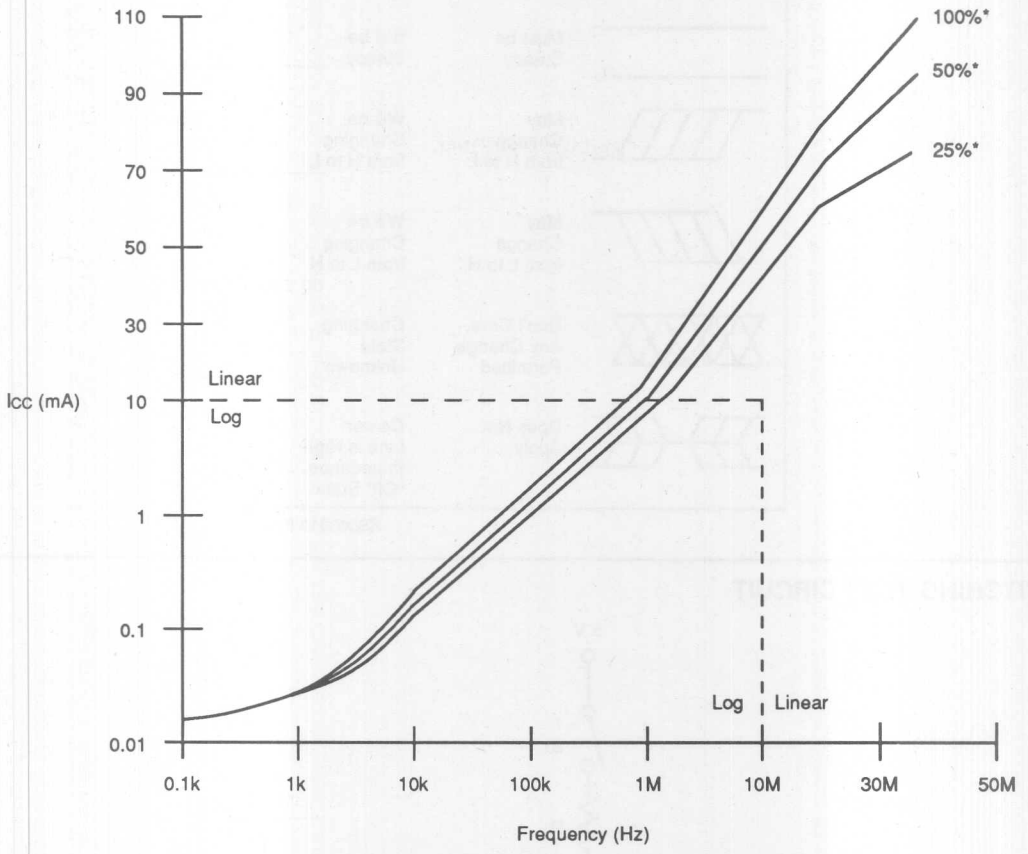
SWITCHING TEST CIRCUIT



15700C-13

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	820 Ω	820 Ω	2.5 V
t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				2.5 V
t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE22V10Z-25
V_{CC} = 5.0 V, T_A = 25°C



*Percent of product terms used.

15700C-15

I_{CC} vs. Frequency Graph for the PALCE22V10Z-25

ENDURANCE CHARACTERISTICS

The PALCE22V10Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

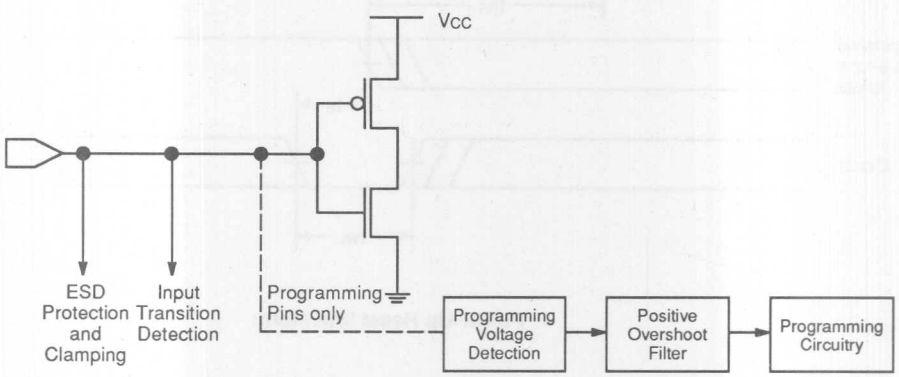
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

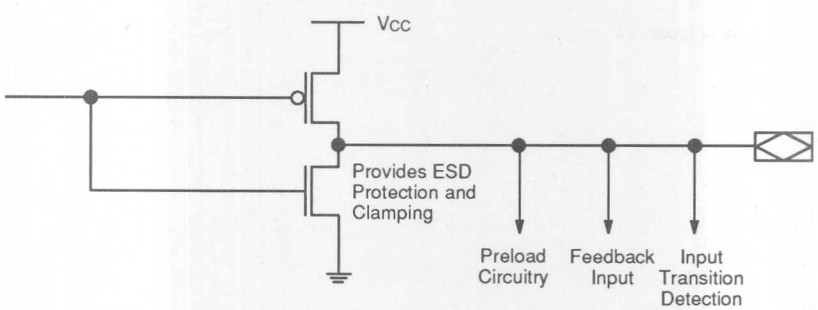
ROBUSTNESS FEATURES

The PALCE22V10Z has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

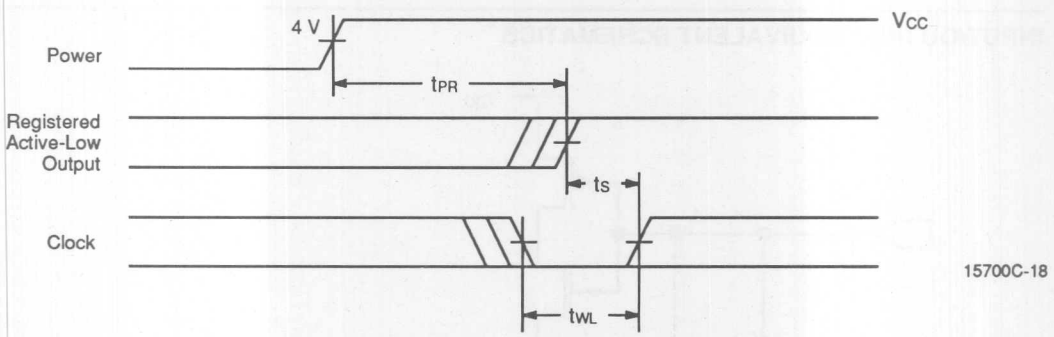
15700C-16

POWER-UP RESET FOR THE PALCE22V10Z-15

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



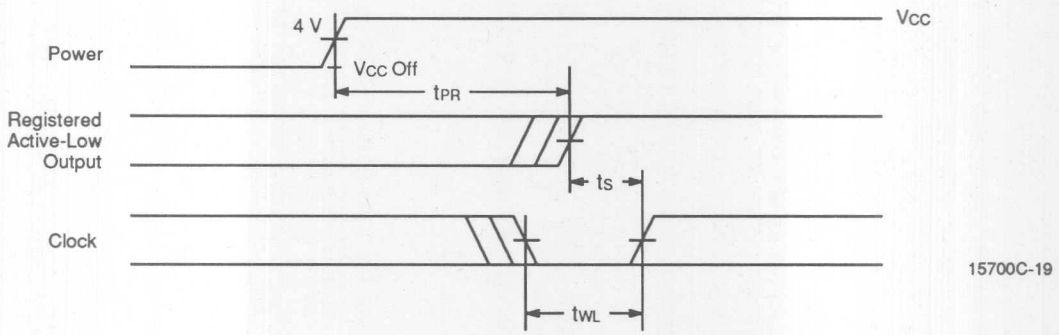
Power-Up Reset Waveform

POWER-UP RESET FOR THE PALCE22V10Z-25

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, four conditions are required to ensure a valid power-up reset. These conditions are:

- The supply voltage prior to the V_{CC} rise must not exceed V_{CC} off.
- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.
- If inputs are not switching at the time of power-up, an input transition must take place to assure proper data is set-up in registers or to outputs.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		
V_{CC} Off	Supply Voltage Prior to Power-Up	100	mV



Power-Up Reset Waveform



ZPAL™ Devices

PRELIMINARY IND: -25

PALLV22V10Z-25

Low-Voltage, Zero-Power 24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
- **Zero-power CMOS technology**
  - — 15 µA standby current
  - — 25 ns first-access propagation delay
- **Unused product term disable for reduced power consumption**
- **Industrial operating temperature range**
  - — Tc = –40°C to +85°C
- **3.3 V (CMOS) and 5 V (CMOS and TTL)-compatible inputs and I/O**
- **Electrically-erasable technology provides reconfigurable logic and full testability**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP, 24-pin SOIC and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PALLV22V10Z is an advanced PAL device built with low-voltage, zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

The PALLV22V10Z provides high speed at low voltage and zero standby power. At 15 µA maximum standby current, the PALLV22V10Z allows battery powered operation for an extended period.

The ZPAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

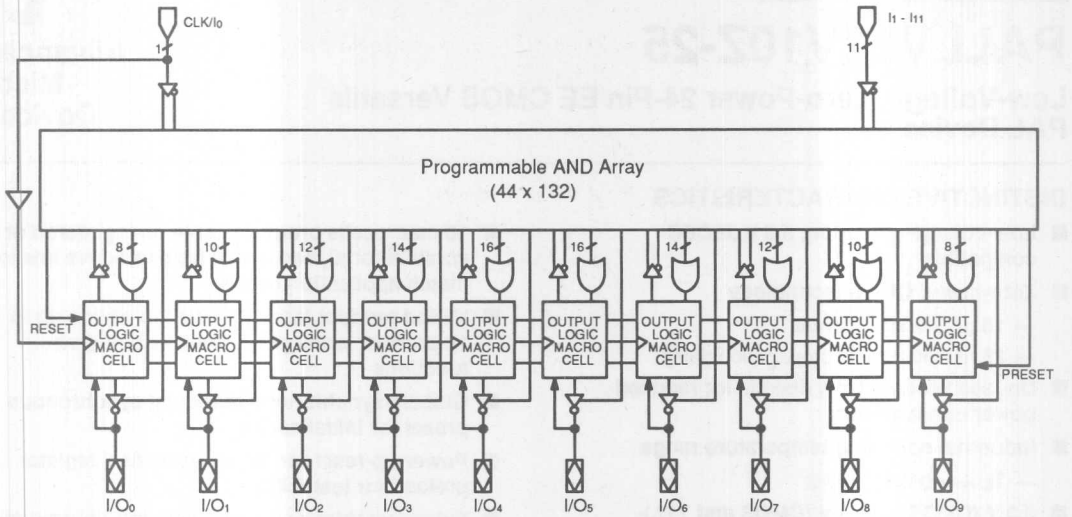
The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALLV22V10Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the Software Reference Guide to PLD Compliers for certified development systems, and the Programmer Reference Guide for approved programmers.

Publication# 17661 Rev. A Amendment /0
Issue Date: February 1993

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

BLOCK DIAGRAM

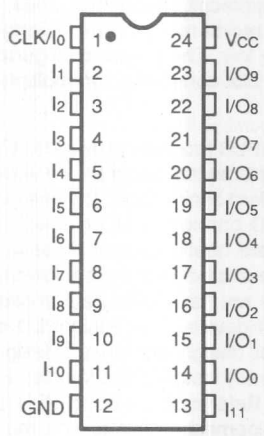


17661A-1

CONNECTION DIAGRAMS

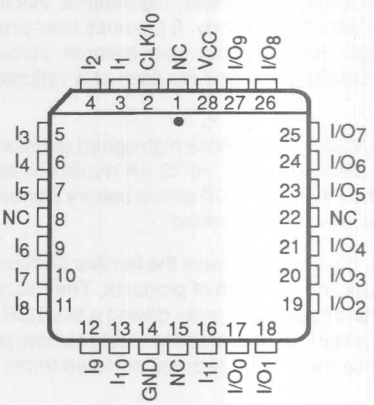
Top View

SKINNYDIP/SOIC



17661A-2

PLCC



17661A-3

Note:
Pin 1 is marked for orientation.

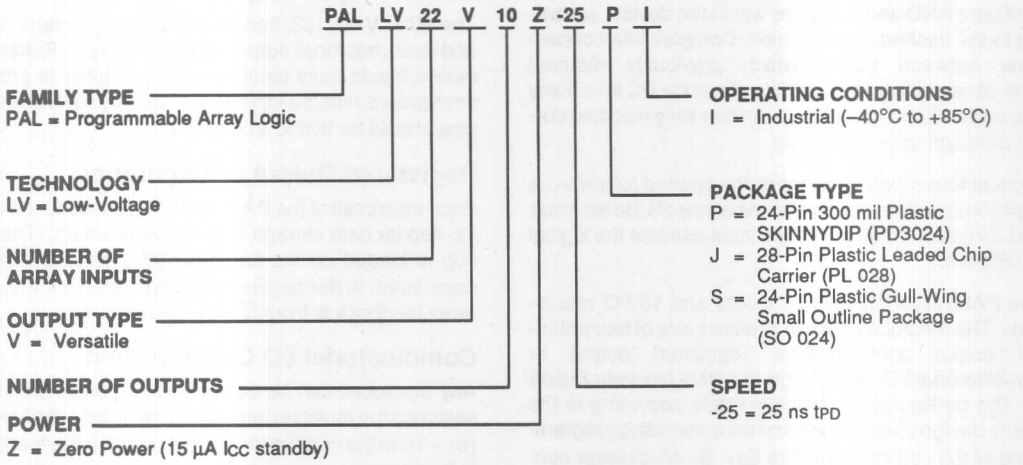
PIN DESCRIPTION

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
VCC	=	Supply Voltage

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
PALLV22V10Z-25	PI, JI, SI

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALLV22V10Z is the low-voltage, zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALLV22V10Z has zero standby power and unused product term disable.

The PALLV22V10Z allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALLV22V10Z has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

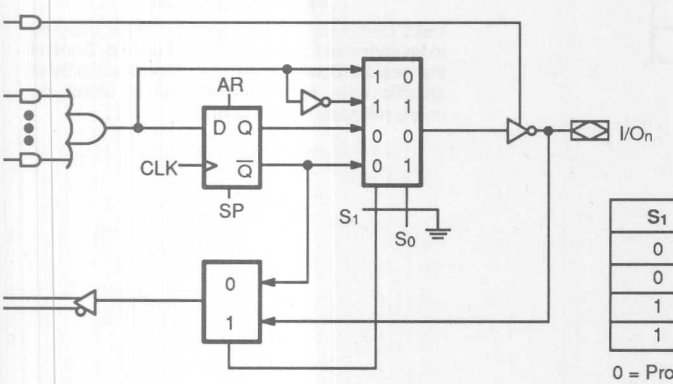
The PALLV22V10Z has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALLV22V10Z includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

17661A-4

Figure 1. Output Logic Macrocell

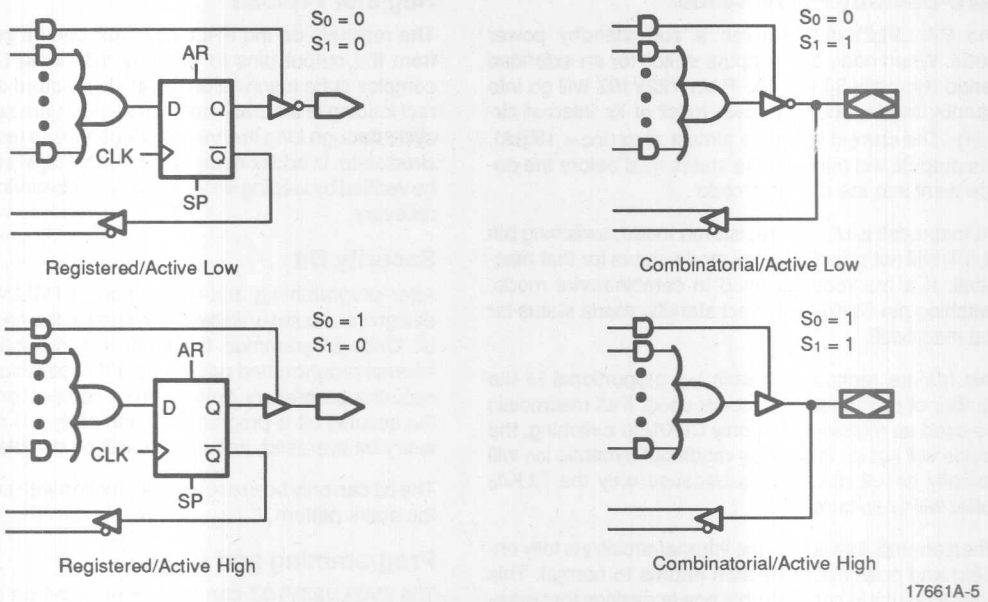


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALLV22V10Z has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Benefits of Lower Operating Voltage

The PALLV22V10Z has an operating voltage range of 3.0 V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3 V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. Lower operating voltage also reduces electromagnetic radiation noise and makes obtaining FCC approval easier.

Zero-Standby Power Mode

The PALLV22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 30 ns), the PALLV22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero (I_{CC} < 15 µA). The outputs will maintain the states held before the device went into the standby mode.

If a macrocell is used in registered mode, switching pin CLK/I_0 will not affect standby mode status for that macrocell. If a macrocell is used in combinatorial mode, switching pin CLK/I_0 will affect standby mode status for that macrocell.

This feature reduces dynamic I_{CC} proportional to the number of registered macrocells used. If all macrocells are used as registers, and only CLK/I_0 is switching, the device will not be in standby mode but dynamic I_{CC} will typically be <2 mA. This is because only the CLK/I_0 buffer will draw current.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies.

Product-Term Disable

On a programmed PALLV22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. Product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note "Minimizing Power Consumption with Zero-Power PLDs."

3.3 V (CMOS) and 5 V (CMOS and TTL)-Compatible Inputs and I/O

Input voltages can be at TTL levels without the device drawing more current than true 3.3 V CMOS levels. Additionally, the PALLV22V10Z can be driven with true 5 V CMOS levels due to special input and I/O buffer circuitry.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALLV22V10Z will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The registers on the PALLV22V10Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALLV22V10Z design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALLV22V10Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALLV22V10Z offers a very high level of built-in quality.

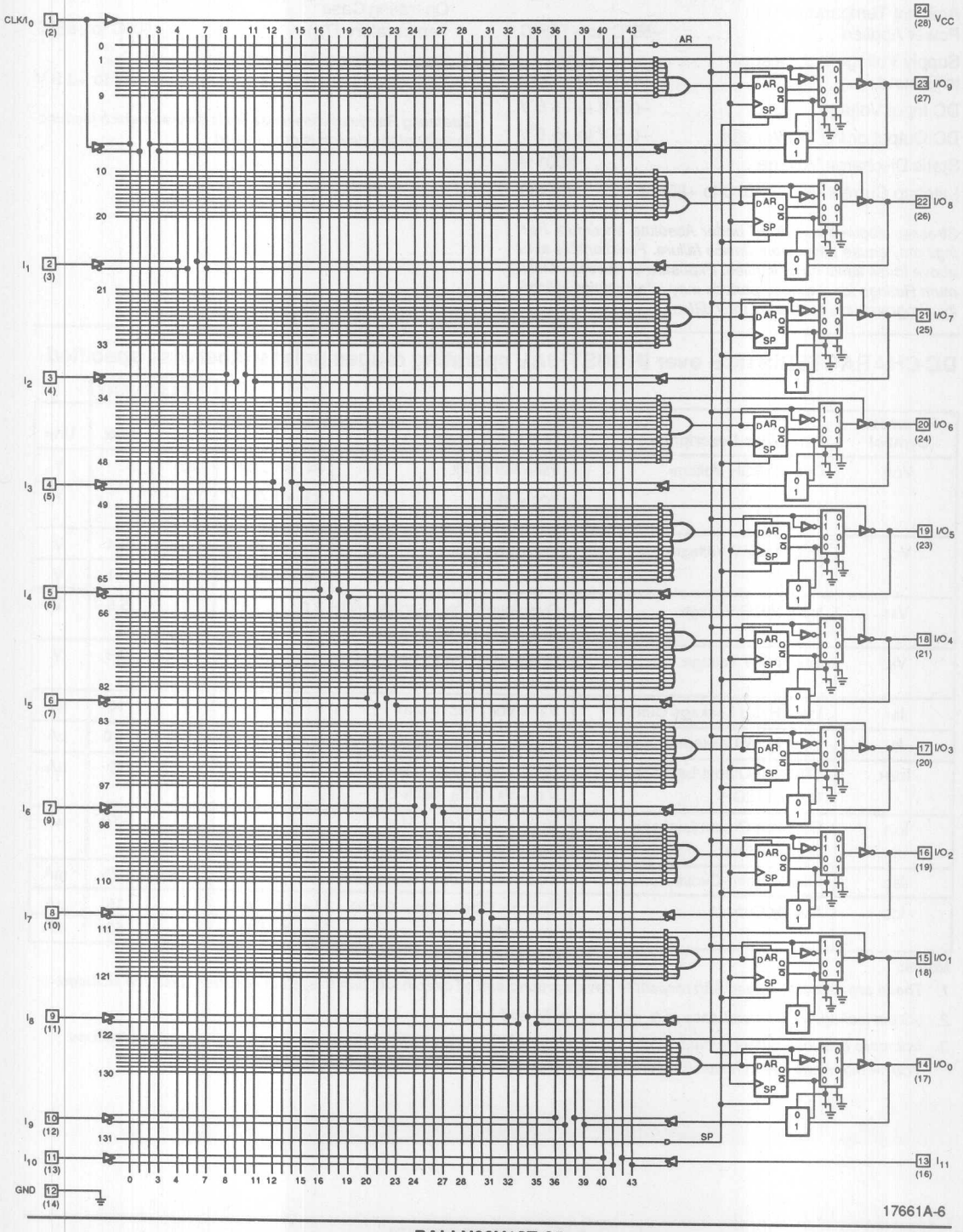
The erasability of the CMOS PALLV22V10Z allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALLV22V10Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be 3.3 and 5 V device compatible. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM

SKINNYDIP (PLCC) Pinouts



17661A-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to +5.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to +5.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_C = –40°C to +85°C) .... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case Temperature (T_C) ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +3.0 V to +3.6 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

				PRELIMINARY		
Parameter Symbol	**Parameter Description**	**Test Conditions**		**Min**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –2 mA	2.4		V
		V_{CC} = Min	I_{OH} = 100 µA	V_{CC}– 0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 2 mA		0.4	V
			I_{OL} = 100 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15	–75	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		15	µA
		V_{CC} = Max	f = 25 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

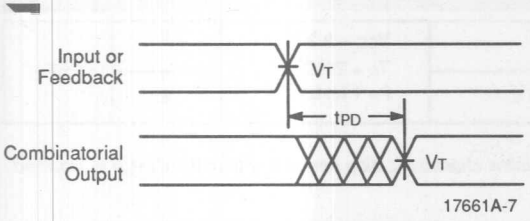
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

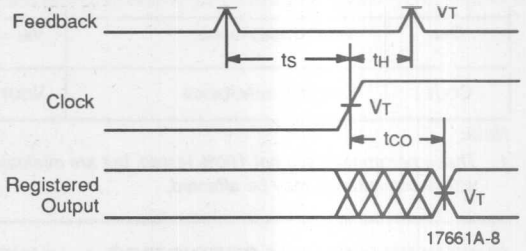
				PRELIMINARY		
Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})		35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

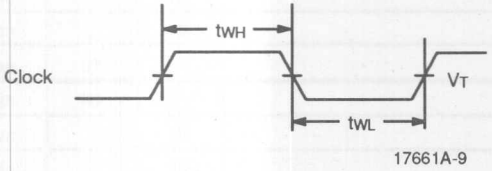
2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} may be slightly faster.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*



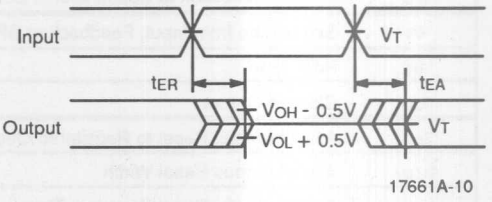
Combinatorial Output



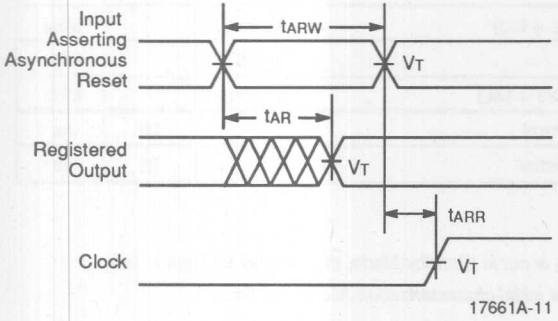
Registered Output



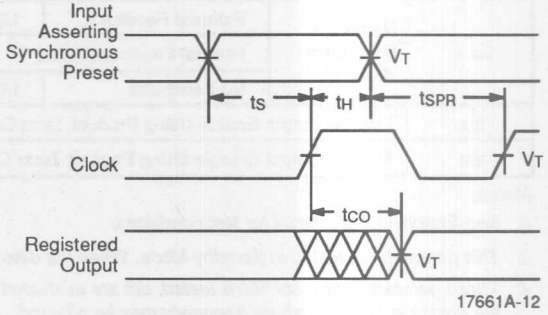
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Notes:

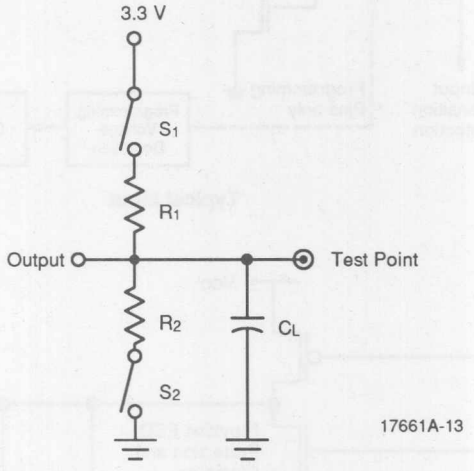
1. *V_T = 1.5 V for Input Signals and 1.65 V for Output Signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



17661A-13

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	1.6K Ω	1.6K Ω	1.65 V
t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				1.65 V
t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

ENDURANCE CHARACTERISTICS

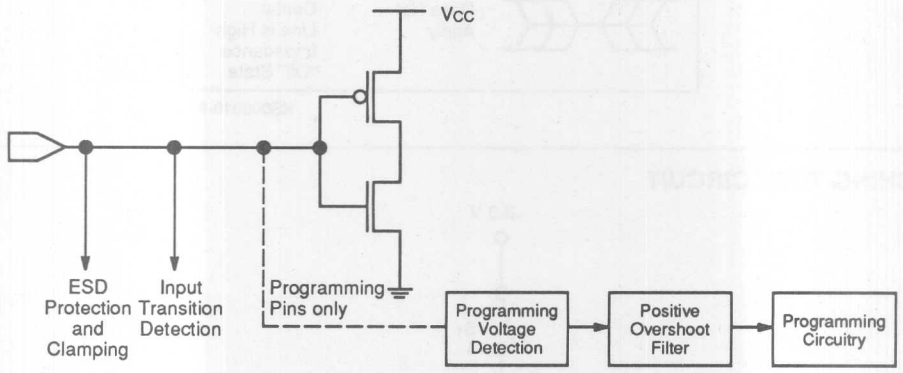
The PALLV22V10Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

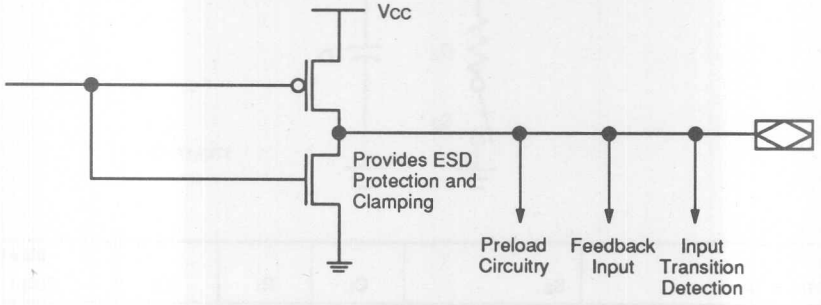
ROBUSTNESS FEATURES

The PALLV22V10Z-25 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

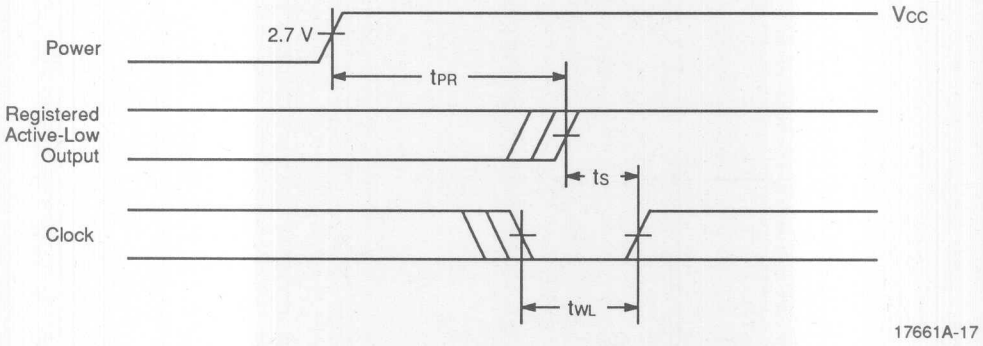
17661A-16

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform



Z PAL™ Devices

PALCE24V10H-15/25

EE CMOS 28-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High speed CMOS technology**
  - — 15 ns propagation delay for "-15" version
  - — 25 ns propagation delay for "-25" version
- **Outputs individually programmable as registered or combinatorial**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Cost-effective 28-pin plastic SKINNYDIP and PLCC packages**
- **Extensive third-party support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

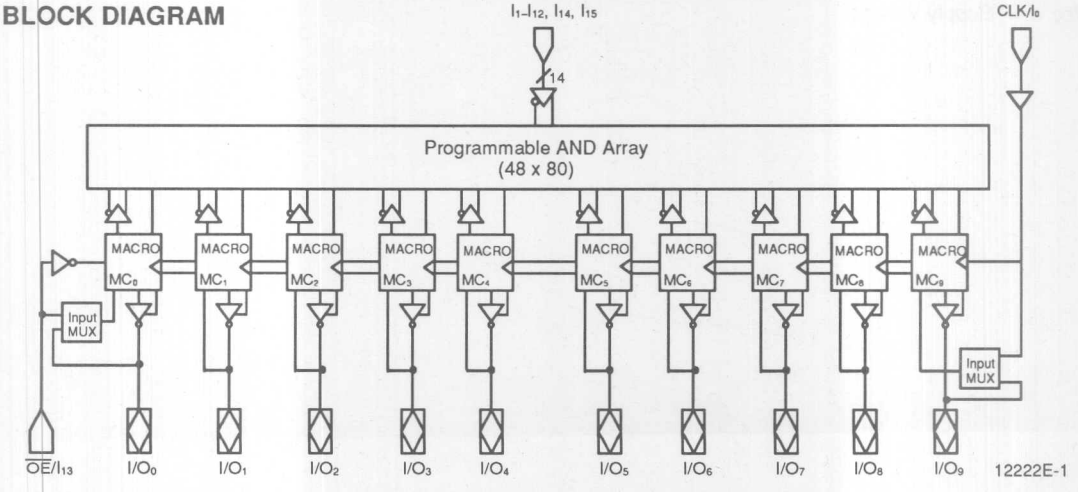
The PALCE24V10 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture.

The PALCE24V10 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE24V10 designs to be implemented using a wide a variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

BLOCK DIAGRAM

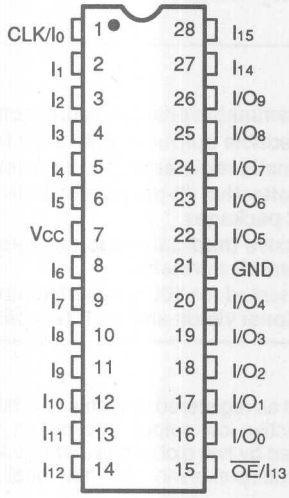


Publication# 12222 Rev. E Amendment /0
Issue Date: June 1993

CONNECTION DIAGRAMS

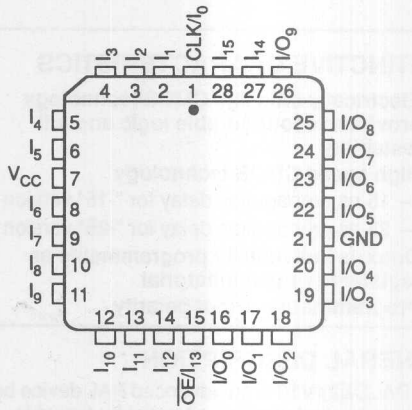
Top View

SKINNYDIP



12222E-2

PLCC



12222E-3

Note:
Pin 1 is marked for orientation.

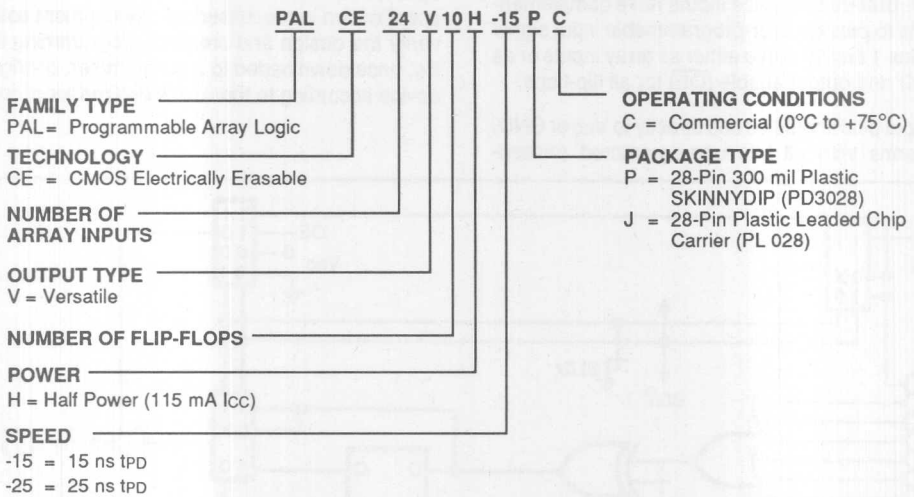
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
$\overline{OE}$ = Output Enable
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE24V10H-15	PC, JC
PALCE24V10H-25	

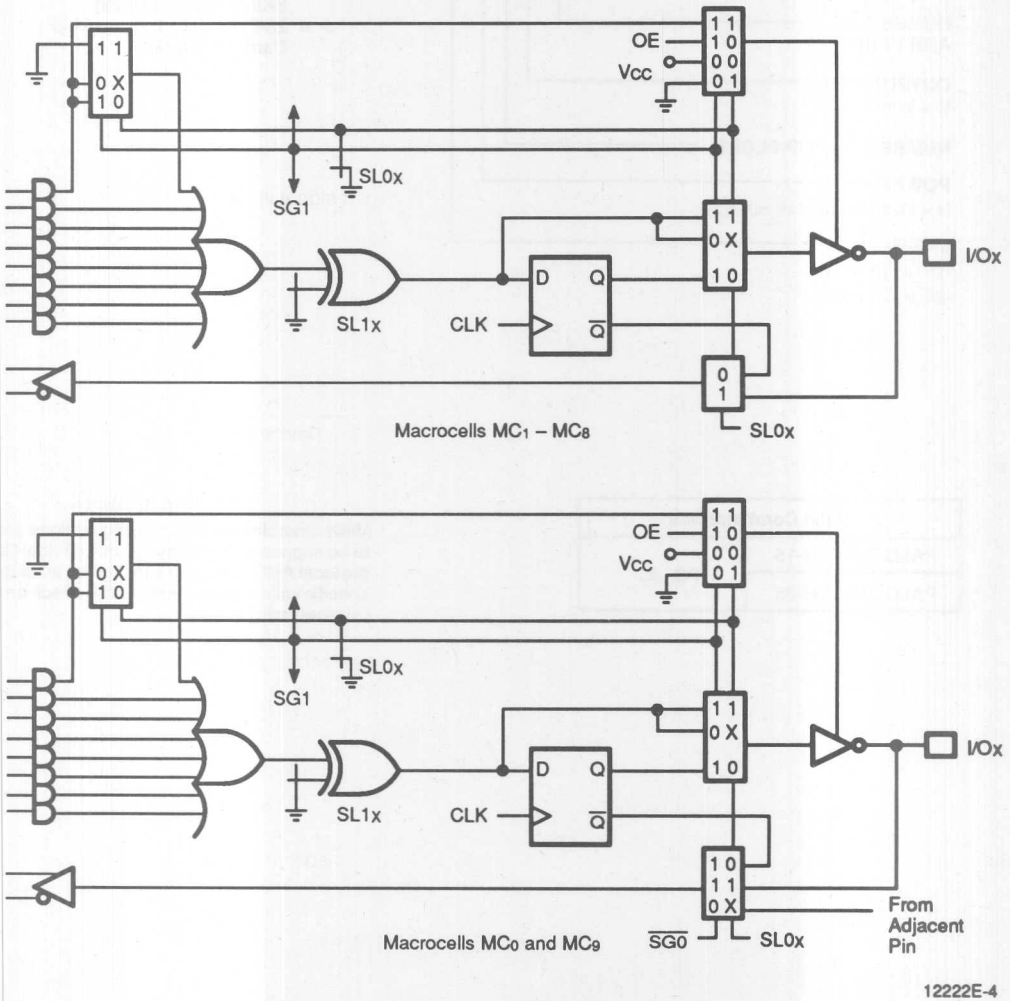
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 15 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to Vcc or GND. Product terms with all bits unprogrammed (disconnected assume a logical LOW state.

The programmable functions on the PALCE24V10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.



PALCE24V10 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 20 local bits ($SL0_0$ through $SL0_9$ and $SL1_0$ through $SL1_9$). SG0 determines whether registers will be allowed. SG1 determines whether the output buffer is user-controlled or in a fixed state. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_9, $\overline{SG0}$ is added on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE24V10 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins are available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE24V10 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Because the macrocell is a dedicated output, the feedback is not used.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is the I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0,SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

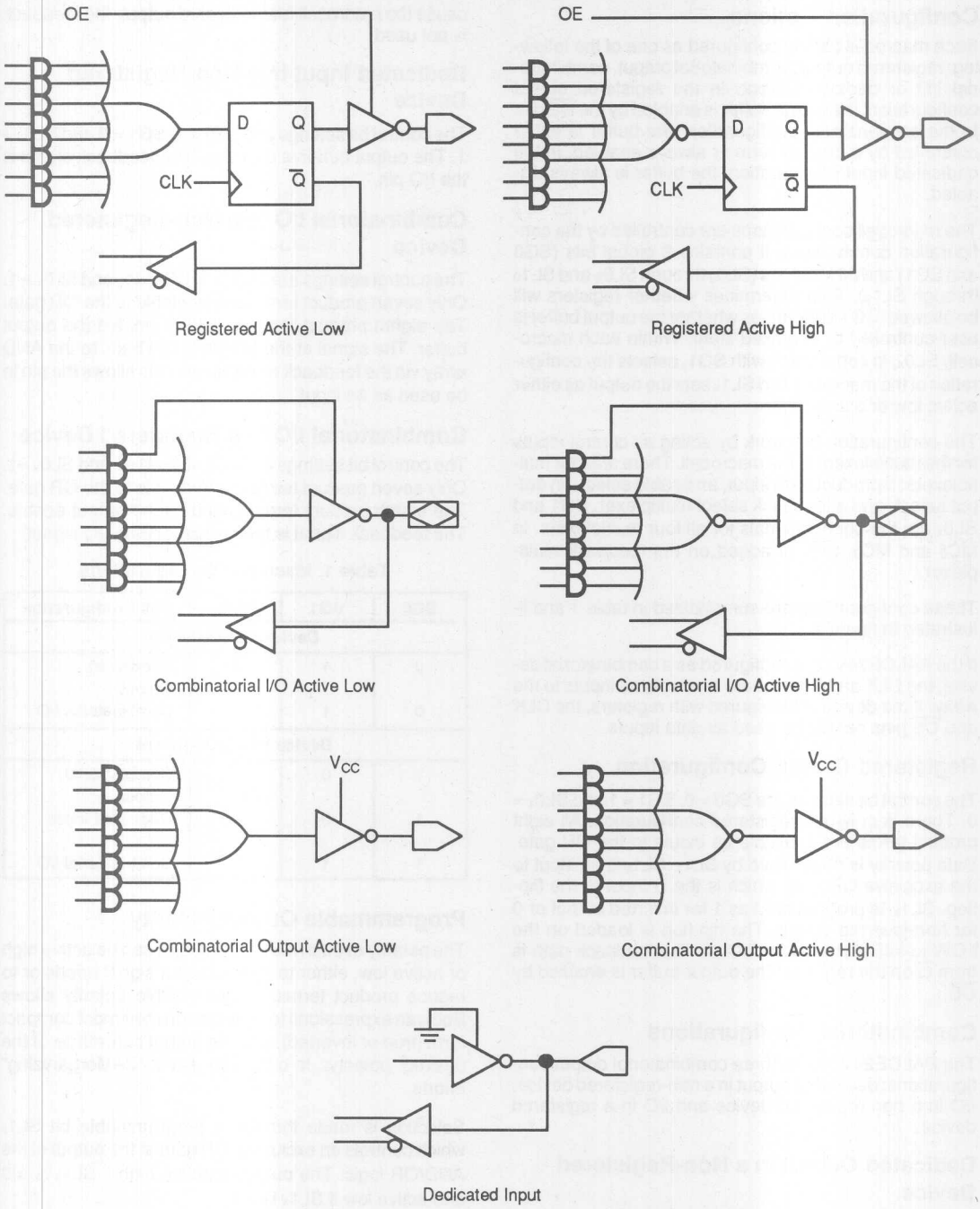
Table 1. Macrocell Configurations

SG0	SG1	$SL0_x$	Cell Configuration
Device has registers			
0	1	0	Registered Output
0	1	1	Combinatorial I/O
Device has no registers			
1	0	0	Combinatorial Output
1	0	1	Dedicated Input
1	1	1	Combinatorial I/O

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is made through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is a 0 and active low if $SL1_x$ is a 1.



12222E-5

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE24V10 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE24V10 Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE24V10 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE24V10. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE24V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

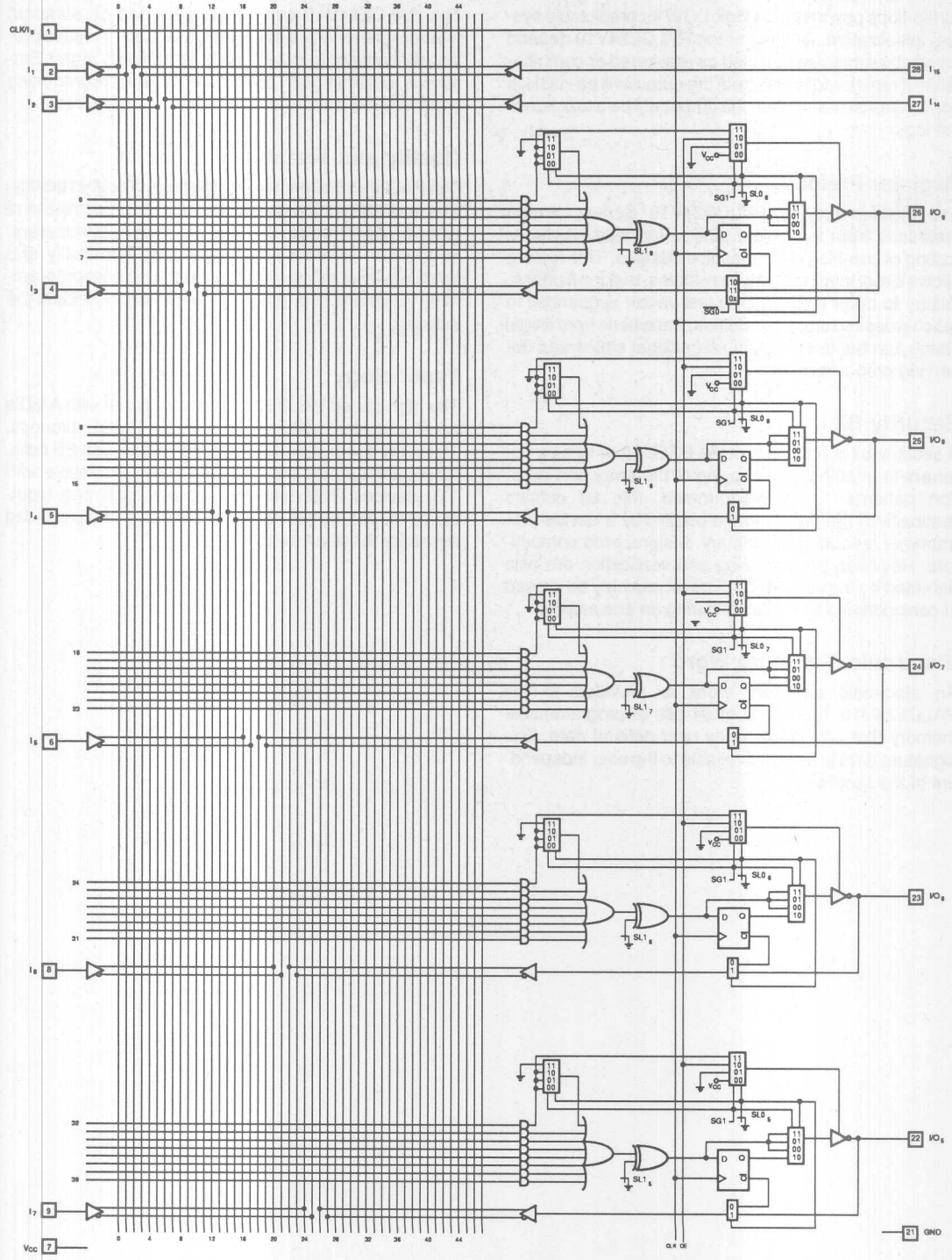
Quality and Testability

The PAL24V10 offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, is verifies complete programmability and functionality of this device to yield the highest programming yields and post-programming function yields in the industry.

Technology

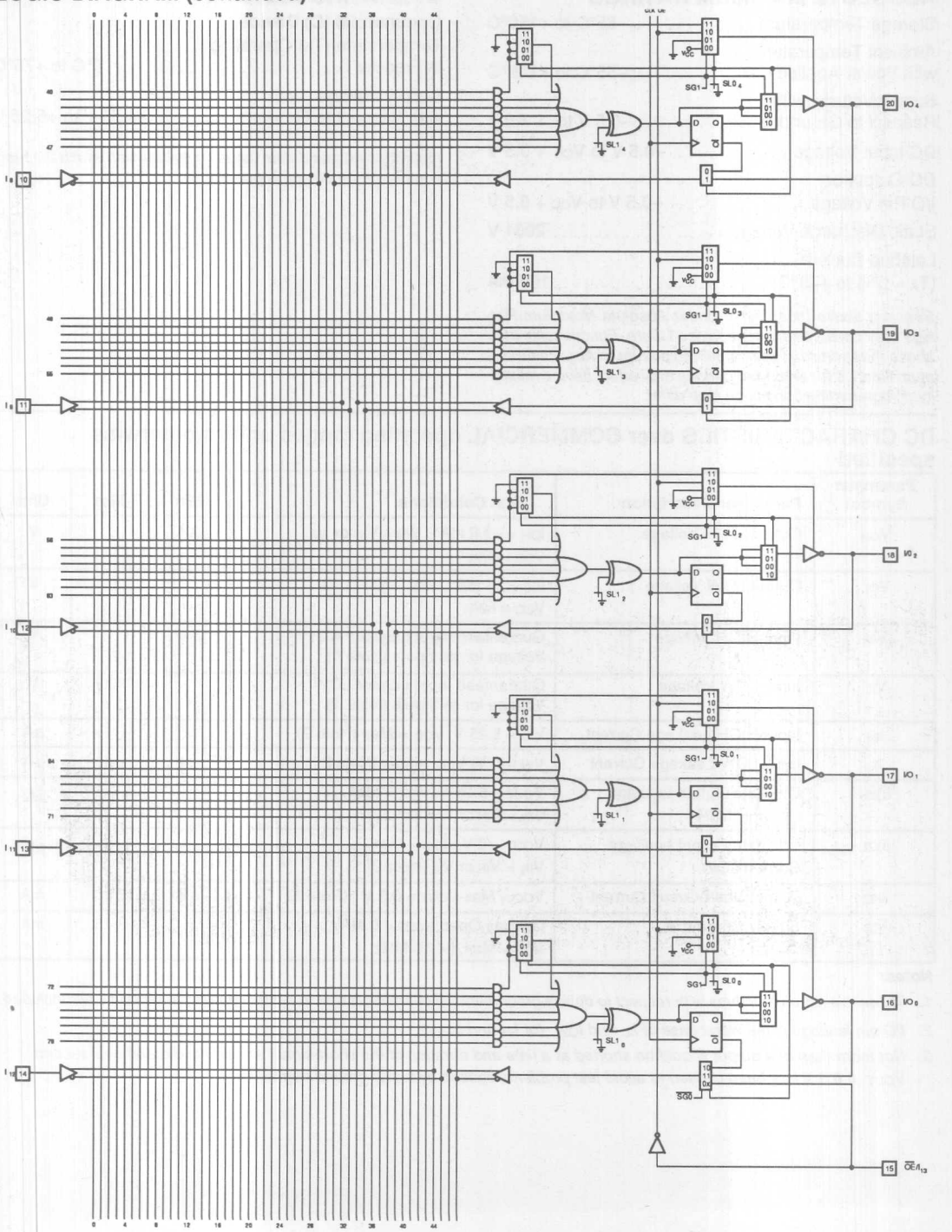
The high-speed PALCE24V10 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



12222E-6

LOGIC DIAGRAM (continued)



12222E-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to + 7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max V_{OUT} = 0.5 V (Note 3)	–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

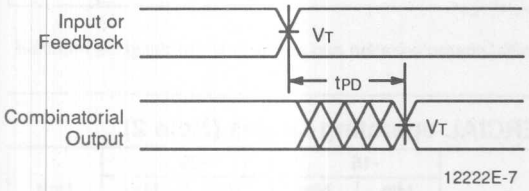
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min	-15 Max	-25 Min	-25 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			15		25		ns
t_S	Setup Time from Input or Feedback to Clock 10				12		ns	
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		6		8		ns
t_{WH}		HIGH		6		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	50		41.6		MHz
		Internal Feedback (f_{CNT})		66		50		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				15		25	ns

Notes:

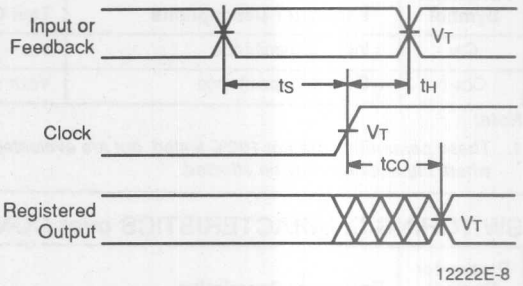
2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING WAVEFORMS



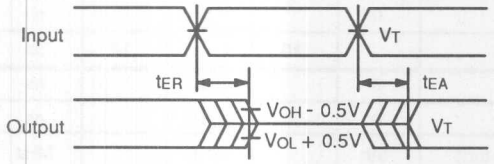
12222E-7

Combinatorial Output



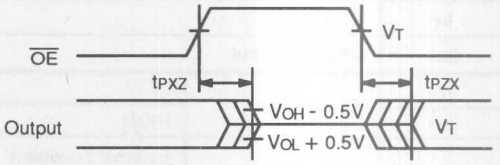
12222E-8

Registered Output



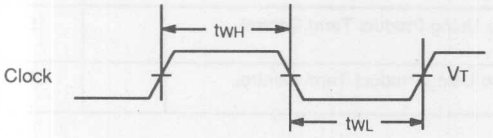
12222E-9

Input to Output Disable/Enable



12222E-10

$\overline{OE}$ to Output Disable/Enable



12222E-11

Clock Width

Notes:

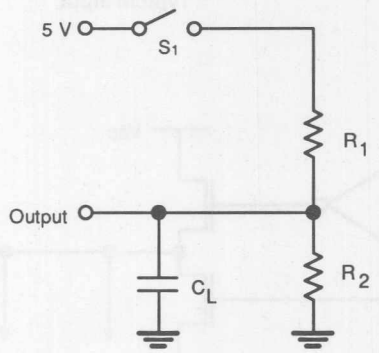
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12222E-12

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

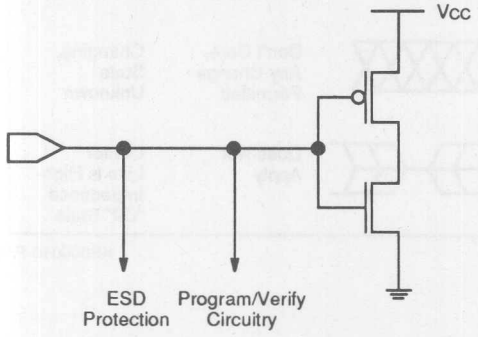
ENDURANCE CHARACTERISTICS

The PALCE24V10 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

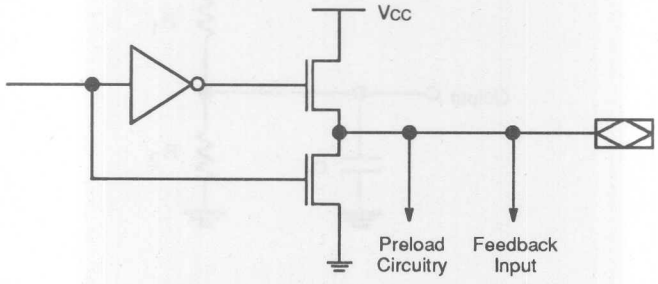
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

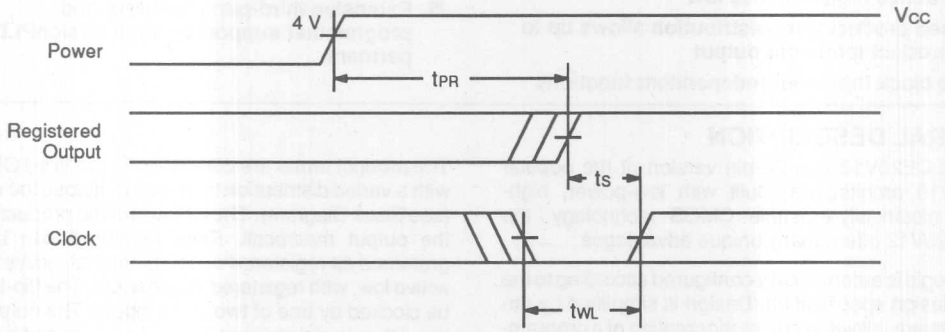
12222E-14

POWER-UP RESET

The PALCE24V10 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12222E-15

Power-Up Reset Waveform

PALCE26V12H-15/20

28-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 28-pin versatile PAL programmable logic device architecture
- Electrically erasable CMOS technology provides half power (only 105 mA) at high speed (15 ns propagation delay)
- 14 dedicated inputs and 12 input/output macrocells for architectural flexibility
- Macrocells can be registered or combinatorial, and active high or active low
- Varied product term distribution allows up to 16 product terms per output
- Two clock inputs for independent functions
- Global asynchronous reset and synchronous preset for initialization
- Register preload for testability and built-in register reset on power-up
- Space-efficient 28-pin SKINNYDIP and PLCC packages
- Center V_{CC} and GND pins to improve signal characteristics
- Extensive third-party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

The PALCE26V12 is a 28-pin version of the popular PAL22V10 architecture. Built with low-power, high-speed, electrically-erasable CMOS technology, the PALCE26V12 offers many unique advantages.

Device logic is automatically configured according to the user's design specification. Design is simplified by design software, allowing automatic creation of a programming file based on Boolean or state equations. The software can also be used to verify the design and can provide test vectors for the programmed device.

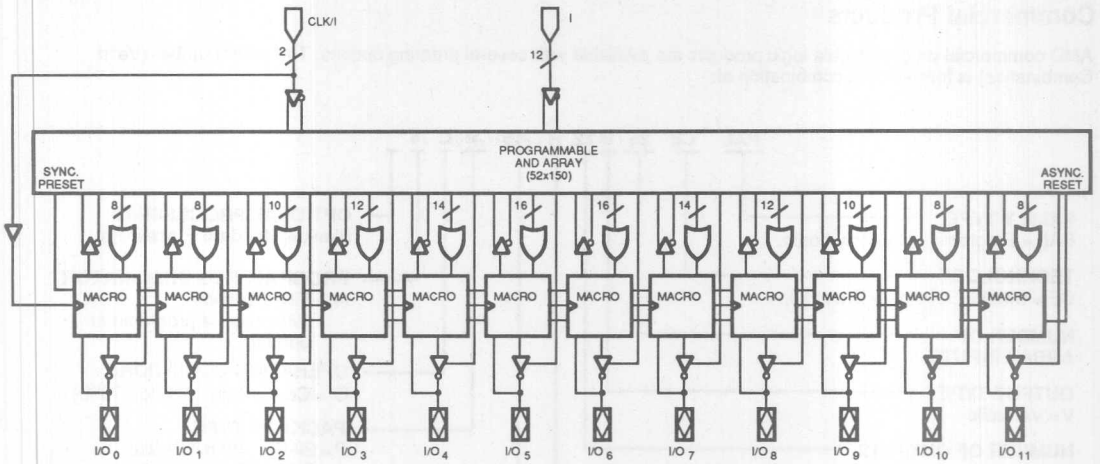
The PALCE26V12 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The functions are programmed into the device through electrically-erasable floating-gate cells in the AND logic array and the macrocells. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected, the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active high or active low, with registered I/O possible. The flip-flop can be clocked by one of two clock inputs. The output configuration is determined by four bits controlling three multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE26V12 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 16072 Rev. C Amendment /0
Issue Date: June 1993

BLOCK DIAGRAM

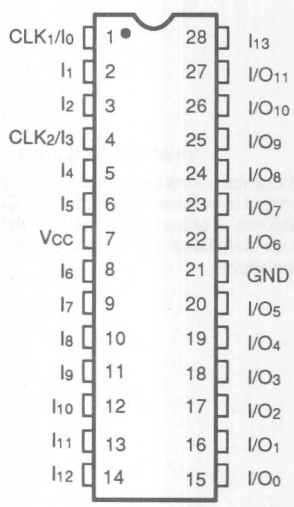


16072C-1

CONNECTION DIAGRAMS

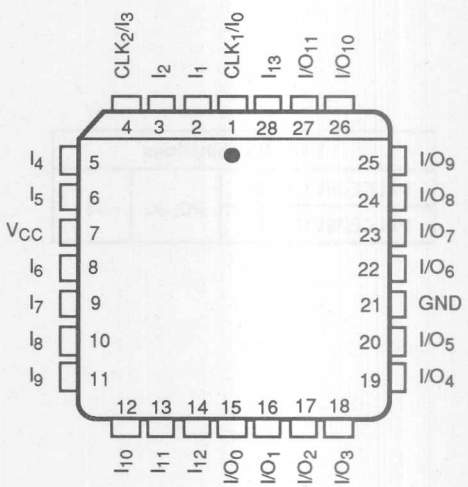
Top View

SKINNYDIP



16072C-2

PLCC



16072C-3

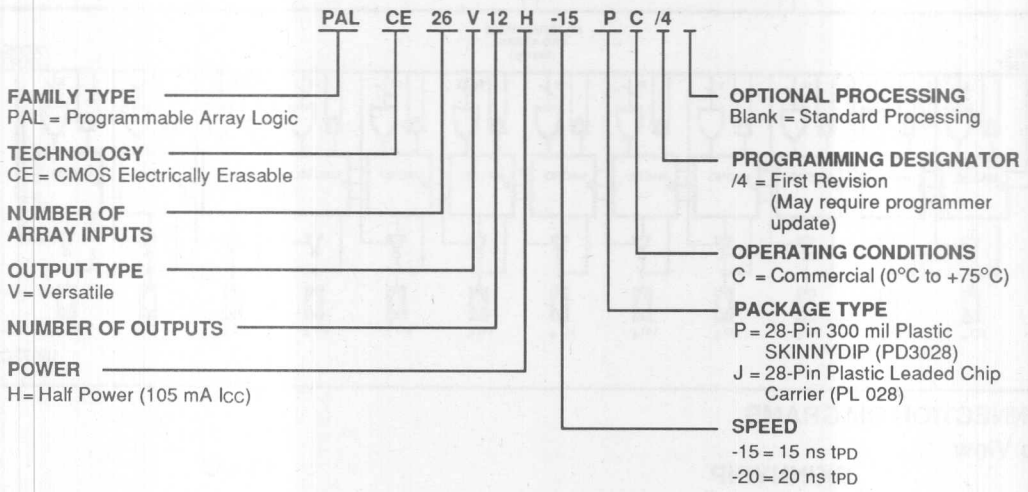
Note:
Pin 1 is marked for orientation.

PIN DESCRIPTION

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
Vcc = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE26V12H-15	PC, JC	/4
PALCE26V12H-20		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE26V12 has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or V_{CC}. Buffers for device inputs and feedbacks have both true and complementary outputs to provide user-selectable signal polarity. The inputs drive a programmable AND logic array, which feeds a fixed OR logic array.

The OR gates feed the twelve I/O macrocells (see Figure 1). The macrocell allows one of eight potential output configurations; registered or combinatorial, active high or active low, with register or I/O pin feedback (see Figure 2). In addition, registered configurations can be clocked by either of the two clock inputs.

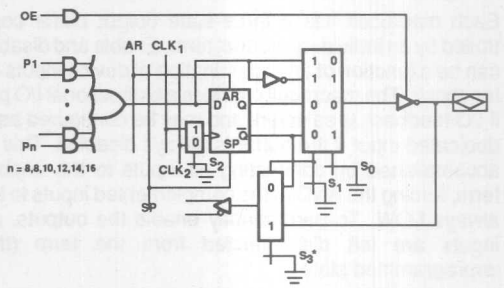
The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0–S_3 (see Table 1). Multiplexer controls initially float to V_{CC} (1) through a programmable cell, selecting the "1" path through the multiplexer. Programming the cell connects the control line to GND (0), selecting the "0" path.

Table 1. Macrocell Configuration Table

S_3	S_1	S_0	Output Configuration
1	0	0	Registered Output and Feedback, Active Low
1	0	1	Registered Output and Feedback, Active High
1	1	0	Combinatorial I/O, Active Low
1	1	1	Combinatorial I/O, Active High
0	0	0	Registered I/O, Active Low
0	0	1	Registered I/O, Active High
0	1	0	Combinatorial Output, Registered Feedback, Active Low
0	1	1	Combinatorial Output, Registered Feedback, Active High

1 = Unprogrammed EE bit
0 = Programmed EE bit

S_2	Clock Input
1	CLK_1/I_0
0	CLK_2/I_3



**When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.*

16072C-4

Figure 1. PALCE26V12 Macrocell

Registered or Combinatorial

Each macrocell of the PALCE26V12 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the selected clock input. Any macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S_1.

Programmable Clock

The clock input for any flip-flop can be selected to be from either pin 1 or pin 4. A 2:1 multiplexer controlled by bit S_2 determines the clock input.

Programmable Feedback

A 2:1 multiplexer allows the user to determine whether the macrocell feedback comes from the flip-flop or from the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal register feedback for higher speed (f_{MAX} internal), or I/O feedback for use of the pin as a direct input (f_{MAX} external). Combinatorial outputs may have I/O feedback, either for use of the signal in other equations or for use as another direct input, or register feedback.

The feedback multiplexer is controlled by the same bit (S_1) that controls whether the output is registered or combinatorial, as on the 22V10, with an additional control bit (S_3) that allows the alternative feedback path to be selected. When S_3 = 1, S_1 selects register feedback for registered outputs (S_1 = 0) and I/O feedback for combinatorial outputs (S_1 = 1). When S_3 = 0, the opposite is selected: I/O feedback for registered outputs and register feedback for combinatorial outputs.

Programmable Enable and I/O

Each macrocell has a three-state output buffer controlled by an individual product term. Enable and disable can be a function of any combination of device inputs or feedback. The macrocell provides a bidirectional I/O pin if I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting all inputs to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all inputs are left disconnected from the term (the unprogrammed state).

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high.

Preset/Reset

For initialization, the PALCE26V12 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH or the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE26V12 will be HIGH or LOW depending on whether the output is active low or active high, respectively. The V_{CC} rise must be monotonic, and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE26V12 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE26V12 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. Programming the security bit disables preload, and the array will read as if every bit is disconnected. The security bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

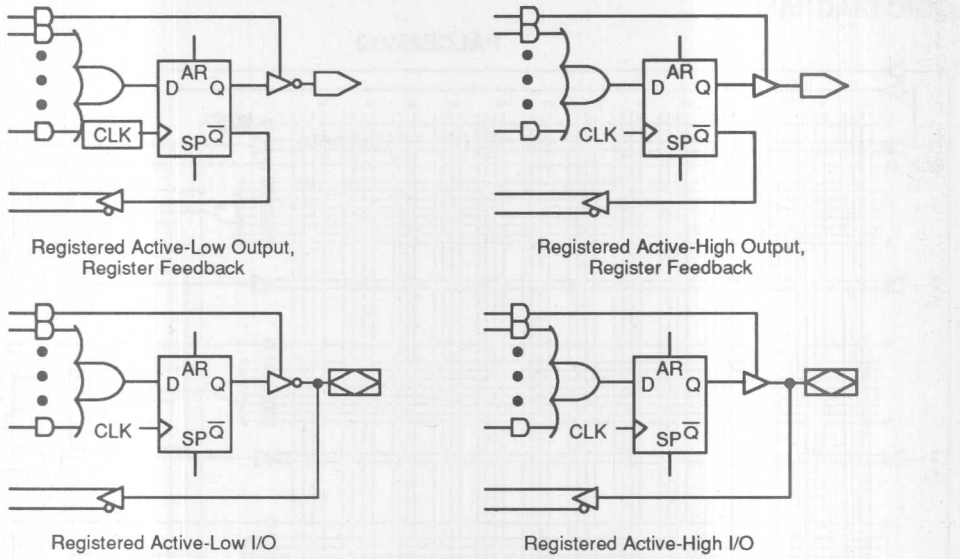
The PALCE26V12 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

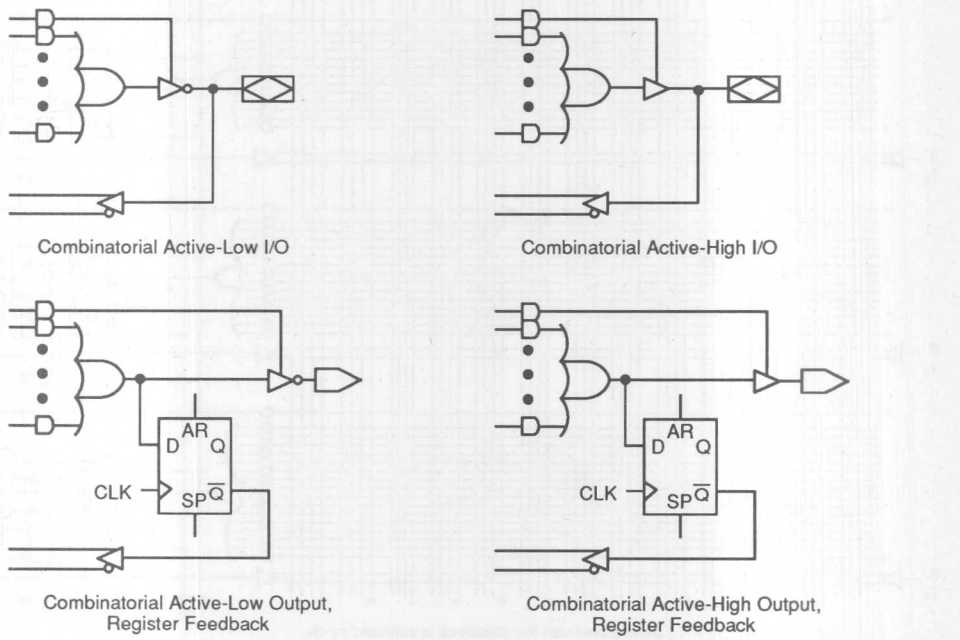
The PALCE26V12 offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE26V12 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.



Registered Outputs

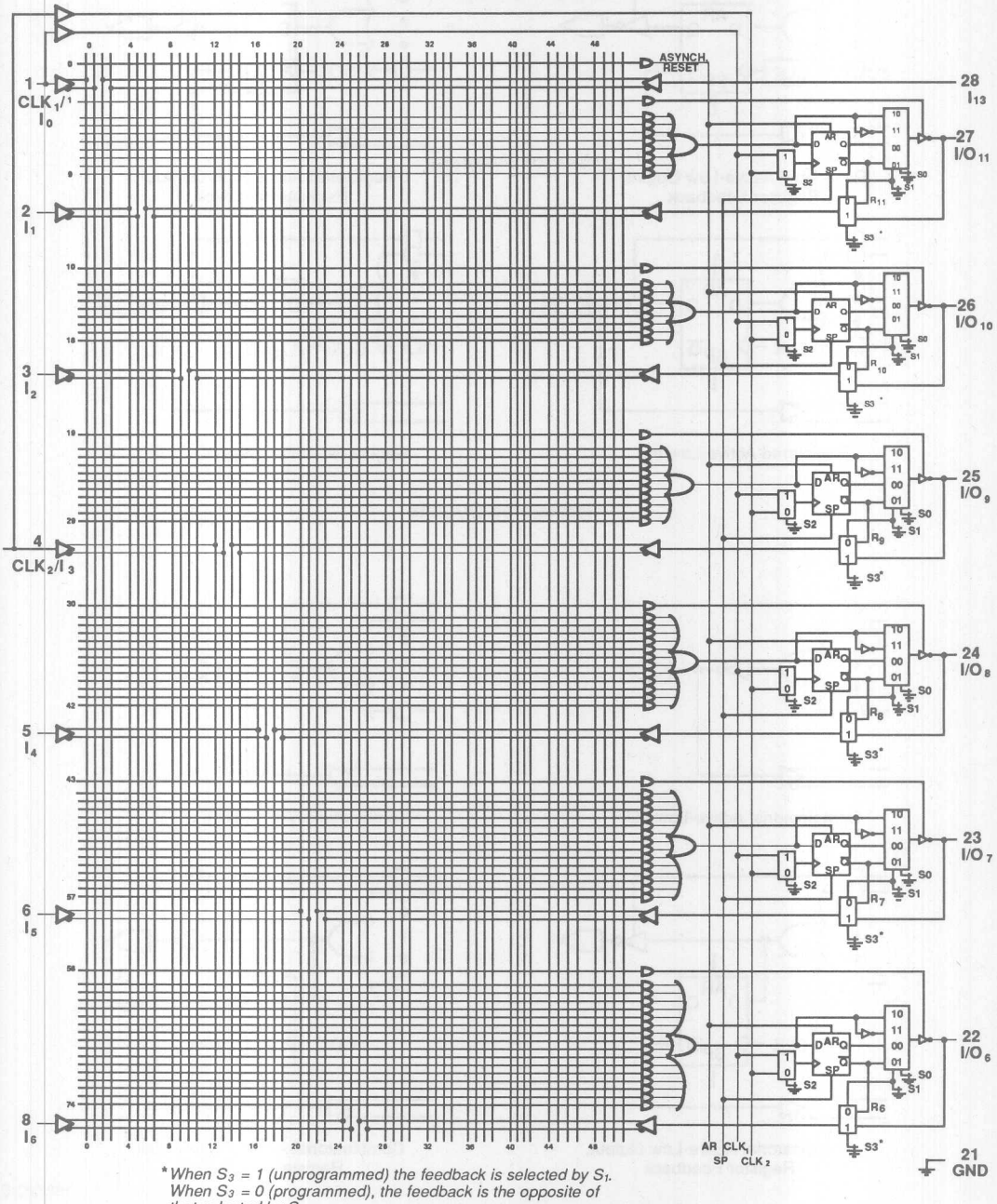


Combinatorial Outputs

Figure 2. PALCE26V12 Macrocell Configuration Options

LOGIC DIAGRAM

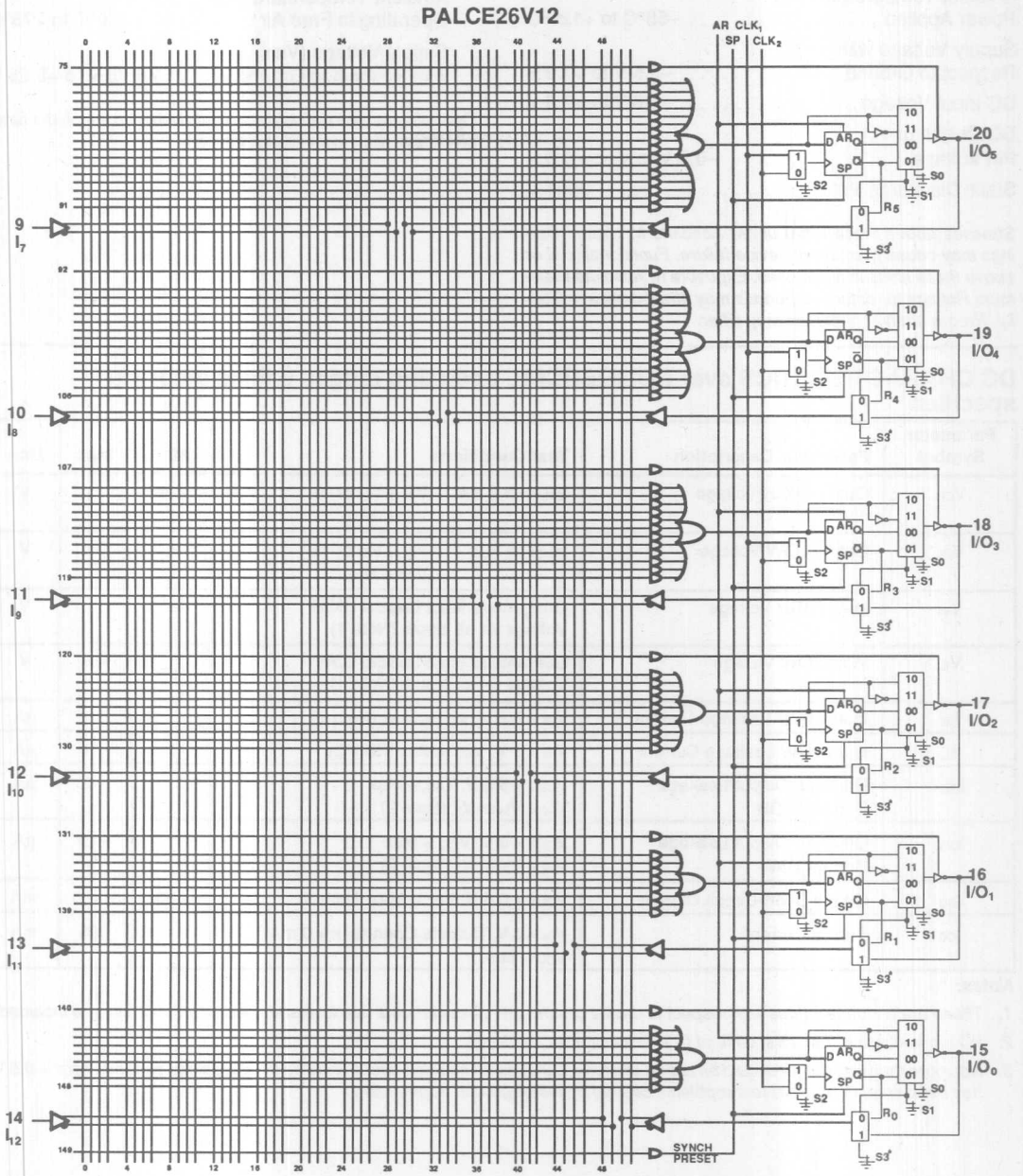
PALCE26V12



*When S_3 = 1 (unprogrammed) the feedback is selected by S_1.
When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

16072C-6

LOGIC DIAGRAM (continued)



* When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

16072C-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.6 V to +7.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		105	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

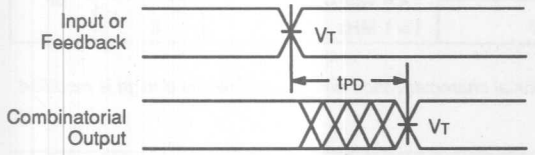
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		20	ns
t_S	Setup Time from Input, Feedback, or SP to Clock			10		13		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time			15		20		ns
t_{SPR}	Synchronous Preset Recovery Time			10		13		ns
t_{WL}	Clock Width	LOW		8		10		ns
t_{WH}		HIGH		8		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		40		MHz
		Internal Feedback (f_{CNT})		58.8		43		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		20	ns

Notes:

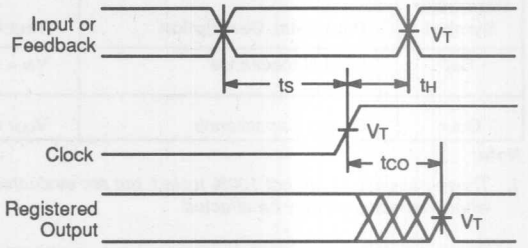
2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING WAVEFORMS



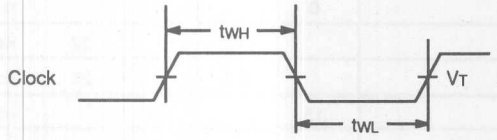
16072C-7

Combinatorial Output



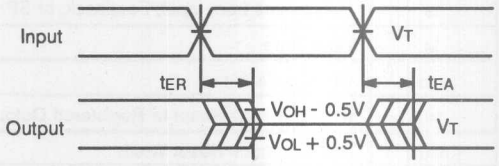
16072C-8

Registered Output



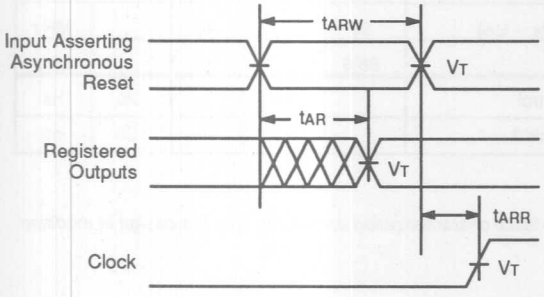
16072C-9

Clock Width



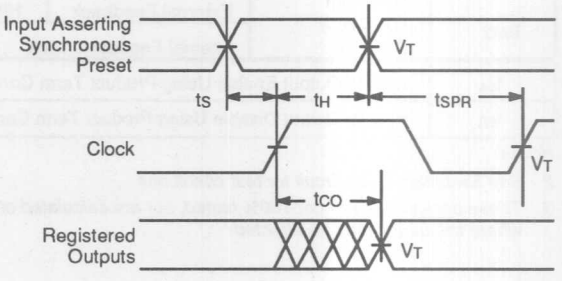
16072C-10

Input to Output Disable/Enable



16072C-11

Asynchronous Reset



16072C-12

Synchronous Preset

Notes:

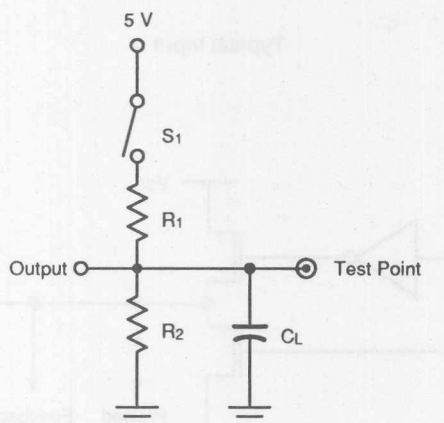
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



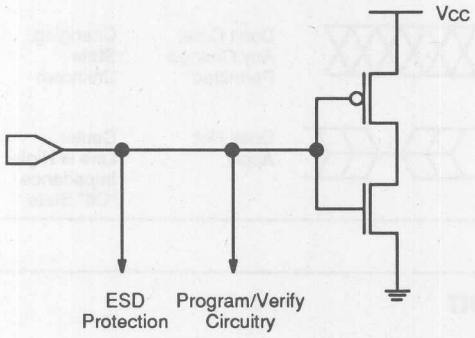
16072C-13

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

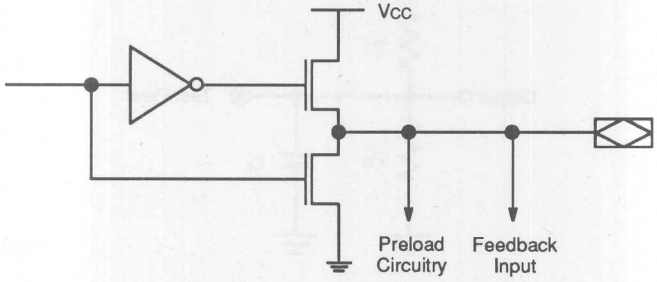
uses an EE cell to replace the fuse link used in bipolar the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



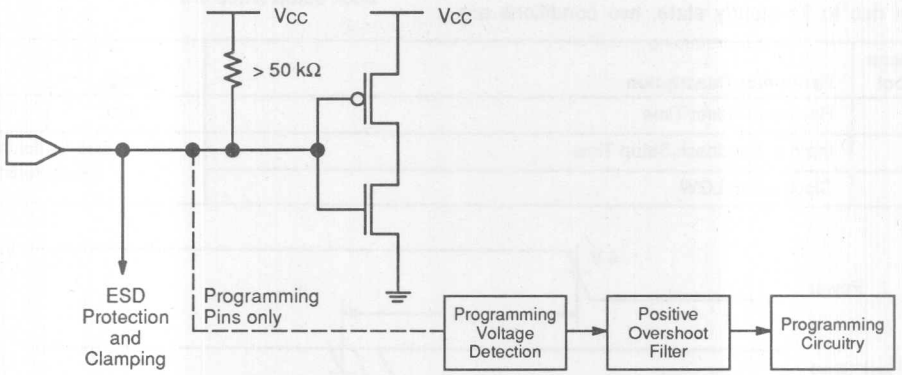
Typical Output

16072C-15

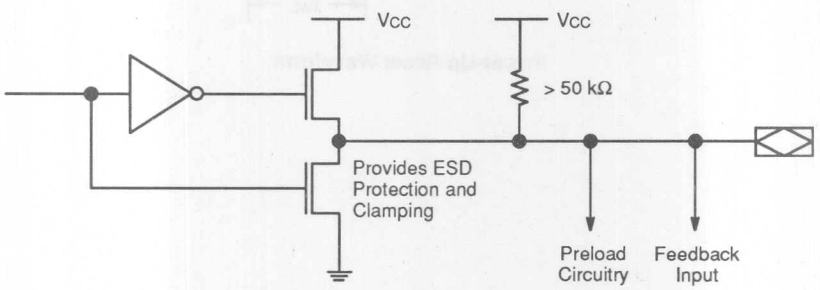
ROBUSTNESS FEATURES

The PALCE26V12H-15/20 Rev. B has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR REV. B VERSION



Typical Input



Typical Output

16072C-15

Device	Rev. Letter
PALCE26V12H-15	B
PALCE26V12H-20	B

Topside Marking:

AMD CMOS PLD's are marked on top of the package in the following manner:

PALCE xxxx

Datecode (3 numbers) LOT ID (4 characters) – – (Rev. Letter)

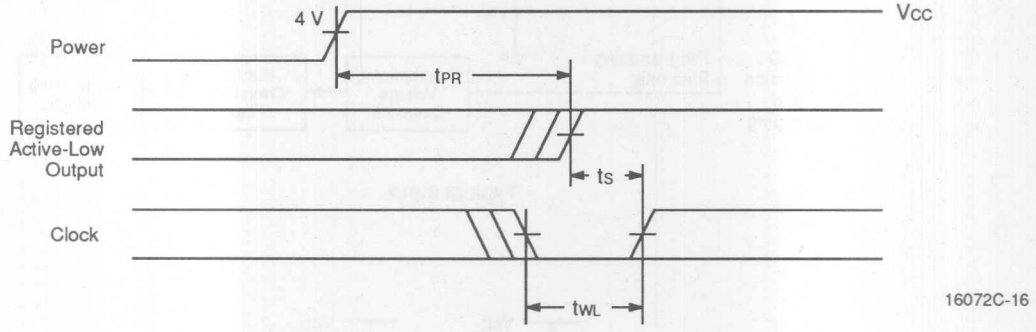
The Lot ID and Rev. letter are separated by two spaces.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

PALCE26V12-15

Parameter Symbol	Parameter Description		Typ. SKINNYDIP	Typ. PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		19	18	°C/W
θ_{ja}	Thermal impedance, junction to ambient		65	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	59	48	°C/W
		400 lfpm air	54	44	°C/W
		600 lfpm air	50	39	°C/W
		800 lfpm air	50	37	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.


IMPORTANT
NOTES

PALCE29M16H-25

24-Pin EE CMOS Programmable Array Logic

Advanced Micro Devices

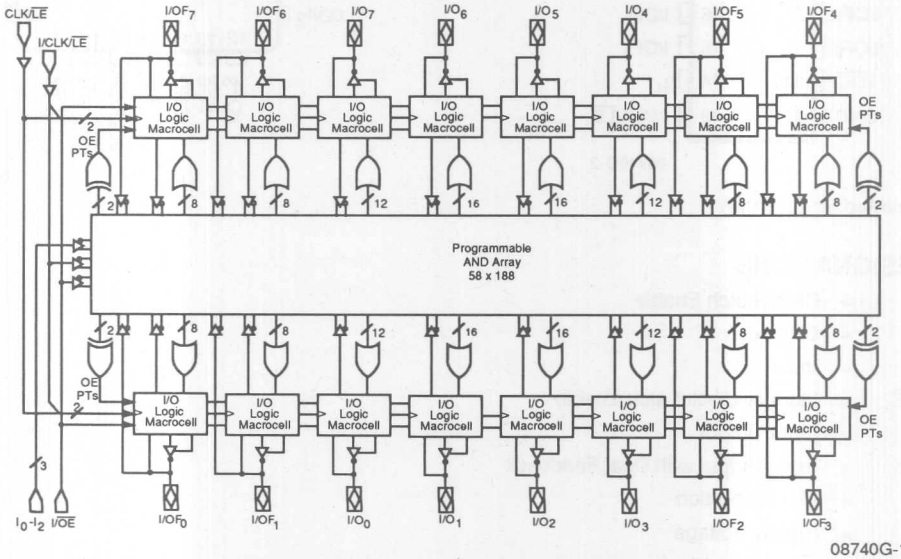
DISTINCTIVE CHARACTERISTICS

- High-performance semicustom logic replacement; Electrically Erasable (EE) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/ Latched operation
- Output Enable controlled by a pin or product terms
- Varied product term distribution for increased design flexibility
- Programmable clock selection with two clocks/ latch enables ($\overline{LE}$s) and LOW/HIGH clock/$\overline{LE}$ polarity
- Register/Latch Preload permits full logic verification
- High speed (t_{PD} = 25 ns, f_{MAX} = 33 MHz and f_{MAX} internal = 50 MHz)
- Full-function AC and DC testing at the factory for high programming and functional yields and high reliability
- 24-Pin 300 mil SKINNYDIP and 28-pin plastic leaded chip carrier packages
- Extensive third-party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

The PALCE29M16 is a high-speed, EE CMOS Programmable Array Logic (PAL) device designed for general logic replacement in TTL or CMOS digital systems. It offers high speed, low power consumption, high programming yield, fast programming and excellent reliability. PAL devices combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

BLOCK DIAGRAM



08740G-1

functions by programming the device for specific applications. It provides up to 29 array inputs and 16 outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as combinatorial, registered, or latched with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PALCE29M16 by providing a varied number of logic product terms per output. Eight outputs have 8 product terms each, four outputs have 12 product terms each, functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or Output Enable product terms per bank of four outputs. Each output can also be permanently enabled or disabled.

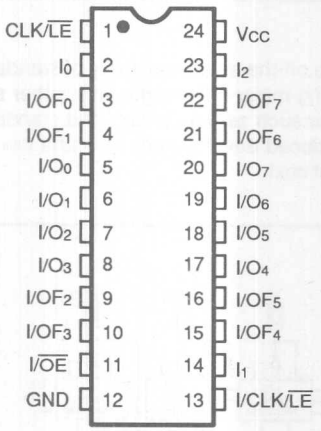
System operation has been enhanced by the addition of common asynchronous-Preset and Reset product terms and a power-up Reset feature. The PALCE29M16 also incorporates Preload and Observability functions which permit full logic verification of the design.

The PALCE29M16 is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

CONNECTION DIAGRAMS

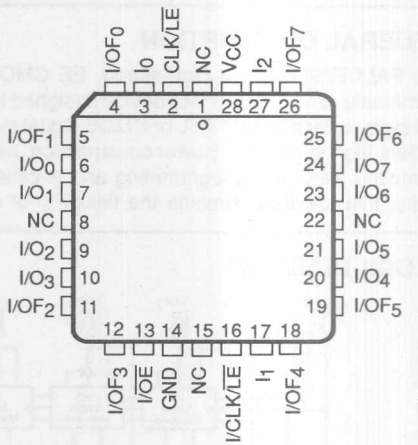
Top View

SKINNYDIP



08740G-2

PLCC



08740G-3

Note:
Pin 1 is marked for orientation.

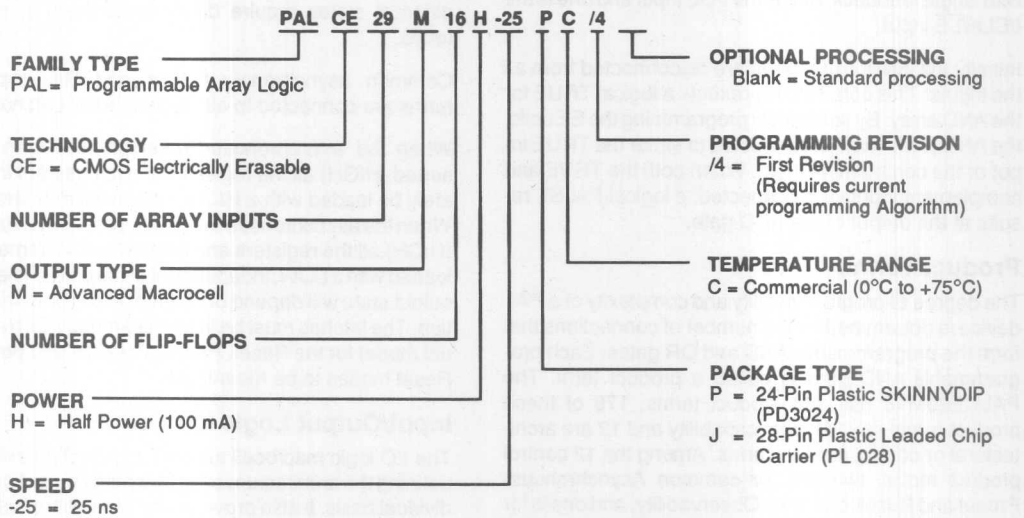
PIN DESIGNATIONS

CLK/$\overline{LE}$	=	Clock/Latch Enable
GND	=	Ground
I	=	Input
I/CLK/$\overline{LE}$	=	Input or Clock/Latch Enable
I/O	=	Input/Output
I/OF	=	Input/Output with Dual Feedback
NC	=	No Connection
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE29M16H-25	PC, JC	/4

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Inputs

The PALCE29M16 has 29 inputs to drive each product term (up to 58 inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these 29 inputs, 3 are dedicated inputs, 16 are from 8 I/O logic macrocells with two feedbacks, 8 are from other I/O logic macrocells with single feedback, one is the I/$\overline{OE}$ input and one is the I/CLK/$\overline{LE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the EE cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29M16 has 188 product terms; 176 of these product terms provide logic capability and 12 are architectural or control product terms. Among the 12 control product terms, two are for common Asynchronous-Preset and Reset, one is for Observability, and one is for Preload. The other eight are common Output Enable product terms. The Output Enable of each bank of four macrocells can be programmed to be controlled by a common Output Enable pin or two AND/XOR product terms. It may be also permanently enabled or permanently disabled.

Each product term on the PALCE29M16 consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from 8 to 16 wide, with an average of 11 logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Common asynchronous-Preset and Reset product terms are connected to all Registered or Latched I/Os.

When the asynchronous-Preset product term is asserted (HIGH) all the registers and latches will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-Reset product term is asserted (HIGH) all the registers and latches will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the Reset, Preset, Preload, and power-up Reset modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29M16 has 16 macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers and Latches are used in synchronous logic applications.

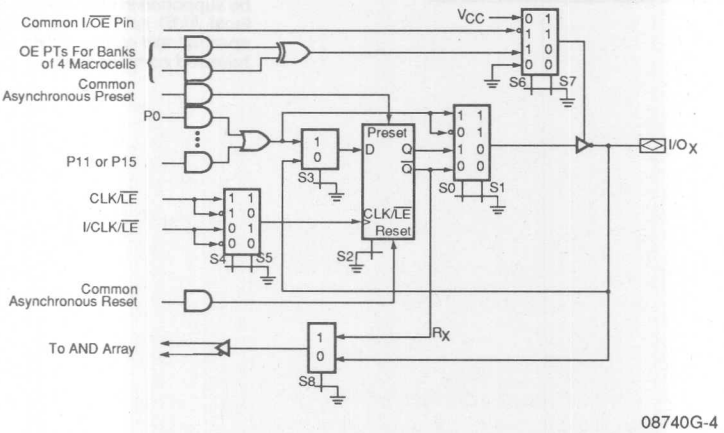


Figure 2a. PALCE29M16 Macrocell (Single Feedback)

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0–I/OF_7) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the signal generated by the AND-OR array or the I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29M16H has a dedicated CLK/$\overline{LE}$ pin and an I/CLK/$\overline{LE}$ pin. All macrocells have a programmable switch to choose between these two pins as the clock or latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers or latches can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by two AND-XOR product terms which are available for each bank of four I/O Logic Macrocells.

I/O Logic Macrocell Configuration

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain 9 EE cells, while the other eight macrocells contain 8 EE cells for programming the input/output functions (see Table 1).

EE cell S_1 controls whether the macrocell will be combinatorial or registered/latched. S_0 controls the output polarity (active-HIGH or active-LOW). S_2 determines whether the storage element is a register or a latch. S_3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable EE cells S_4 and S_5 allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. S_6 and S_7 are used to control Output Enable as pin controlled, two-product-term-controlled, permanently enabled or permanently disabled. S_8 controls a feedback multiplexer for the macrocells with a single feedback path only.

Using the programmable EE cells S_0–S_8 various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the unprogrammed state (charged, disconnected), an architectural cell is said to have a value of "1"; in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of "0."

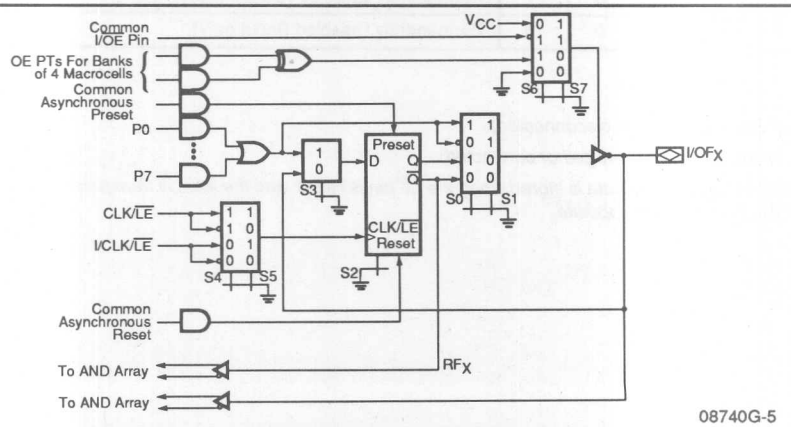


Figure 2b. PALCE29M16 Macrocell (Dual Feedback)

Table 1a. PALCE29M16 I/O Logic Macrocell Architecture Selections

S_3	I/O Cell
1	Output Cell
0	Input Cell

S_2	Storage Element
1	Register
0	Latch

S_1	Output Type
1	Combinatorial
0	Register/Latch

S_0	Output Polarity
1	Active LOW
0	Active HIGH

S_8	Feedback*
1	Register/Latch
0	I/O

**Applies to macrocells with single feedback only.*

Table 1b. PALCE29M16 I/O Logic Macrocell Clock Polarity and Output Enable Selections

S_4	S_5	Clock Edge/Latch Enable Level
1	1	CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
1	0	CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE
0	1	I/CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
0	0	I/CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE

S_6	S_7	Output Buffer Control
1	1	Pin-Controlled Three-State Enable
1	0	XOR PT-Controlled Three-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

Notes:

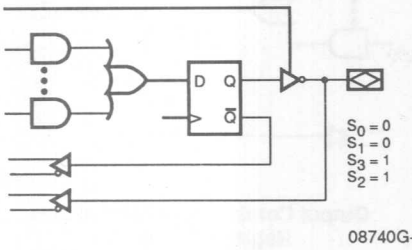
1 = Erased State (charged or disconnected).

0 = Programmed State (discharged or connected).

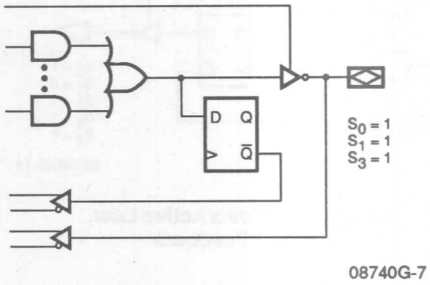
**Active-LOW LE means that data is stored when the $\overline{LE}$ pin is HIGH, and the latch is transparent when the $\overline{LE}$ pin is LOW. Active-HIGH LE means the opposite.*

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

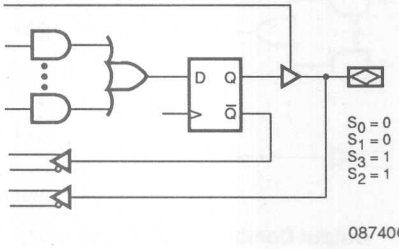
(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable).



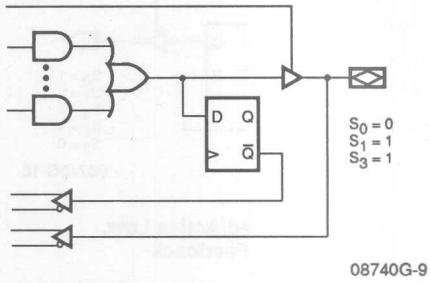
Output Registered/Active Low



Output Combinatorial/Active Low

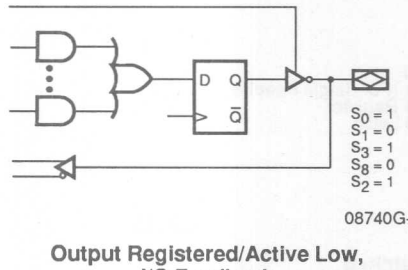


Output Registered/Active High

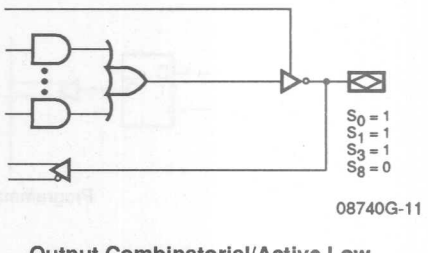


Output Combinatorial/Active High

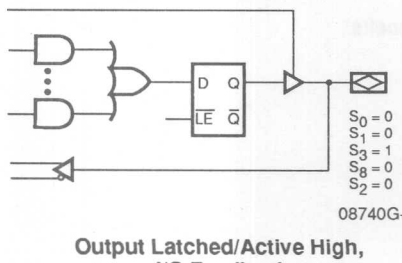
Figure 3a. Dual Feedback Macrocells



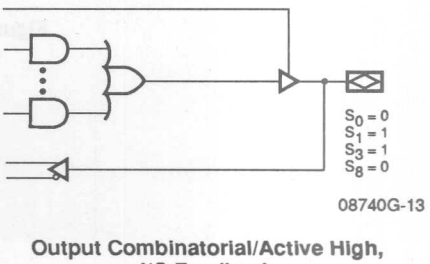
Output Registered/Active Low, I/O Feedback



Output Combinatorial/Active Low, I/O Feedback



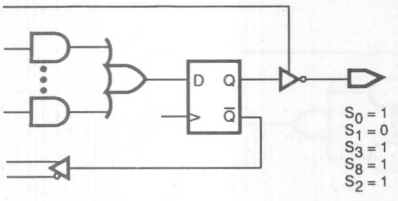
Output Latched/Active High, I/O Feedback



Output Combinatorial/Active High, I/O Feedback

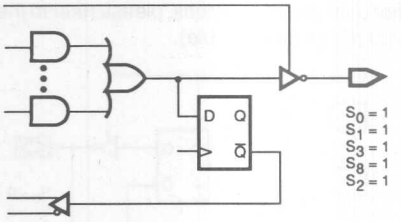
Figure 3b. Single Feedback Macrocells

POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL



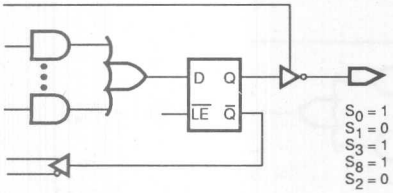
08740G-14

Output Registered/Active Low, Register Feedback



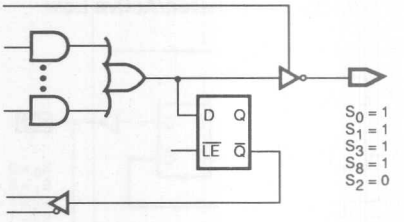
08740G-15

Output Combinatorial/Active Low, Register Feedback



08740G-16

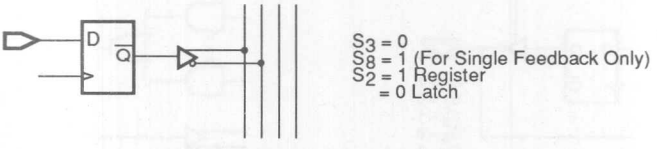
Output Latched/Active Low, Latched Feedback



08740G-17

Output Combinatorial/Active Low, Latched Feedback

Figure 3b. Single Feedback Macrocells (continued)



08740G-18

Input Registered/Latched

Figure 3c. All Macrocells

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. The outputs of the PALCE29M16 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW if programmed as active LOW and HIGH if programmed as active HIGH. If combinatorial is selected, the output will be a function of the logic.

Preload

To simplify testing, the PALCE29M16 is designed with preload circuitry that provides an easy method for testing logical functionality. Both product-term-controlled and supervoltage-enabled preload modes are available. The TTL-level preload product term can be useful during debugging, where supervoltages may not be available.

Preload allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into an arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way any transition can be checked.

Since preload can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, preload, and the observability modes. The only way to erase the protection cell is by erasing the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

Programming and Erasing

The PALCE29M16 can be programmed on standard logic programmers. It may also be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erasure operation is required.

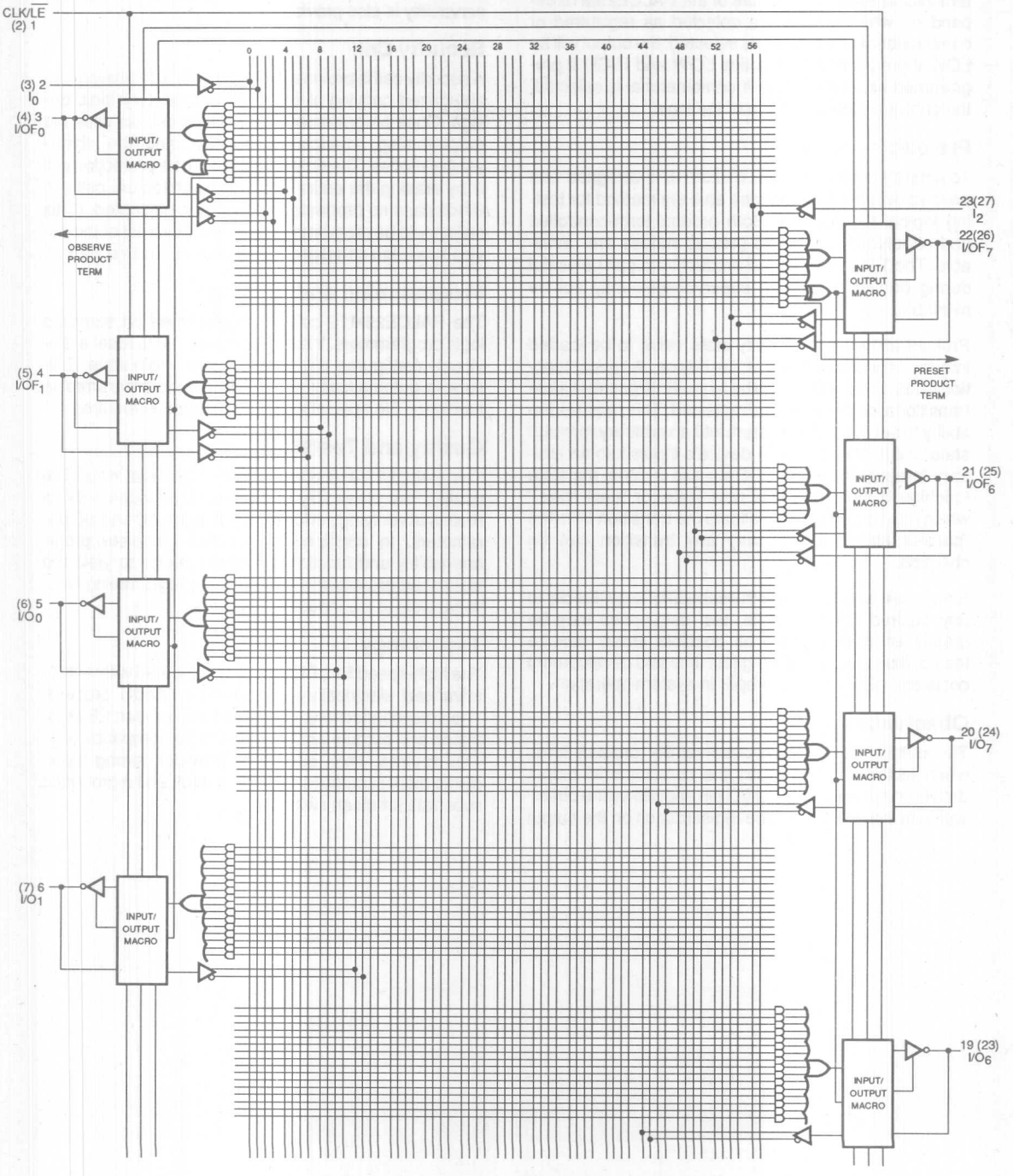
Quality and Testability

The PALCE29M16 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yield and post-programming functional yield in the industry.

Technology

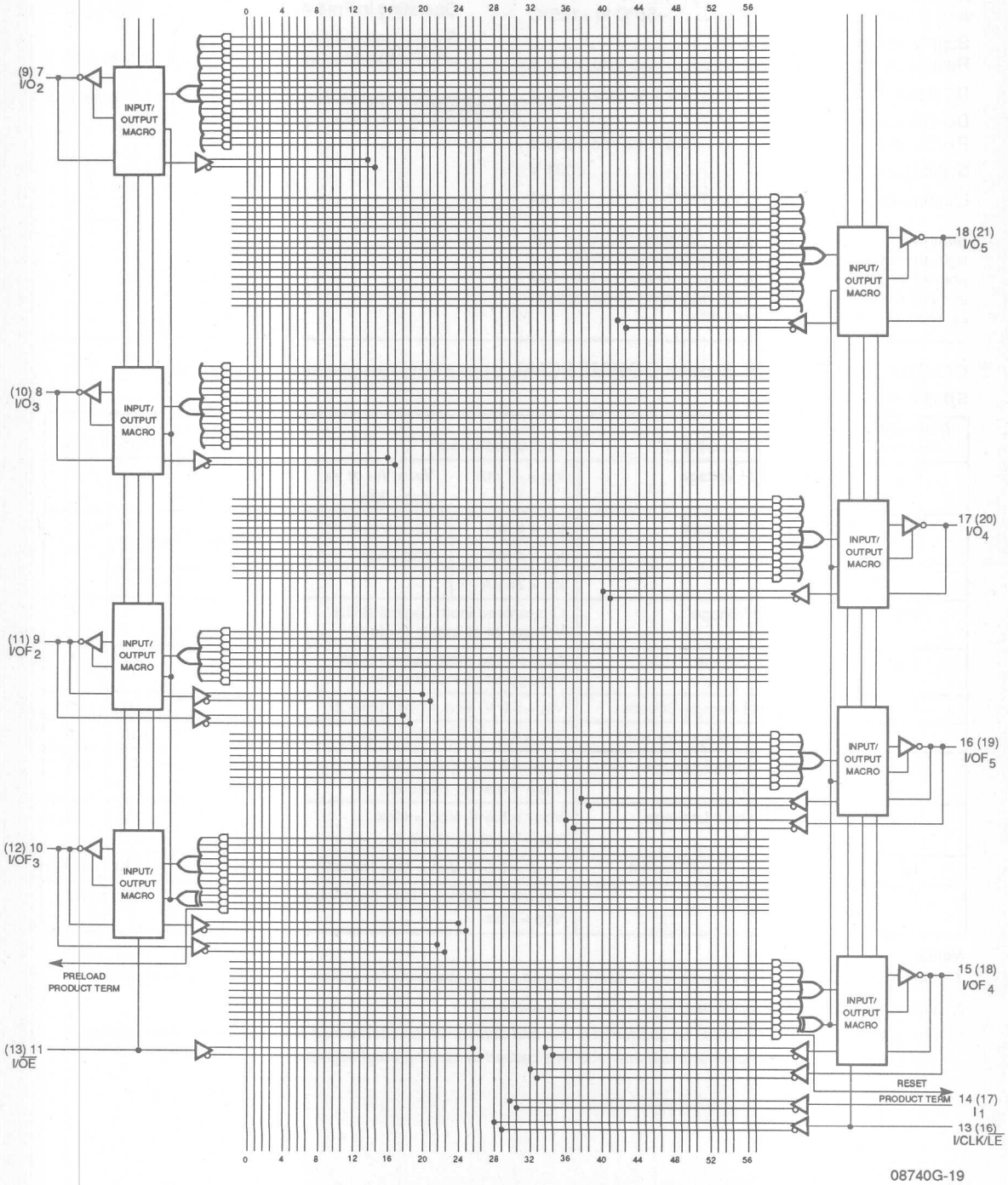
The high-speed PALCE29M16 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
DIP (PLCC) Pinouts



08740G-19

LOGIC DIAGRAM
DIP (PLCC) Pinouts



08740G-19
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . 4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.5	V
		I_{OL} = 4 mA			0.33	
		I_{OL} = 20 µA			0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max			100	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	pF

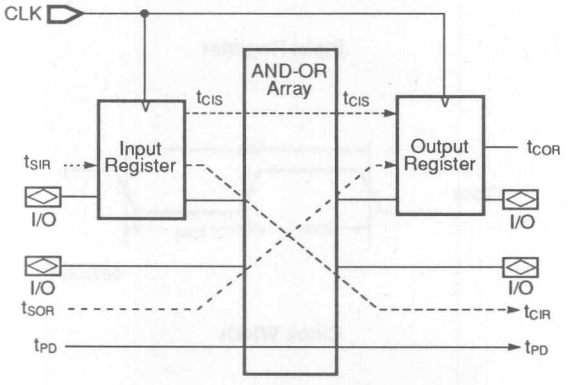
Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS

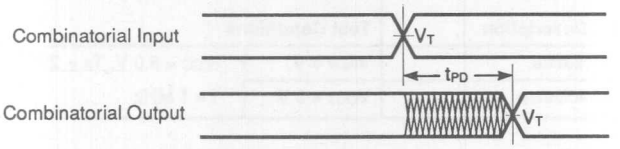
Registered Operation

Parameter Symbol	Parameter Description	Min	Max	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
Output Register				
t_{SOR}	Input or I/O Pin to Output Register Setup	15		ns
t_{COR}	Output Register Clock to Output		15	ns
t_{HOR}	Data Hold Time for Output Register	0		ns
Input Register				
t_{SIR}	I/O Pin to Input Register Setup	2		ns
t_{CIR}	Register Feedback Clock to Combinatorial Output		28	ns
t_{HIR}	Data Hold Time for Input Register	6		ns
Clock and Frequency				
t_{CIS}	Register Feedback to Output Register/Latch Setup	20		ns
f_{MAX}	Maximum Frequency 1/(t_{SOR} + t_{COR})	33.3		MHz
f_{MAXI}	Maximum Internal Frequency 1/t_{CIS}	50		MHz
t_{CWH}	Pin Clock Width HIGH	8		ns
t_{CWL}	Pin Clock Width LOW	8		ns



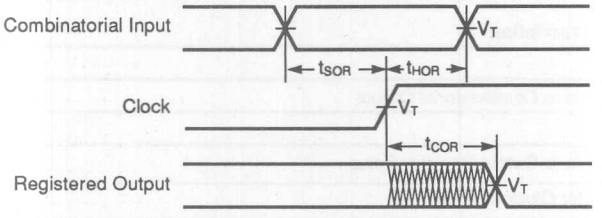
08740G-20

SWITCHING WAVEFORMS



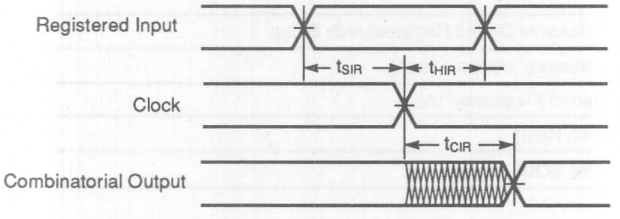
08740G-21

Combinatorial Output



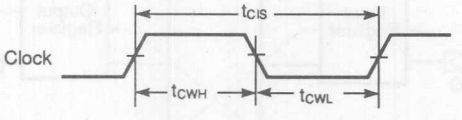
08740G-22

Output Register



08740G-23

Input Register



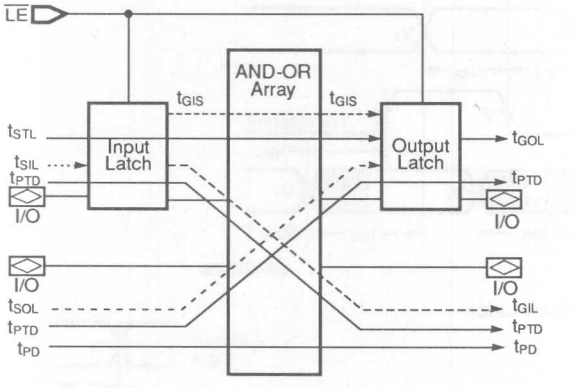
08740G-24

Clock Width

SWITCHING CHARACTERISTICS

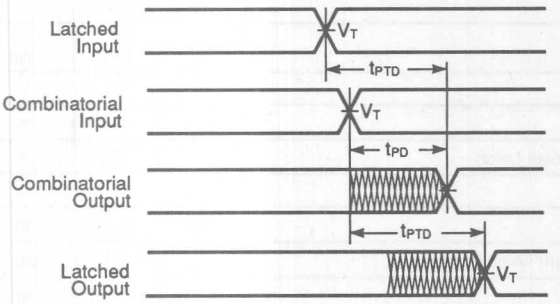
Latched Operation

Parameter Symbol	Parameter Description	Min	Max	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
t_{PTD}	Input or I/O Pin to Output via One Transparent Latch		28	ns
Output Latch				
t_{SOL}	Input or I/O Pin to Output Latch Setup	15		ns
t_{GOL}	Latch Enable to Output Through Transparent Output Latch		15	ns
t_{HOL}	Data Hold Time for Output Latch	0		ns
t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	18		ns
Input Latch				
t_{SIL}	I/O Pin to Input Latch Setup	2		ns
t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		28	ns
t_{HIL}	Data Hold Time for Input Latch	6		ns
Latch Enable				
t_{GIS}	Latch Feedback to Output Register/Latch Setup	20		ns
t_{GWH}	Pin Enable Width HIGH	8		ns
t_{GWL}	Pin Enable Width LOW	8		ns



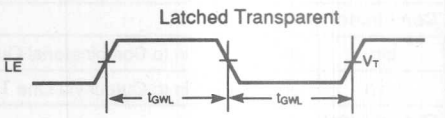
Input/Output Latch Specs

SWITCHING WAVEFORMS



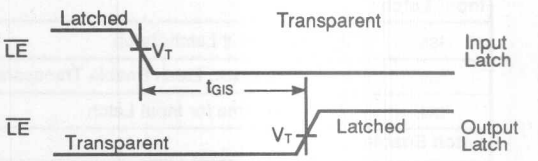
08740G-26

Latch (Transparent Mode)



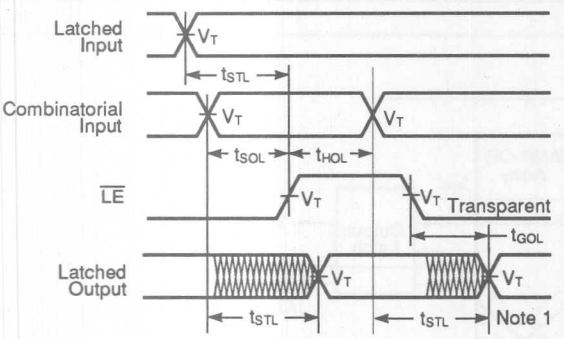
08740G-27

$\overline{LE}$ Width



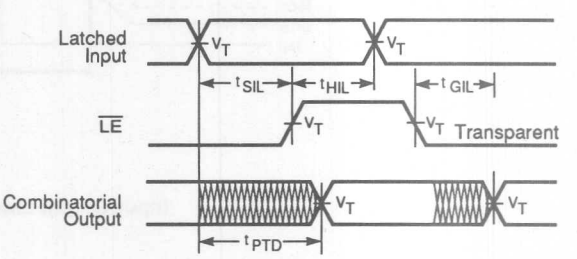
08740G-29

Input and Output Latch Relationship



08740G-28

Output Latch



08740G-30

Input Latch

Note:

1. *If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode after t_{PTD} ns has elapsed, the corresponding latched output will change t_{GOL} ns after $\overline{LE}$ goes into the transparent mode. If the combinatorial input change while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode before t_{PTD} ns has elapsed, the corresponding latched output will change at the later of the following—t_{PTD} ns after the combinatorial input changes or t_{GOL} ns after $\overline{LE}$ goes into the latched mode.*

SWITCHING CHARACTERISTICS

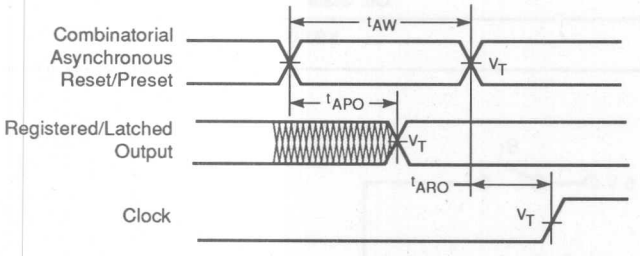
Reset/Preset, Enable

Parameter Symbol	Parameter Description	Min	Max	Unit
Combinatorial Output				
t_{APO}	Input or I/O Pin to Output Register/Latch Reset/Preset		30	ns
t_{AW}	Asynchronous Reset/Preset Pulse Width	15		ns
t_{ARO}	Asynchronous Reset/Preset to Output Register/Latch Recovery	15		ns
t_{ARI}	Asynchronous Reset/Preset to Input Register/Latch Recovery	12		ns
Output Enable Operation				
t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		20	ns
t_{PXZ}	I/$\overline{OE}$ Pin to Output Disable (Note 1)		20	ns
t_{EA}	Input or I/O to Output Enable via PT		25	ns
t_{ER}	Input or I/O to Output Disable via PT (Note 1)		25	ns

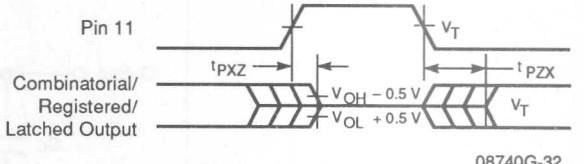
Note:

1. Output disable times do not include test load RC time constants.

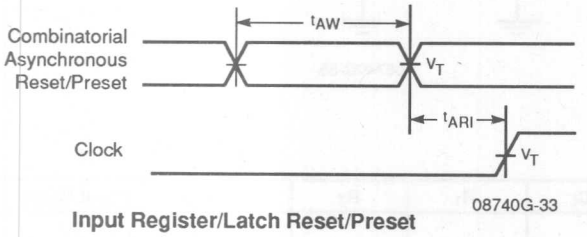
SWITCHING WAVEFORMS



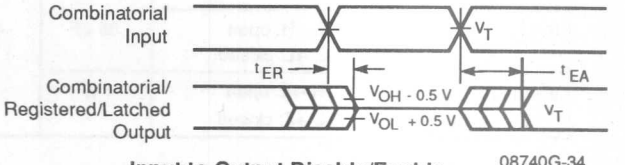
Output Register/Latch Reset/Preset



Pin 11 to Output Disable/Enable



Input Register/Latch Reset/Preset



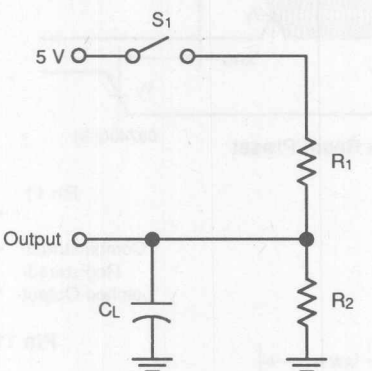
Input to Output Disable/Enable

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING TEST CIRCUIT



08740G-35

Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{GOL}	Closed	35 pF	470 Ω	390 Ω	1.5 V
t_{EA}, t_{PZX}	Z→H: open Z→L: closed				1.5 V
t_{ER}, t_{PXZ}	H→Z: open L→Z: closed	5 pF			H→Z: V_{OH} –0.5 V L→Z: V_{OL} +0.5 V

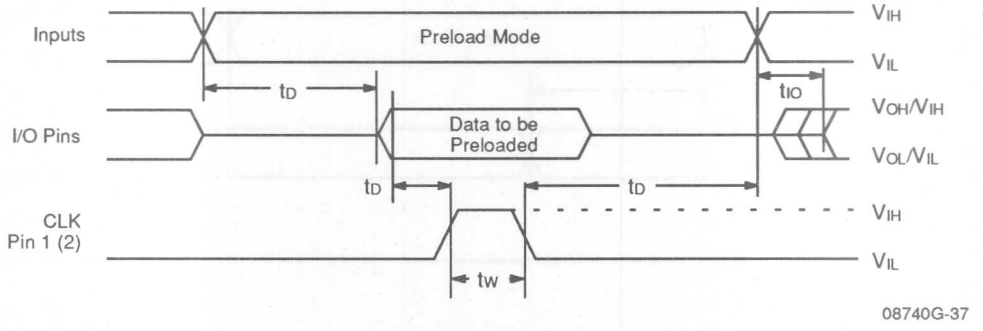
PRELOAD

The PALCE29M16 has the capability for product-term Preload. When the global-preload product term is true, the PALCE29M16 will enter the preload mode. This feature aids functional testing by allowing direct setting of register states. The procedure for Preload is as follows:

- Set the selected input pins to the user selected preload condition.
- Apply the desired register value to the I/O pins. This sets Q of the register. The value seen on the I/O pin, after Preload, will depend on whether the macrocell is active high or active low.
- Pulse the clock pin (pin 1).
- Remove the inputs to the I/O pins.
- Remove the Preload condition.
- Verify V_{OL}/V_{OH} for all output pins as per programmed pattern.

Because the Preload command is a product term, any input to the array can be used to set Preload (including I/O pins and registers). Preload itself will change the values of the I/O pins and registers. This will have unpredictable results. Therefore, only dedicated input pins should be used for the Preload command.

Parameter Symbol	Parameter Description	Min	Rec.	Max	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
tw	Pulse Width	250	500	700	ns
$t_{I/O}$	Valid Output	100		500	ns



Preload Waveform

OBSERVABILITY

The PALCE29M16 has the capability for product-term Observability. When the global-Observe product term is true, the PALCE29M16 will enter the Observe mode. This feature aids functional testing by allowing direct observation of register states.

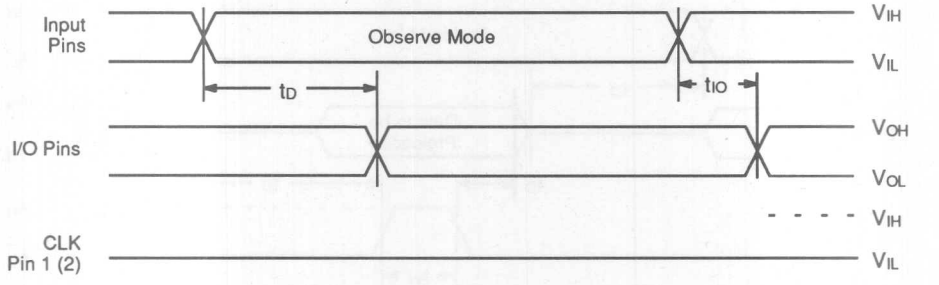
When the PALCE29M16 is in the Observe mode, the output buffer is enabled and the I/O pin value will be Q of the corresponding register. This overrides any $\overline{OE}$ inputs.

The procedure for Observe is:

- Remove the inputs to all the I/O pins.
- Set the inputs to the, user selected, Observe configuration.
- The register values will be sent to the corresponding I/O pins.
- Remove the Observe configuration from the selected I/O pins.

Because the Observe command is a product term, any input to the array can be used to set Observe (including I/O pins and registers). If I/O pins are used, the observe mode could cause a value change, which would cause the device to oscillate in and out of the Observe mode. Therefore, only dedicated input pins should be used for the Observe command.

Parameter Symbol	Parameter Description	Min	Rec.	Max	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
$t_{I/O}$	Valid Output	100		500	ns



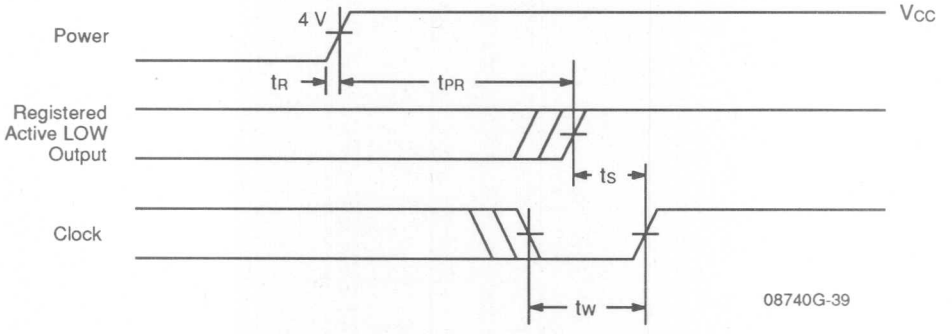
Observability Waveform

POWER-UP RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min	Max	Unit
t_{PR}	Power-Up Reset Time		10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_W	Clock Width			
t_R	V_{CC} Rise Time	500		µs



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. SKINNYDIP	Typ. PLCC	Unit
θ_{jc}	Thermal Impedance, Junction to Case		17	11	°C/W
θ_{ja}	Thermal Impedance, Junction to Ambient		63	51	°C/W
θ_{jma}	Thermal Impedance, Junction to Ambient with Air Flow	200 lfpm air	60	43	°C/W
		400 lfpm air	52	38	°C/W
		600 lfpm air	43	34	°C/W
		800 lfpm air	39	30	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

FINAL

COM'L: H-25

PALCE29MA16H-25

24-Pin EE CMOS Programmable Array Logic

Advanced Micro Devices

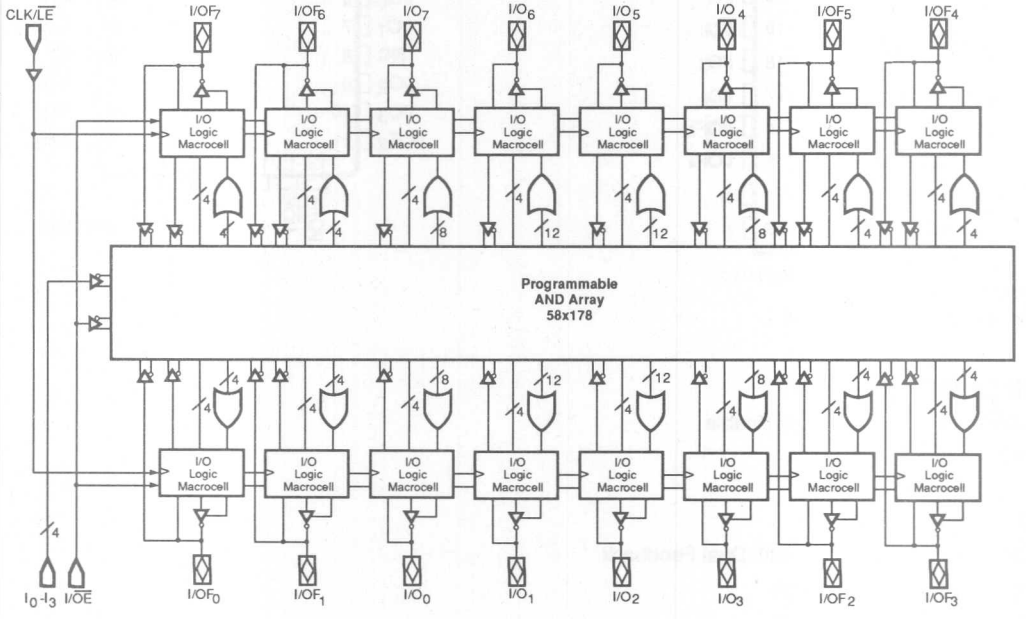
DISTINCTIVE CHARACTERISTICS

- High-performance semicustom logic replacement; Electrically Erasable (EE) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/ Latched operation
- Output Enable controlled by a pin or product terms
- Varied product term distribution for increased design flexibility
- Programmable clock selection with common pin clock/latch enable ($\overline{LE}$) or individual product term clock/$\overline{LE}$ with LOW/HIGH clock/ $\overline{LE}$ polarity
- Register/Latch Preload permits full logic verification
- High speed (t_{PD} = 25 ns, f_{MAX} = 33 MHz and f_{MAX} internal = 50 MHz)
- Full-function AC and DC testing at the factory for high programming and functional yields and high reliability
- 24-pin 300 mil SKINNYDIP and 28-pin plastic leaded chip carrier packages
- Extensive third-party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

The PALCE29MA16 is a high-speed, EE CMOS Programmable Array Logic (PAL) device designed for general logic replacement in TTL or CMOS digital systems. It offers high speed, low power consumption, high programming yield, fast programming, and excellent reliability. PAL devices combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other

BLOCK DIAGRAM



08811G-1

Publication# 08811 Rev. G Amendment/0
Issue Date: June 1993

GENERAL DESCRIPTION (continued)

semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

The PALCE29MA16 uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to 29 array inputs and 16 outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as combinatorial, registered, or latched with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PALCE29MA16 by providing a varied number of logic product terms per output. Of the 16 outputs, 8 outputs have 4 product terms each, 4 outputs have 8 product terms each, and the other 4 outputs have 12 product terms each. This varied product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or Output Enable product term. Each output can also be permanently enabled or disabled.

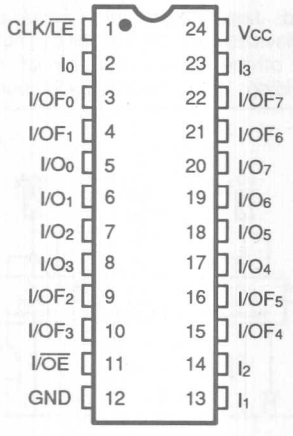
System operation has been enhanced by the addition of common asynchronous-Preset and Reset product terms and a power-up Reset feature. The PALCE29MA16 also incorporates Preload and Observability functions which permit full logic verification of the design.

The PALCE29MA16 is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

CONNECTION DIAGRAMS

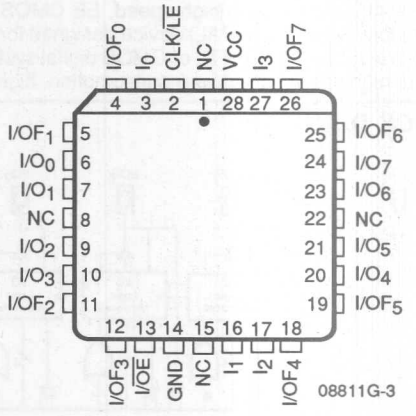
Top View

SKINNYDIP



08811G-2

PLCC



08811G-3

Note:

Pin 1 is marked for orientation.

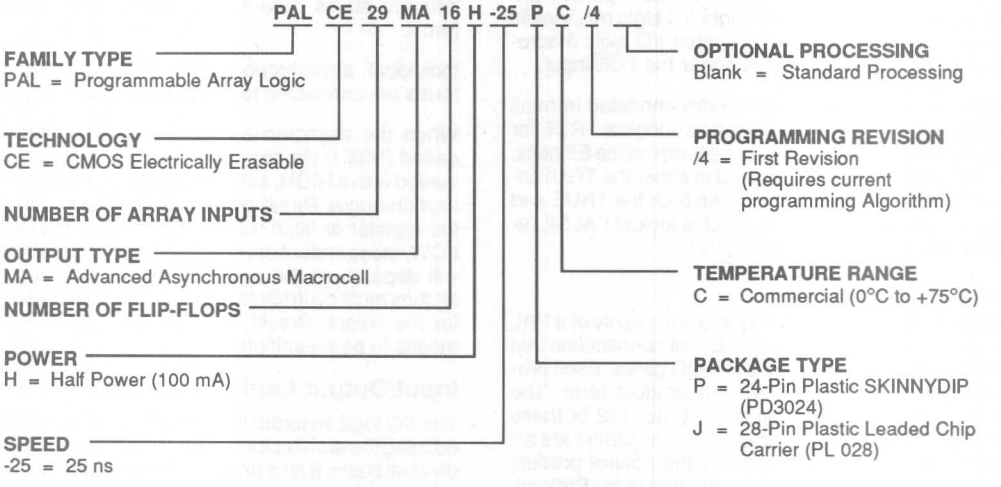
PIN DESIGNATIONS

CLK/$\overline{LE}$	=	Clock or Latch Enable
GND	=	Ground
I	=	Input
I/O	=	Input/Output
I/OF	=	Input/Output with Dual Feedback
Vcc	=	Supply Voltage
NC	=	No Connection

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations		
PALCE29MA16H-25	PC, JC	/4

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Inputs

The PALCE29MA16 has 29 inputs to drive each product term (up to 58 inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these 29 inputs, 4 are dedicated inputs, 16 are from eight I/O logic macrocells with two feedbacks, 8 are from other I/O logic macrocells with single feedback and one is the I/$\overline{OE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the EE cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29MA16 has 178 product terms; 112 of these product terms provide logic capability and others are architectural product terms. Among the control product terms, one is for Observability, and one is for Preload. The Output Enable of each macrocell can be programmed to be controlled by a common Output Enable pin or an individual product term. It may also be permanently disabled. In addition, independent product terms for each macrocell control Preset, Reset and CLK/$\overline{LE}$.

Each product term on the PALCE29MA16 consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from 4 to 12 wide, with an average of 7 logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Individual asynchronous-Preset and Reset product terms are connected to all Registered or Latched I/Os.

When the asynchronous-Preset product term is asserted (HIGH) the register or latch will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-Reset product term is asserted (HIGH) the register or latch will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the Reset, Preset, Preload, and power-up Reset modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29MA16 has 16 macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers and Latches are used in synchronous logic applications. Registers and Latches with product term controlled clocks can also be used in asychronous application.

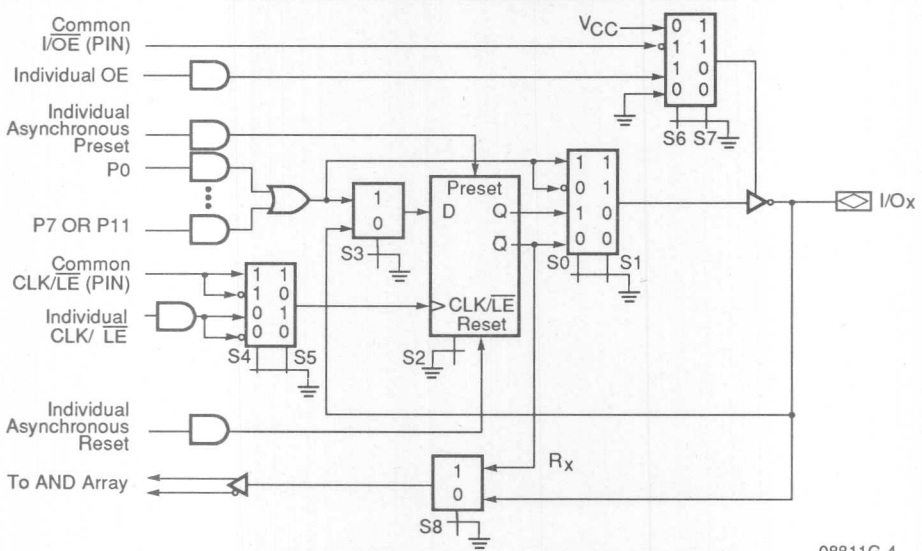


Figure 2a. PALCE29MA16 Macrocell (Single Feedback)

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0–I/OF_7) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the signal generated by the AND-OR array or the corresponding I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29MA16 has a dedicated CLK/$\overline{LE}$ pin and one individual CLK/$\overline{LE}$ product term or macrocell. All macrocells have a programmable switch to choose between the CLK/$\overline{LE}$ pin and the CLK/$\overline{LE}$ product term as the clock or latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers or latches can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by a product term.

I/O Logic Macrocell Configuration

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain 9 EE cells, while the other eight macrocells contain 8 EE cells for programming the input/output functions (see Table 1).

EE cell S_1 controls whether the macrocell will be combinatorial or registered/latched. S_0 controls the output polarity (active-HIGH or active-LOW). S_2 determines whether the storage element is a register or a latch. S_3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable EE cells S_4 and S_5 allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. S_6 and S_7 are used to control Output Enable as pin controlled, product-term controlled, permanently enabled or permanently disabled. S_8 controls a feedback multiplexer for the macrocells with a single feedback path only.

Using the programmable EE cells S_0–S_8 various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the erased state (charged, disconnected), an architectural cell is said to have a value of "1"; in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of "0."

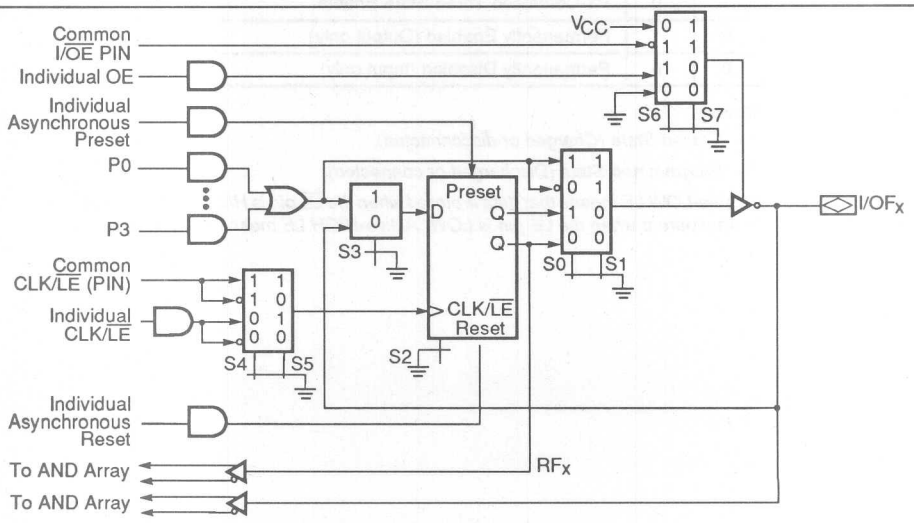


Figure 2b. PALCE29MA16 Macrocell (Dual Feedback)

Table 1a. PALCE29MA16 I/O Logic Macrocell Architecture Selections

S_3	I/O Cell
1	Output Cell
0	Input Cell

S_2	Storage Element
1	Register
0	Latch

S_1	Output Type
1	Combinatorial
0	Register/Latch

S_0	Output Polarity
1	Active LOW
0	Active HIGH

S_8	Feedback*
1	Register/Latch
0	I/O

**Applies to macrocells with single feedback only.*

Table 1b. PALCE29MA16 I/O Logic Macrocell Clock Polarity and Output Enable Selections

S_4	S_5	Clock Edge/Latch Enable Level
1	1	CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE*
1	0	CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE*
0	1	CLK/$\overline{LE}$ PT positive-going edge, active-LOW LE*
0	0	CLK/$\overline{LE}$ PT negative-going edge, active-HIGH LE*

S_6	S_7	Output Buffer Control
1	1	Pin-Controlled Three-State Enable
1	0	PT-Controlled Three-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

Notes:

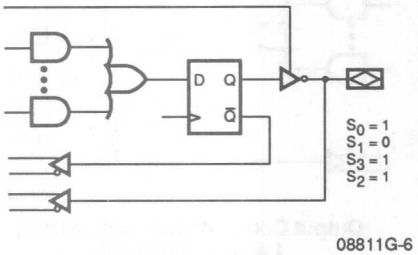
1 = Erased State (Charged or disconnected).

0 = Programmed State (Discharged or connected).

**Active-LOW LE means that data is stored when the $\overline{LE}$ pin is HIGH, and the latch is transparent when the $\overline{LE}$ pin is LOW. Active-HIGH LE means the opposite.*

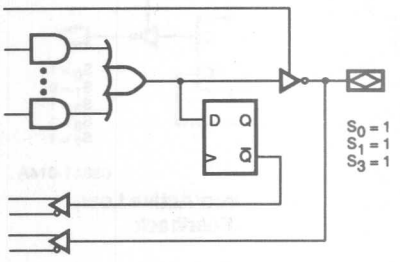
SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable).



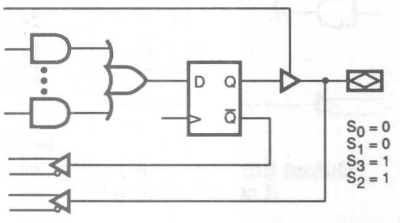
08811G-6

Output Registered/Active Low



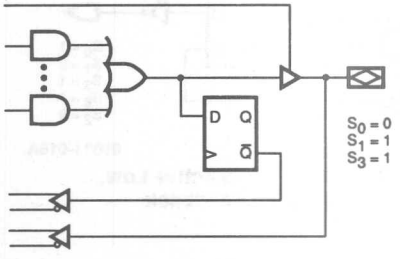
08811G-7

Output Combinatorial/Active Low



08811G-8

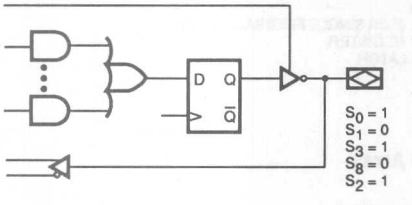
Output Registered/Active High



08811G-9

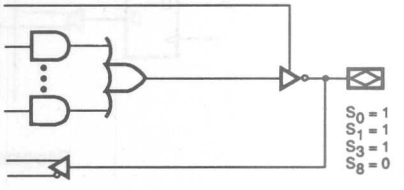
Output Combinatorial/Active High

Figure 3a. Dual Feedback Macrocells



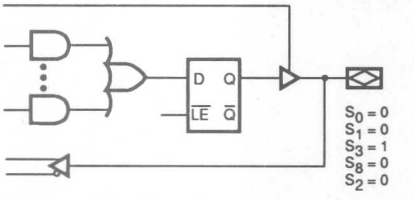
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Output Registered/Active Low, I/O Feedback



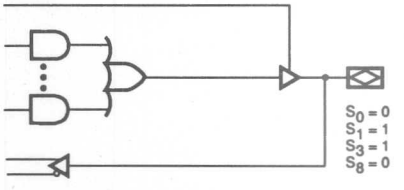
08811G-11

Output Combinatorial/Active Low, I/O Feedback



08811G-12

Output Latched/Active High, I/O Feedback

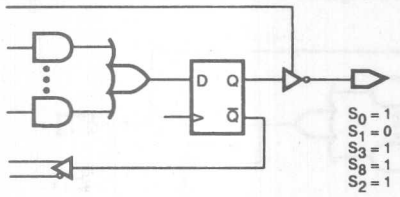


08811G-13

Output Combinatorial/Active High, I/O Feedback

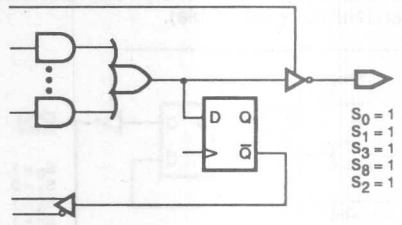
Figure 3b. Single Feedback Macrocells

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL



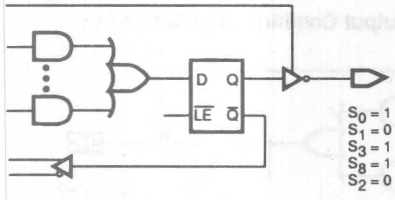
08811-014A

Output Registered/Active Low, Register Feedback



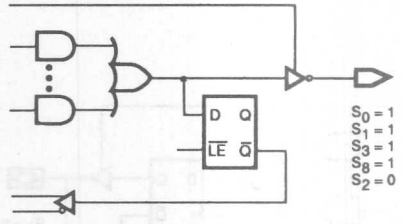
08811-015A

Output Combinatorial/Active Low, Latched Feedback



08811-016A

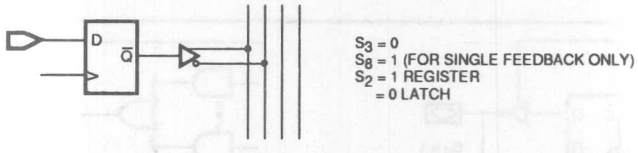
Output Latched/Active Low, Latched Feedback



08811-017A

Output Combinatorial/Active Low, Latched Feedback

Figure 3b. Single Feedback Macrocells (Continued)



08811-018A

Programmable-AND Array

Figure 3c. All Macrocells

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. The outputs of the PALCE29MA16 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW if programmed as active LOW and HIGH if programmed as active HIGH. If combinatorial is selected, the output will be a function of the logic.

Preload

To simplify testing, the PALCE29MA16 is designed with preload circuitry that provides an easy method for testing logical functionality. Both product-term-controlled and supervoltage-enabled preload modes are available. The TTL-level preload product term can be useful during debugging, where supervoltages may not be available.

Preload allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into an arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way any transition can be checked.

Since preload can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, preload, and the observability modes. The only way to erase the protection cell is by erasing the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

Programming and Erasing

The PALCE29MA16 can be programmed on standard logic programmers. It may also be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erasure operation is required.

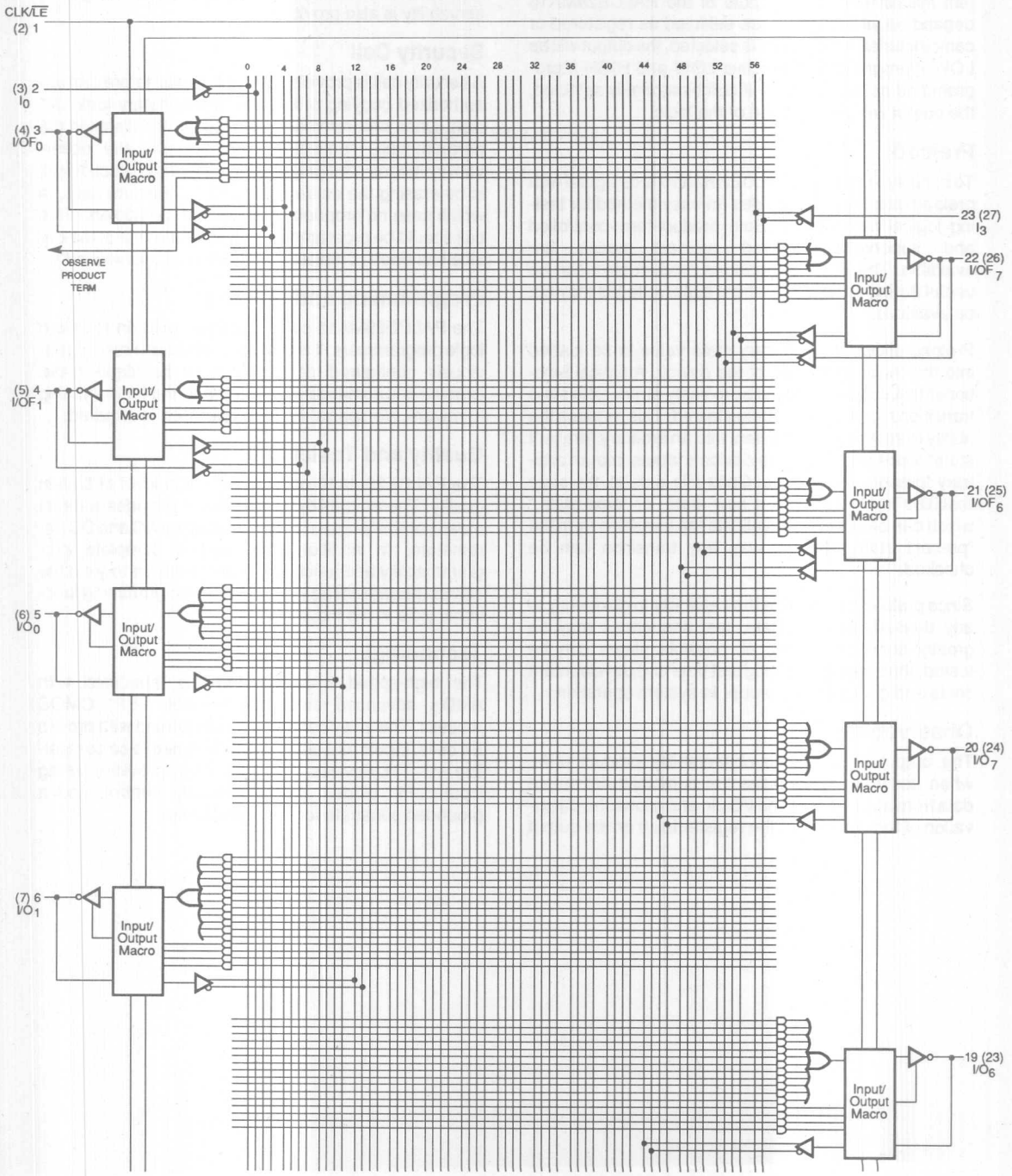
Quality and Testability

The PALCE29MA16 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yield and post-programming functional yield in the industry.

Technology

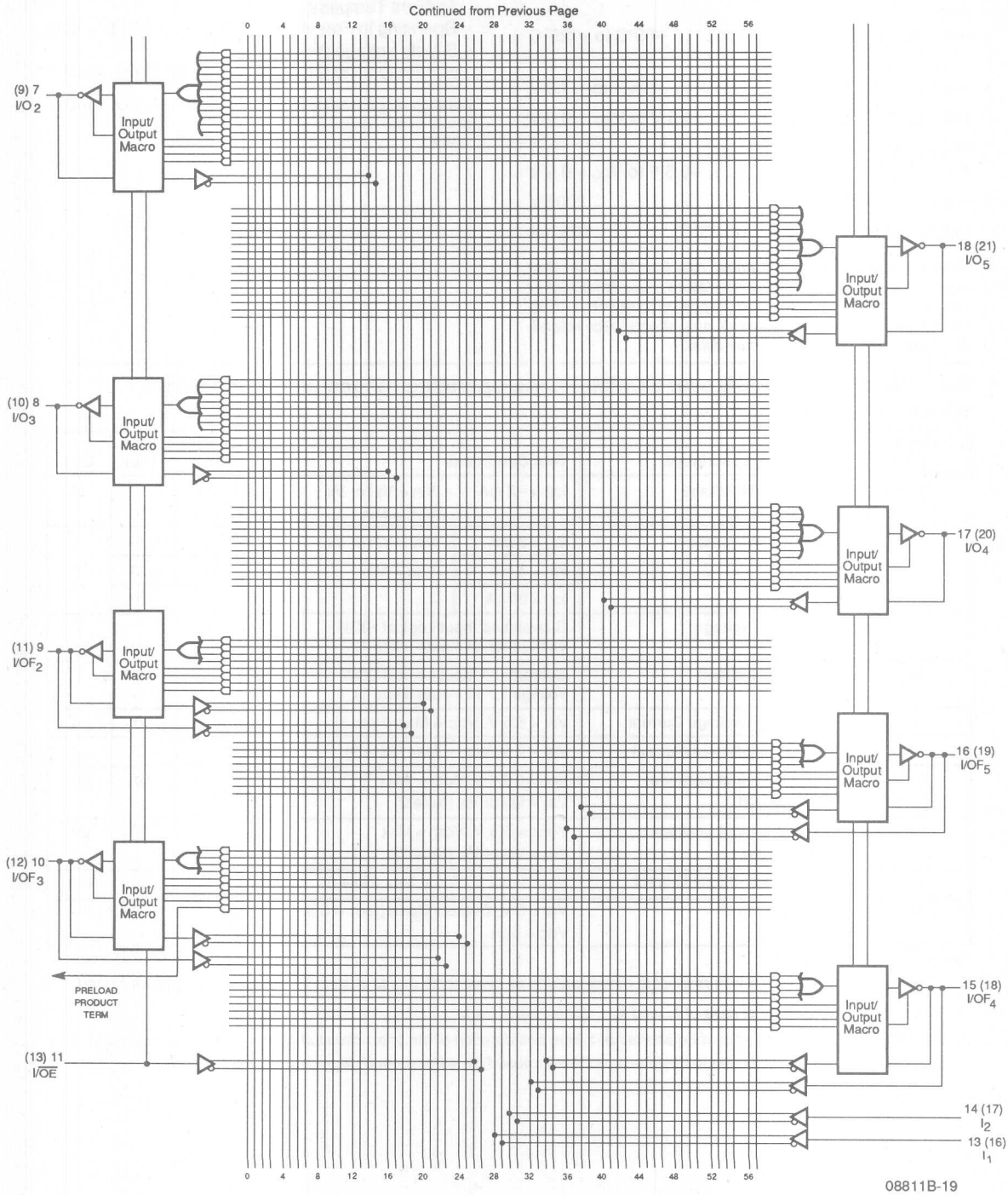
The high-speed PALCE29MA16 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNY DIP (PLCC) Pinouts



08811B-19

LOGIC DIAGRAM
SKINNY DIP (PLCC) Pinouts



08811B-19
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA	V_{IN} = V_{IH} or V_{IL}		0.5	V
		I_{OL} = 4 mA	V_{CC} = Min		0.33	
		I_{OL} = 20 µA			0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max			100	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

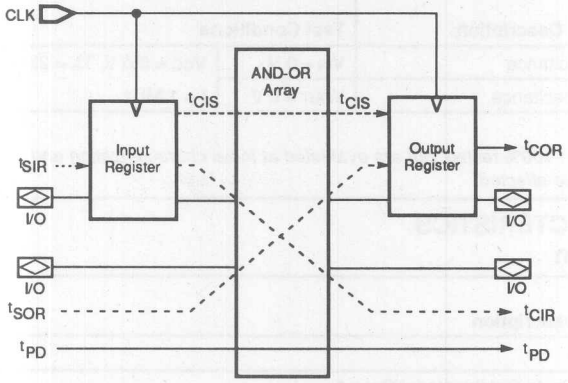
Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

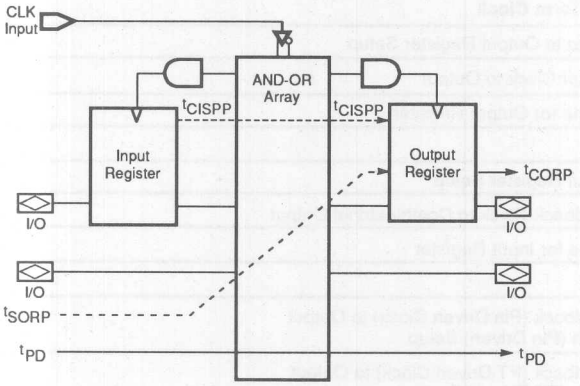
SWITCHING CHARACTERISTICS
Registered Operation

Parameter Symbol	Parameter Description	Min	Max	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
Output Register – Pin Clock				
t_{SOR}	Input or I/O Pin to Output Register Setup	15		ns
t_{COR}	Output Register Clock to Output		15	ns
t_{HOR}	Data Hold Time for Output Register	0		ns
Output Register – Product Term Clock				
t_{SORP}	I/O Pin or Input to Output Register Setup	4		ns
t_{CORP}	Output Register Clock to Output		29	ns
t_{HORP}	Data Hold Time for Output Register	10		ns
Input Register – Pin Clock				
t_{SIR}	I/O Pin to Input Register Setup	2		ns
t_{CIR}	Register Feedback Clock to Combinatorial Output		28	ns
t_{HIR}	Data Hold time for Input Register	6		ns
Clock and Frequency				
t_{CIS}	Register Feedback (Pin Driven Clock) to Output Register/Latch (Pin Driven) Setup	20		ns
t_{CISPP}	Register Feedback (PT Driven Clock) to Output Register/Latch (PT Driven) Setup	25		ns
f_{MAX}	Maximum Frequency (Pin Driven) $1/(t_{SOR} + t_{COR})$	33.3		MHz
f_{MAXI}	Maximum Internal Frequency (Pin Driven) $1/t_{CIS}$	50		MHz
f_{MAXP}	Maximum Frequency (PT Driven) $1/(t_{SORP} + t_{CORP})$	30		MHz
f_{MAXIPP}	Maximum Internal Frequency (PT Driven) $1/t_{CISPP}$	40		MHz
t_{CWH}	Pin Clock Width HIGH	8		ns
t_{CWL}	Pin Clock Width LOW	8		ns
t_{CWHP}	PT Clock Width HIGH	12		ns
t_{CWLP}	PT Clock Width LOW	12		ns



08811G-20

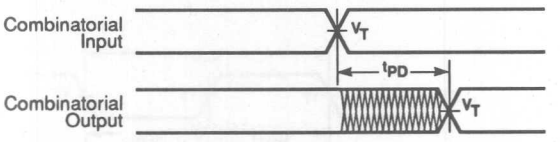
Input/Output Register Specs (Pin CLK Reference)



08811G-21

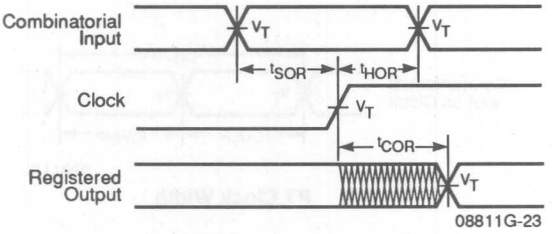
Input/Output Register Specs (PT CLK Reference)

SWITCHING WAVEFORMS



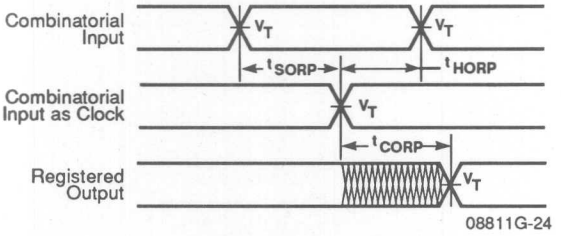
08811G-22

Combinatorial Output



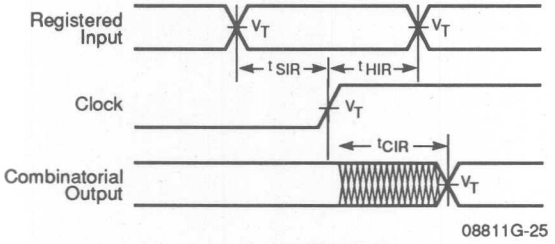
08811G-23

Output Register (Pin Clock)



08811G-24

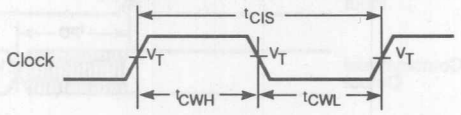
Output Register (PT Clock)



08811G-25

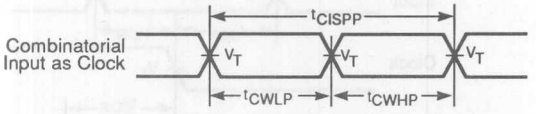
Input Register

SWITCHING WAVEFORMS



08811G-26

Pin Clock Width



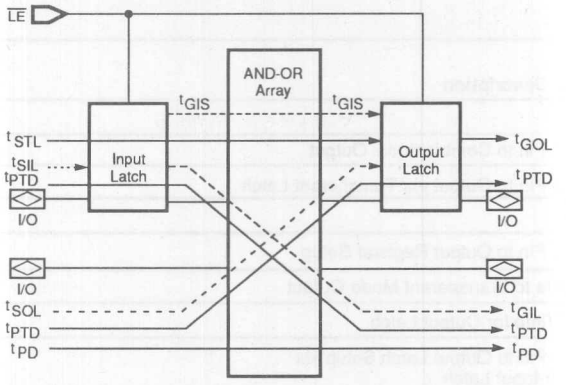
08811G-27

PT Clock Width

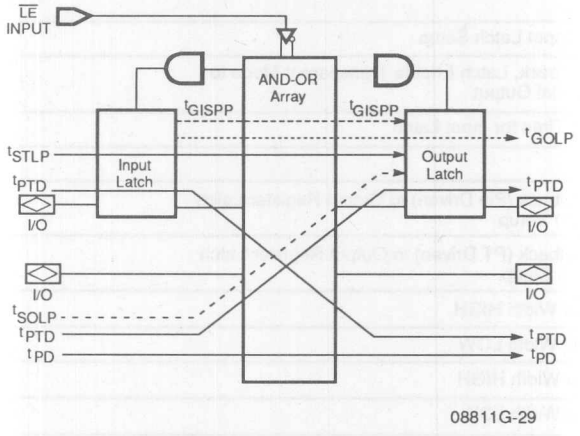
SWITCHING CHARACTERISTICS

Latched Operation

Parameter Symbol	Parameter Description	Min	Max	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
t_{PTD}	Input or I/O Pin to Output via Transparent Latch		28	ns
Output Latch – Pin LE				
t_{SOL}	Input or I/O Pin to Output Register Setup	15		ns
t_{GOL}	Latch Enable to Transparent Mode Output		15	ns
t_{HOL}	Data Hold Time for Output Latch	0		ns
t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	18		ns
Output Latch – Product Term LE				
t_{SOLP}	Input or I/O Pin to Output Latch Setup	4		ns
t_{GOLP}	Latch Enable to Transparent Mode Output		29	ns
t_{HOLP}	Data Hold Time for Output Latch	10		ns
t_{STLP}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	10		ns
Input Latch – Pin LE				
t_{SIL}	I/O Pin to Input Latch Setup	2		ns
t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		28	ns
t_{HIL}	Data Hold Time for Input Latch	6		ns
Latch Enable				
t_{GIS}	Latch Feedback (Pin Driven) to Output Register/Latch (Pin Driven) Setup	20		ns
t_{GISPP}	Latch Feedback (PT Driven) to Output Register/Latch (PT Driven) Setup	25		ns
t_{GWH}	Pin Enable Width HIGH	8		ns
t_{GWL}	Pin Enable Width LOW	8		ns
t_{GWHP}	PT Enable Width HIGH	12		ns
t_{GWLP}	PT Enable Width LOW	12		ns

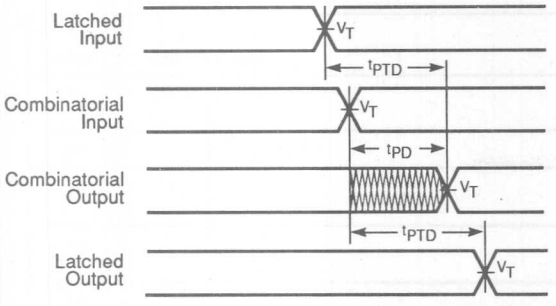


Input/Output Latch Specs (Pin $\overline{LE}$ Reference)



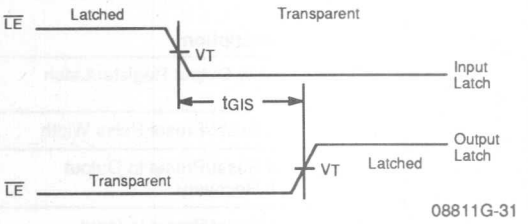
Input/Output Latch Specs (PT $\overline{LE}$ Reference)

SWITCHING WAVEFORMS



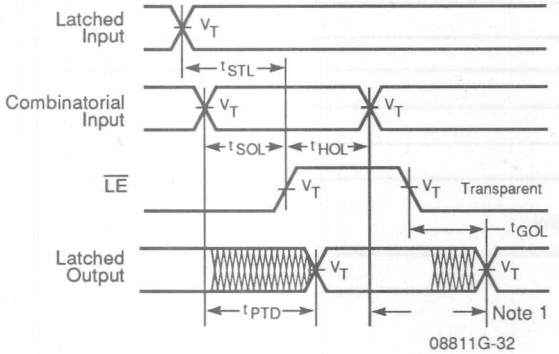
08811G-30

Latch (Transparent Mode)



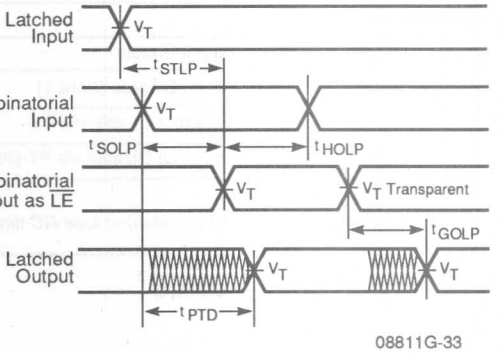
08811G-31

Input and Output Latch Relationship



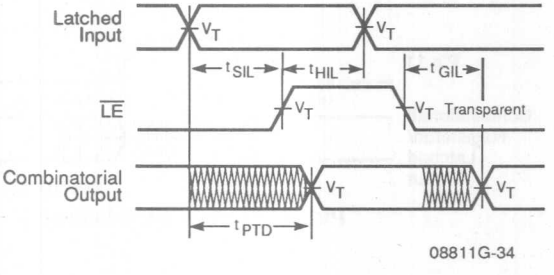
08811G-32

Output Latch (Pin $\overline{LE}$)



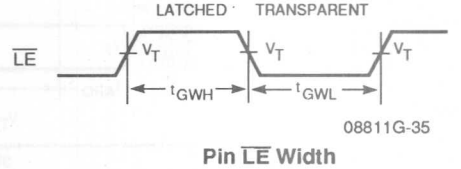
08811G-33

Output Latch (PT $\overline{LE}$)



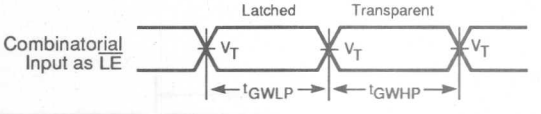
08811G-34

Input Latch (Pin $\overline{LE}$)



08811G-35

Pin $\overline{LE}$ Width



08811G-36

PT $\overline{LE}$ Width

Note:

1. *If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode after t_{PTD} ns has elasped, the corresponding latched output will change t_{GOL} ns after $\overline{LE}$ goes into the transparent mode. If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode before t_{PTD} ns has elapsed, the corresponding latched output will change at the later of the following – t_{PTD} ns after the combinatorial input changes or t_{GOL} ns after $\overline{LE}$ goes into the latched mode.*

SWITCHING CHARACTERISTICS

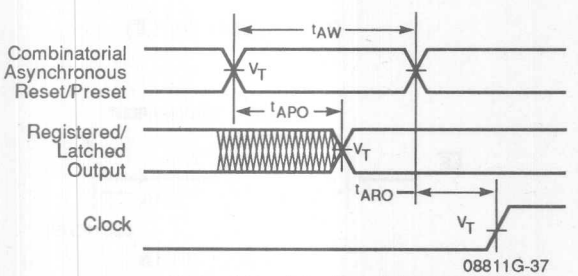
Reset/Preset, Enable

Parameter Symbol	Parameter Description	Min	Max	Unit
t_{APO}	Input or I/O Pin to Output Register/Latch Reset/Preset		30	ns
t_{AW}	Asynchronous Reset/Preset Pulse Width	15		ns
t_{ARO}	Asynchronous Reset/Preset to Output Register/Latch Recovery	15		ns
t_{ARI}	Asynchronous Reset/Preset to Input Register/Latch Recovery	12		ns
t_{ARPO}	Asynchronous Reset/Preset to Output Register/Latch Recovery PT Clock/LE	4		ns
t_{ARPI}	Asynchronous Reset/Preset to Input Register/Latch Recovery PT Clock/LE	6		ns
Output Enable Operation				
t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		20	ns
t_{PXZ}	I/$\overline{OE}$ Pin to Output Disable (Note 1)		20	ns
t_{EA}	Input or I/O to Output Enable via PT		25	ns
t_{ER}	Input or I/O to Output Disable via PT (Note 1)		25	ns

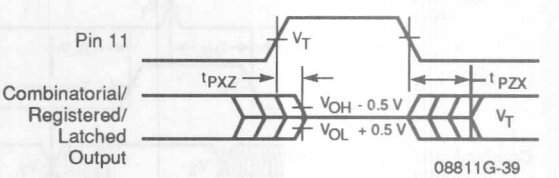
Note:

1. Output disable times do not include test load RC time constants.

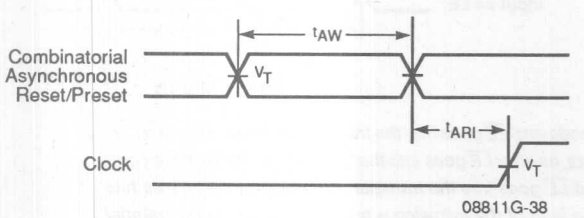
SWITCHING WAVEFORMS



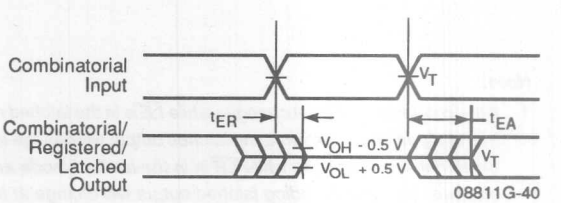
Output Register/Latch Reset/Preset



Pin 11 to Output Disable/Enable

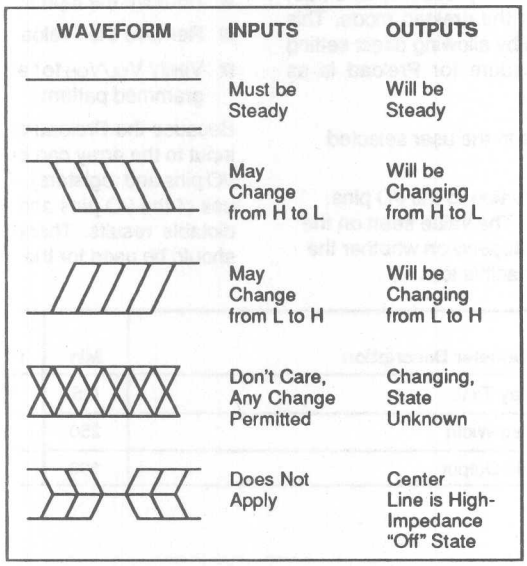


Input Register/Latch Reset/Preset



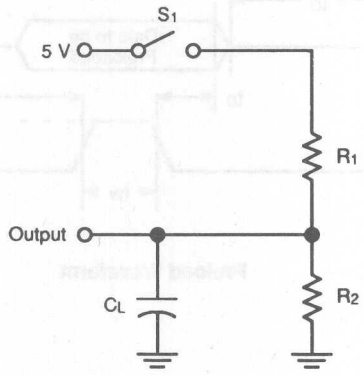
Input to Output Disable/Enable

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



08811G-41

Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{GOL}	Closed	35 pF	470 Ω	390 Ω	1.5 V
t_{EA}, t_{PZX}	Z→H: open Z→L: closed				1.5 V
t_{ER}, t_{PXZ}	H→Z: open L→Z: closed	5 pF			H→Z: V_{OH} –0.5 V L→Z: V_{OL} +0.5 V

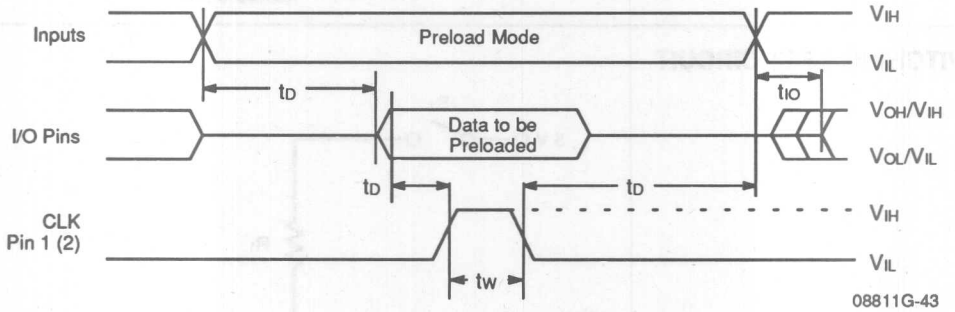
PRELOAD

The PALCE29MA16 has the capability for product-term Preload. When the global-preload product term is true, the PALCE29MA16 will enter the preload mode. This feature aids functional testing by allowing direct setting of register states. The procedure for Preload is as follows:

- Set the selected input pins to the user selected preload condition.
- Apply the desired register value to the I/O pins. This sets Q of the register. The value seen on the I/O pin, after Preload, will depend on whether the macrocell is active high or active low.
- Pulse the clock pin (pin 1).
- Remove the inputs to the I/O pins.
- Remove the Preload condition.
- Verify V_{OL}/V_{OH} for all output pins as per programmed pattern.

Because the Preload command is a product term, any input to the array can be used to set Preload (including I/O pins and registers). Preload itself will change the values of the I/O pins and registers. This will have unpredictable results. Therefore, only dedicated input pins should be used for the Preload command.

Parameter Symbol	Parameter Description	Min	Rec.	Max	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
t_W	Pulse Width	250	500	700	ns
t_{VO}	Valid Output	100		500	ns



Preload Waveform

OBSERVABILITY

The PALCE29MA16 has the capability for product-term Observability. When the global-Observe product term is true, the PALCE29MA16 will enter the Observe mode. This feature aids functional testing by allowing direct observation of register states.

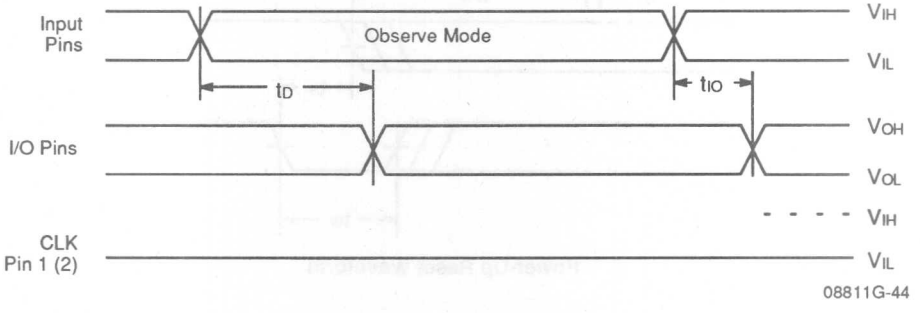
When the PALCE29MA16 is in the Observe mode, the output buffer is enabled and the I/O pin value will be Q of the corresponding register. This overrides any $\overline{OE}$ inputs.

The procedure for Observe is:

- Remove the inputs to all the I/O pins.
- Set the inputs to the, user selected, Observe configuration.
- The register values will be sent to the corresponding I/O pins.
- Remove the Observe configuration from the selected I/O pins.

Because the Observe command is a product term, any input to the array can be used to set Observe (including I/O pins and registers). If I/O pins are used, the observe mode could cause a value change, which would cause the device to oscillate in and out of the Observe mode. Therefore, only dedicated input pins should be used for the Observe command.

Parameter Symbol	Parameter Description	Min	Rec.	Max	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
$t_{I/O}$	Valid Output	100		500	ns



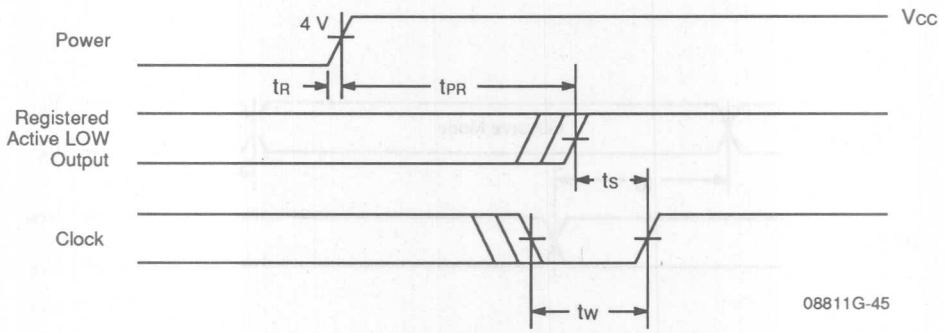
Observability Waveform

POWER-UP RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min	Max	Unit
t_{PR}	Power-Up Reset Time		10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_W	Clock Width			
t_R	V_{CC} Rise Time	500		µs



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		17	11	°C/W
θ_{ja}	Thermal impedance, junction to ambient		63	51	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	60	43	°C/W
		400 lfpm air	52	38	°C/W
		600 lfpm air	43	34	°C/W
		800 lfpm air	39	30	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PALCE610 Family

EE CMOS High Performance Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- AMD's Programmable Array Logic (PAL) architecture
- Electrically-erasable CMOS technology providing half power (90 mA I_{CC}) at high speed
  - -15 = 15 ns t_{PD}
  - -25 = 25 ns t_{PD}
- Sixteen macrocells with configurable I/O architecture
- Registered or combinatorial operation
- Registers programmable as D, T, J-K, or S-R
- Asynchronous clocking via product term or bank register clocking from external pins
- Register preload for testability
- Power-up reset for initialization
- Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages
- Fully tested for 100% programming yield and high reliability
- Extensive third-party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

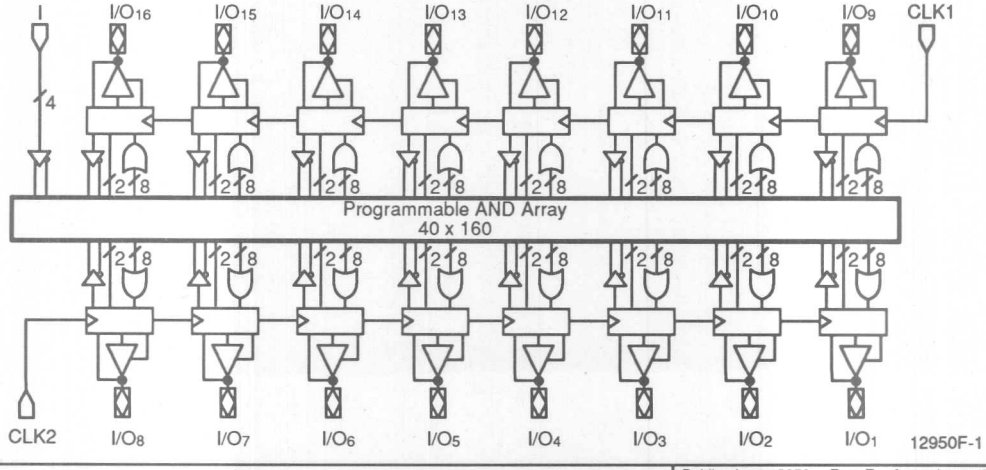
The PALCE610 is a general purpose PAL device and is functionally and fuse map equivalent to the EP610. It can accommodate logic functions with up to 20 inputs and 16 outputs. There are 16 I/O macrocells that can be individually configured to the user's specifications. The macrocells can be configured as either registered or combinatorial. The registers can be configured as D, T, J-K, or S-R flip-flops.

The PALCE610 uses the familiar sum-of-products logic with programmable-AND and fixed-OR structure. Eight product terms are brought to each macrocell to provide logic implementations.

The PALCE610 is manufactured using advanced CMOS EE technology providing high density and low power consumption. Moreover, it is a high-speed device having a worst-case t_{PD} of 15 ns. Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages are offered.

This device can be quickly erased and reprogrammed providing for easy prototyping. Once a device is programmed the security bit can be used to provide protection from copying a proprietary design.

BLOCK DIAGRAM

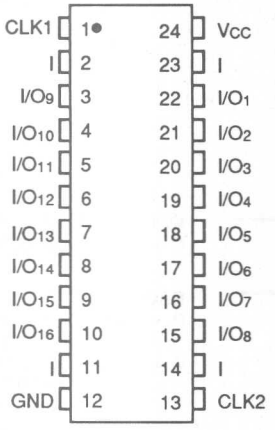


Publication# 12950 Rev. F Amendment /0
Issue Date: June 1993

CONNECTION DIAGRAMS

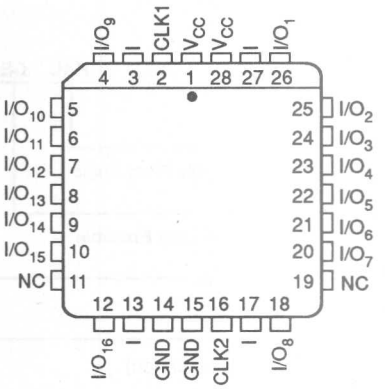
Top View

SKINNYDIP



12950F-2

PLCC/LCC



12950F-3

Note:
Pin 1 is marked for orientation

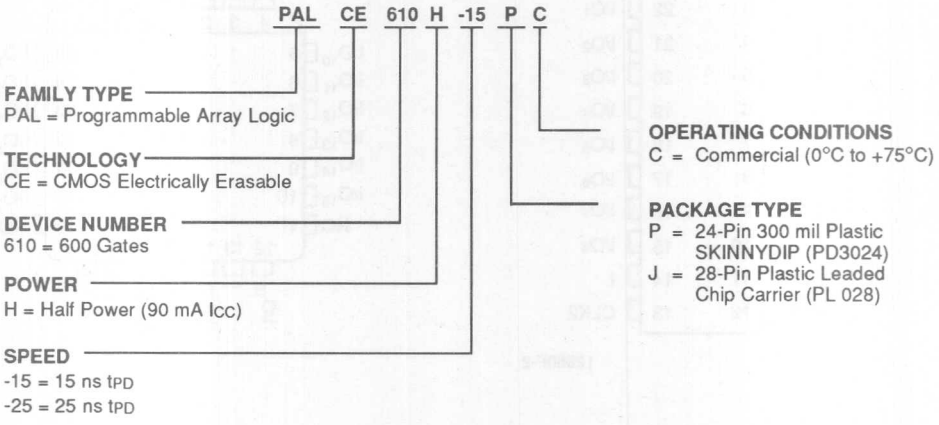
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE610H-15	PC, JC
PALCE610H-25	

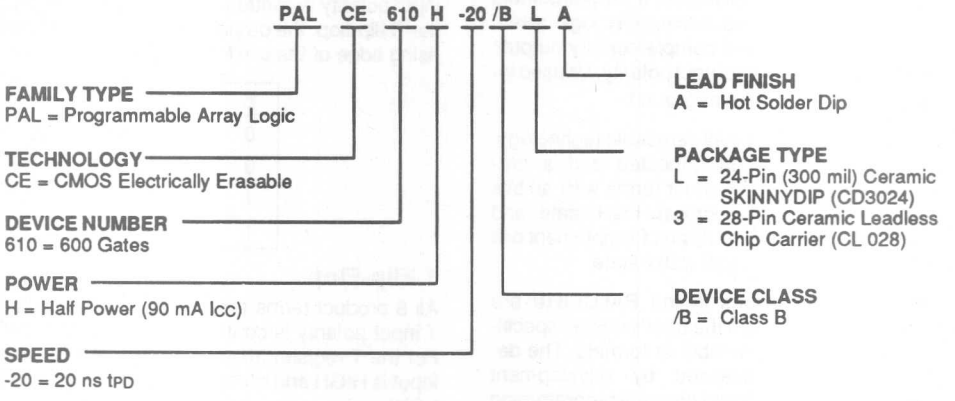
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE610H-20	/BLA,/B3A

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PALCE610 is a general purpose programmable logic device. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J–K, or S–R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Each clock pin controls 8 of the 16 macrocells.

The programming matrix implements a programmable AND logic array which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input polarity. Unused input pins should be tied to V_{CC} or ground.

The array uses AMD's electrically erasable technology. An unprogrammed bit is disconnected and a programmed bit is connected. Product terms with all bits unprogrammed assume the logical-HIGH state and product terms with both the TRUE and Complement bits programmed assume the logical-LOW state.

The programmable functions in the PALCE610 are automatically configured from the user's design specifications, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to the programmer, configures the design according to the user's desired function.

Macrocell Configurations

The PALCE610 macrocell can be configured as either combinatorial or registered. Both the combinatorial and registered configurations have output polarity control. The register can be configured as a D, T, J–K, or S–R type flip-flop. Figure 1 shows the possible configurations.

Each macrocell can select as its clock either the corresponding clock pin or the CLK/OE product term. If the clock pin is selected, the output enable is controlled by the CLK/OE product term. If the CLK/OE product term is selected, the output is always enabled.

Combinatorial I/O

All 8 product terms are available to the OR gate. The output-enable function is performed by the CLK/OE product term.

Registered Configurations

There are 4 flip-flop types available: D, T, J-K and S-R.

The registers can be configured as synchronous or asynchronous. In the synchronous configuration, the clock is controlled by the clock input pin. The output enable is controlled by the product term function. In the asynchronous configuration, the clock input is controlled by the product term. The output is always enabled.

In The D and T configurations, feedback can be either from Q or the output pin. This allows D and T configurations to be either outputs or I/O. In the J–K and S–R configurations, feedback is only from Q; therefore, J–K and S–R configurations are strictly outputs.

D Flip-Flop

All 8 product terms are available to the OR gate. The D input polarity is controlled by an exclusive-OR gate. For the D flip-flop, the output level is the D-input level at the rising edge of the clock.

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

T Flip-Flop

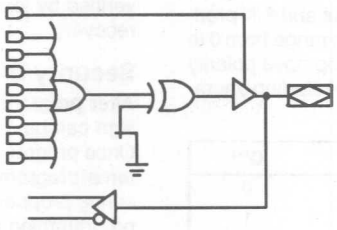
All 8 product terms are available to the OR gate. The T input polarity is controlled by an exclusive-OR gate. For the T register, the output level toggles when the T input is HIGH and remains the same when the T input is LOW.

T	Q^n	Q^{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

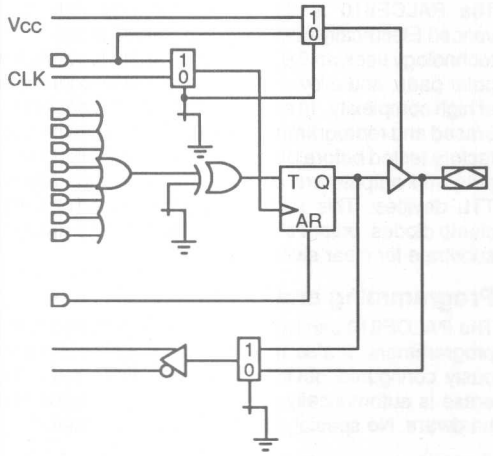
J–K Flip-Flop

The 8 product terms are divided between the J and K inputs. N product terms go to the J input and 8-N product terms go to the K input, where N can range from 0 to 8. Both the J and K inputs to the flip-flop have polarity control via exclusive-OR gates. The J-K flip-flop operation is shown below.

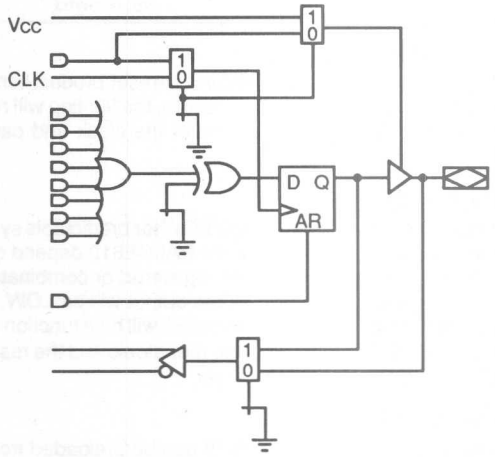
J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



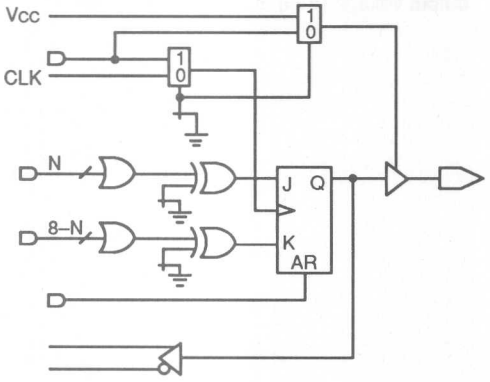
Combinatorial



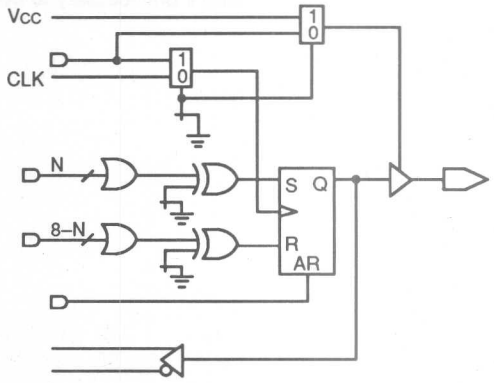
T Register



D Register



J–K Register



S–R Register

12950F-4

Figure 1. Macrocell Configurations

S-R Flip-Flop

The 8 product terms are divided between the S and R inputs. N product terms go to the S input and 8-N product terms go to the R input, where N can range from 0 to 8. Both the S and R inputs to the flip-flop have polarity control via exclusive-OR gates. The S-R flip-flop operation is shown below.

S	R	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1		Not Allowed

Asynchronous Reset

All flip-flops have an asynchronous-reset product-term input. When the product term is true, the flip-flop will reset to a logic LOW, regardless of the clock and data inputs.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE610 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW. If combinatorial is selected, the output will be a function of the logic. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE610 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE610 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during the erase cycle. Preload is not affected by the security bit.

Technology

The PALCE610 is manufactured using AMD's advanced Electrically Erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link in bipolar parts, and allows AMD to offer lower-power parts of high complexity. In addition, since the EE cells can be erased and reprogrammed, these devices can be 100% factory tested before being shipped to the customer. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

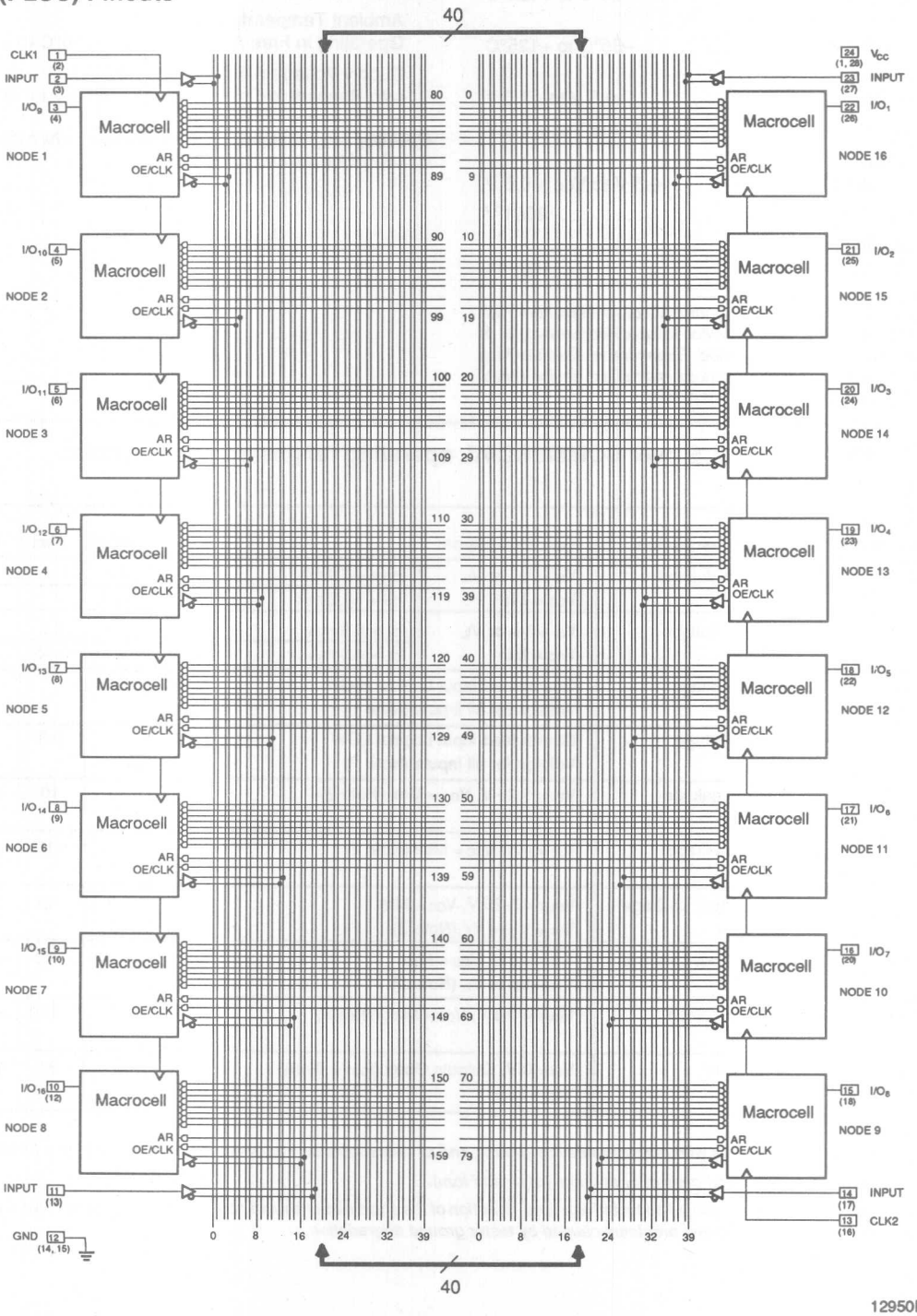
Programming and Erasing

The PALCE610 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

CMOS Compatibility

The PALCE610 has CMOS-compatible outputs. The output voltage (V_{OH}) is 3.85 V at –2.0 mA.

PALCE610 LOGIC DIAGRAM
DIP (PLCC) Pinouts



12950F-5

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OH} = –4.0 mA	2.4		V
			I_{OH} = –2.0 mA	3.84		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	I_{OL} = 8.0 mA		0.5	V
			I_{OL} = 4.0 mA		0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max			90	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min	-15 Max	-25 Min	-25 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				8		12	ns
t_{WL}	Clock Width	LOW		6		10		ns
t_{WH}		HIGH		6		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		37		MHz
		Internal Feedback (f_{CNT})		76.1		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns
t_{AR}	Asynchronous Reset to Registered Output				15		25	ns
t_{ARW}	Asynchronous Reset Width			10		15		ns
t_{ARR}	Asynchronous Reset Recovery Time				15		25	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 4)			5		8		ns
t_{HA}	Hold Time (Note 4)			5		12		ns
t_{COA}	Clock to Output (Note 4)				15		27	ns
t_{WLA}	Clock Width	LOW (Note 4)		6		10		ns
t_{WHA}		HIGH (Note 4)		6		10		ns
f_{MAXA}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_{SA} + t_{COA})$	50		28.6		MHz
		Internal Feedback (f_{CNT})		61.6		29.4		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	83.3		50		MHz

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are measured using the asynchronous product-term clock.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_C = –55°C to +125°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case
Temperature (T_C) . . . . . –55°C to +125°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. *Military products are 100% tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.*

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OH} = –2 mA I_{OH} = –1 mA	2.4 3.84		V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 4)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 4)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = 25° C (Note 5)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT}= 0 A) V_{CC} = Max			90	mA

Notes:

2. *For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.*
3. *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
5. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at anytime the design is modified where I_{OS} may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC}	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	T_A = +25°C, f = 1 MHz	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

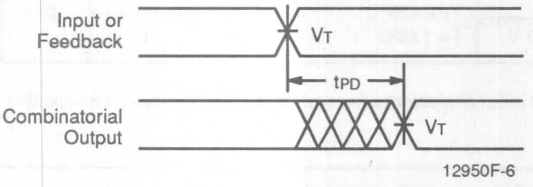
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20 Min	-20 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20	ns
t_S	Setup Time from Input or Feedback to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			10	ns	
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	40		MHz
		Internal Feedback (f_{CNT})		50		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				20	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)				20	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 4)			8		ns
t_{HA}	Hold Time (Note 4)			10		ns
t_{COA}	Clock to Output (Note 4)			20	ns	
t_{WLA}	Clock Width	LOW (Note 4)		8		ns
t_{WHA}		HIGH (Note 4)		8		ns
f_{MAXA}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_{SA} + t_{COA})$	35.8		MHz
		Internal Feedback (f_{CNT})		45		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	52.6		MHz

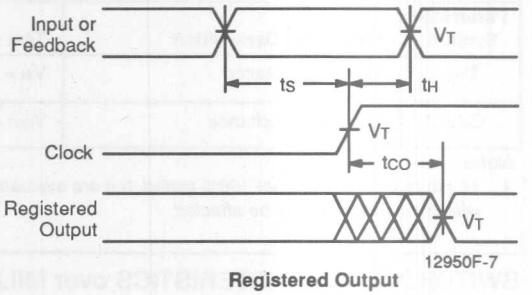
Notes:

2. *See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *These parameters are measured using the asynchronous product-term clock.*

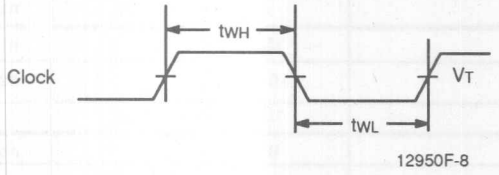
SWITCHING WAVEFORMS



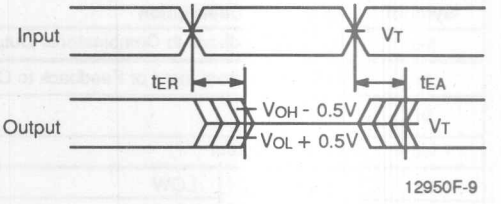
Combinatorial Output



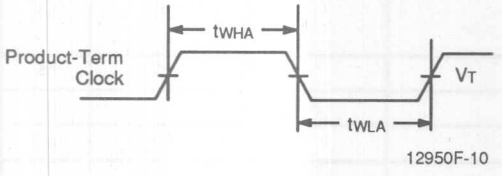
Registered Output



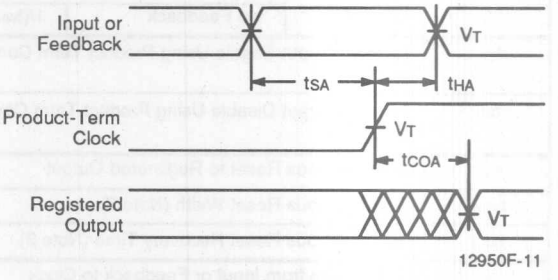
Clock Width



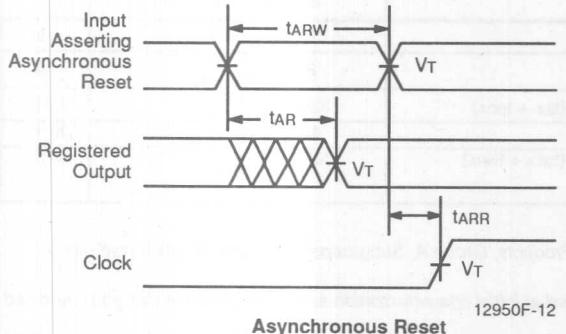
Input to Output Disable/Enable



Clock Width Using Product-Term Clock



Registered Output Using Product-Term Clock

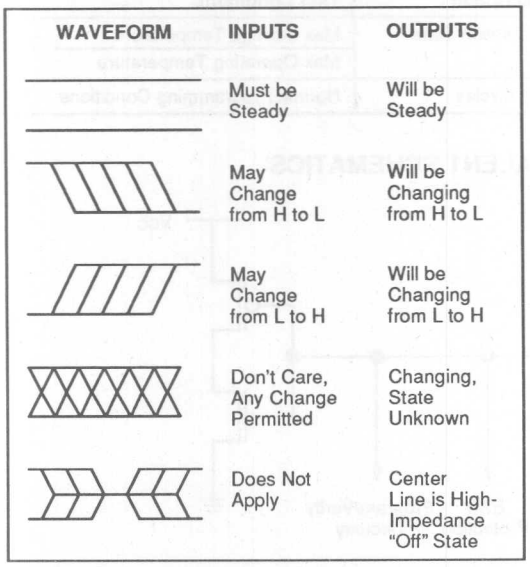


Asynchronous Reset

Notes:

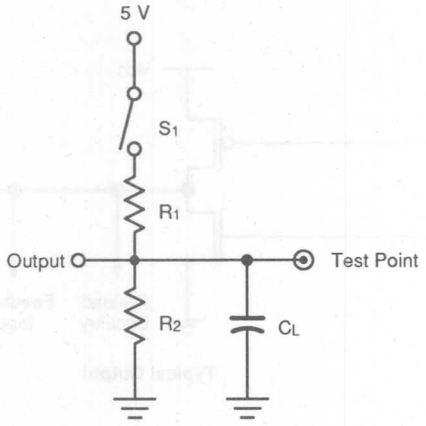
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2 ns–5 ns typical.

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



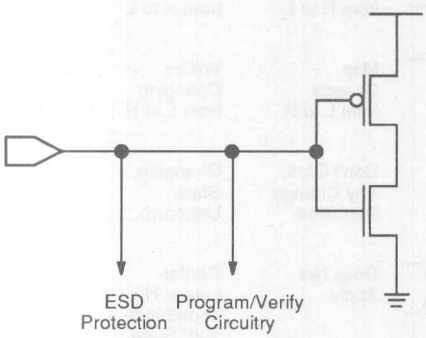
12950F-13

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	855 Ω	340 Ω	855 Ω	340 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed	35 pF					1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

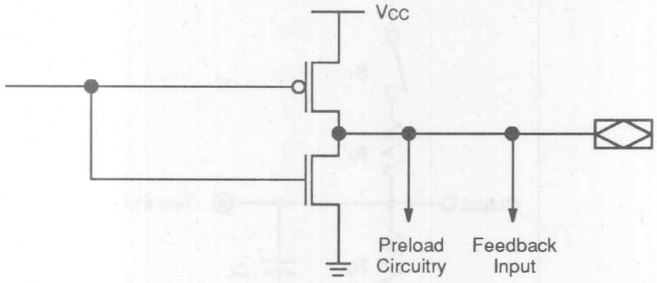
ENDURANCE

Symbol	Parameter Description	Test Conditions	Min	Unit
t_{DR}	Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

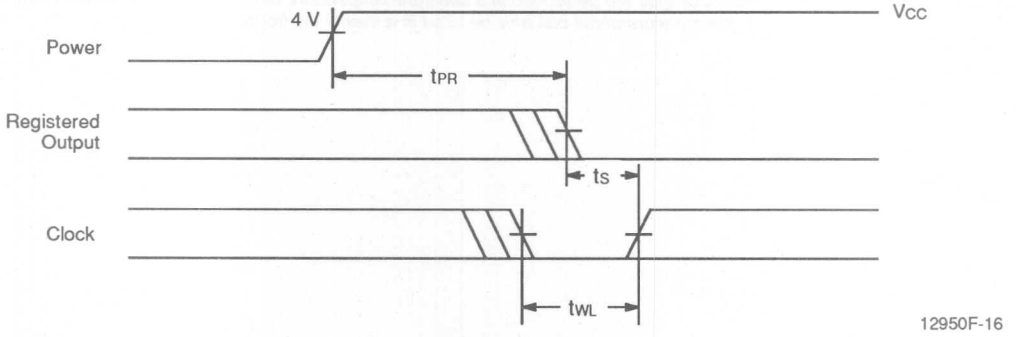
12950F-15

Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		21	20	°C/W
θ_{ja}	Thermal impedance, junction to ambient		72	57	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	64	47	°C/W
		400 lfpm air	60	44	°C/W
		600 lfpm air	55	40	°C/W
		800 lfpm air	49	36	°C/W

Plastic θjc Considerations

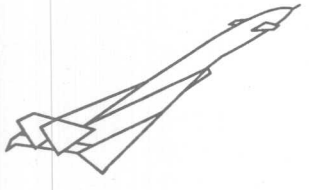
The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

CHAPTER

3 MACH DEVICES

MACH 1 and 2 Device Families **3-3**
MACH110-12/15/20 3-7
MACH120-15/20 3-9
MACH130-15/20 3-11
MACH210A-10, MACH210-12/15/20, MACH210AQ-15/20 3-13
MACHLV210A-15/20 3-15
MACH220-12/15/20 3-17
MACH230-15/20 3-19
MACH215-12/15/20 3-21

MACH 3 and 4 Device Families **3-23**
MACH435-15/20, Q-25 3-27
MACH355-15/20 3-29
MACH445-15/20 3-31
MACH465-15/20 3-33



MACH 1 and 2 Device Families

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density, electrically-erasable CMOS PLD families**
- **900 to 3600 PLD gates**
- **44 to 84 pins in cost-effective PLCC and CQFP packages**
- **32 to 128 macrocells**
- **0.8 µm CMOS provides predictable design-independent high speeds**
  - — Commercial 10/12/15/20-ns t_{PD}, 80/67/50/40-MHz f_{MAX}
  - — Military 20-ns t_{PD}, 40-MHz f_{MAX}
- **Synchronous and asynchronous devices**
- **PAL blocks connected by switch matrix**
  - — Provides optimized global connectivity
  - — Switch matrix integrates blocks into uniform device
- **Configurable macrocells**
  - — Programmable polarity
  - — Registered or combinatorial
  - — Internal and I/O feedback
  - — D-type or T-type flip-flops
  - — Choice of clocks for each flip-flop
  - — Input registers for MACH 2 family
- **Extensive third-party software and programmer support through FusionPLD partners**
  - — Schematic capture and text entry
  - — Compilation and JEDEC file generation
  - — Design simulation
  - — Logic and timing models
  - — Standard PLD programmers
- **Each MACH product has a factory programming option available for high-volume applications**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	PLD Gates	Max Inputs	Max Outputs	Max Flip-Flops	Speed (ns)
MACH 1 Family							
MACH110	44	32	900	38	32	32	12, 15, 20
MACH120	68	48	1200	56	48	48	15, 20
MACH130	84	64	1800	70	64	64	15, 20
MACH 2 Family							
MACH210	44	64	1800	38	32	64	10, 12, 15, 20
MACH220	68	96	2400	56	48	96	12, 15, 20
MACH230	84	128	3600	70	64	128	15, 20
Asynchronous MACH Device							
MACH215	44	64	1500	38	32	64	12, 15, 20

GENERAL DESCRIPTION

The MACH (Macro Array CMOS High-density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced electrically-erasable CMOS technology to offer a device with several times the logic capability of the industry's most popular existing PAL device solutions at comparable speed and cost.

Their unique architecture makes these devices ideal for replacing large amounts of TTL, PAL-device, glue, and gate-array logic. They are the first devices to provide such increased functionality with completely predictable, deterministic speed.

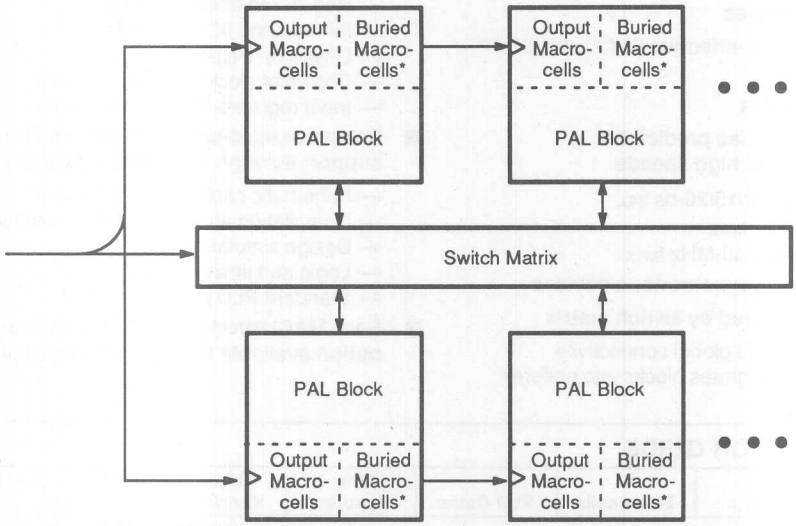
The MACH devices consist of PAL blocks interconnected by a programmable switch matrix (Figure 1). Designs that consist of several interconnected functional modules can be efficiently implemented by placing the modules into PAL blocks. Designs that are not as modular can also be readily implemented since the switch matrix provides a high level of connectivity between PAL blocks. The internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

The MACH family consists of the MACH 1 and MACH 2 series of synchronous devices and the MACH215, an

asynchronous device. The MACH 1 and 2 series are ideal for synchronous subsystems like memory controllers and peripheral controllers. The MACH215 is appropriate for applications having asynchronous inputs and for collecting random glue logic.

AMD's FusionPLD program allows MACH device designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide timely, accurate, quality support. This ensures that a designer does not have to buy a complete new set of tools for each new device, but rather can use the tools with which he or she is already familiar. The MACH devices can be programmed on conventional PAL device programmers with appropriate personality and socket adapter modules.

MACH devices are manufactured using AMD's state-of-the-art advanced CMOS electrically-erasable process for high performance and logic density. CMOS EE technology provides 100% testability, reducing both prototype development costs and production costs.



** Buried macrocell available on MACH 2 devices only.*

Figure 1. MACH 1 and 2 Block Diagram

Design Methodology

Design tools for MACH devices are widely available both from AMD and from third-party software vendors. AMD provides PALASM software as a low-cost baseline tool set and works with tools vendors to ensure broad MACH device support. This allows designers to do MACH device designs using the same tools that they would use to do PAL device designs, whether PALASM software or any of the other popular PAL device design packages.

Design entry is the same as that used for PAL devices. The basic logic processing steps are the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all approved software packages, and other options for simulating the timing and board-level behavior of the MACH devices are available. The end result is a JEDEC file that can be downloaded to a programmer for device configuration.

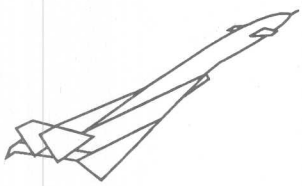
MACH device design methodology differs somewhat from that of a PAL device due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture, state machine equations, or Boolean equations—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. The overall device utilization provided by the Fitter will vary from design to design, but a utilization target of no greater than 70% is recommended. Since a design must be entered and fit in order to calculate actual utilization, it is best to be conservative when estimating utilization before starting a design.

AMD recommends allowing the software to decide the best fit and pin placement automatically for the first design iteration to provide the best chance of fitting. With this approach, large designs can be implemented incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. While it is possible to pre-place signals, it is not recommended in most cases. If done carefully, pre-placement can help the software fit

difficult designs; if not done carefully, it may make it harder for the design to fit. Guidelines on specifying the initial pinout are provided in the MACH Technical Briefs book.

The design is partitioned and placed into the MACH device by the software so as not to affect the performance of the design. With designs that do not fit, it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or passing through the device more than once), but those tradeoffs must be specifically requested, and any additional delays are entirely predictable.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. Design changes make it necessary to refit the design, which may result in a different pinout. Some design changes may make it impossible to refit the design, regardless of the pinout. The stability of the design and the expected extent of any changes should therefore be considered before committing the design to layout. Careful designs that target about 70% utilization will make future changes much easier. Higher utilization will make design changes much more difficult to implement. Hints on designing for change can be found in the *MACH Device Design Planning Guide* near the end of this book, and in the article *Designing for Change with MACH Devices* in the Technical Briefs book.



FINAL COM'L: -12/15/20 MIL: -20

MACH110-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 12 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 66.7 MHz f_{MAX} external Commercial
  40 MHz f_{MAX} external Military
- 38 Inputs
- 32 Outputs
- 32 Flip-Flops; 2 clock choices
- 2 "PAL22V16" Blocks
- Pin-compatible with MACH210, MACH215

GENERAL DESCRIPTION

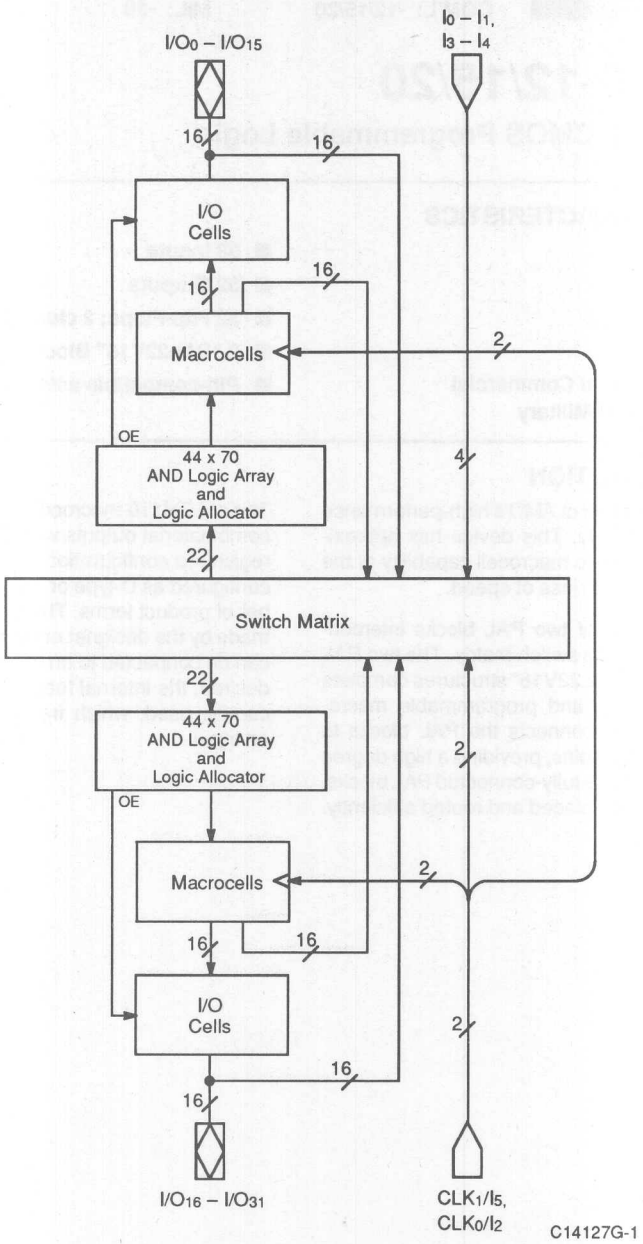
The MACH110 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 with no loss of speed.

The MACH110 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH110 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication# C14127 Rev. G Amendment /0
Issue Date: June 1993

BLOCK DIAGRAM



FINAL

COM'L: -15/20

MACH120-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 48 Macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 56 Inputs
- 48 Outputs
- 48 Flip-flops; 4 clock choices
- 4 PAL blocks
- Pin-compatible with MACH220

GENERAL DESCRIPTION

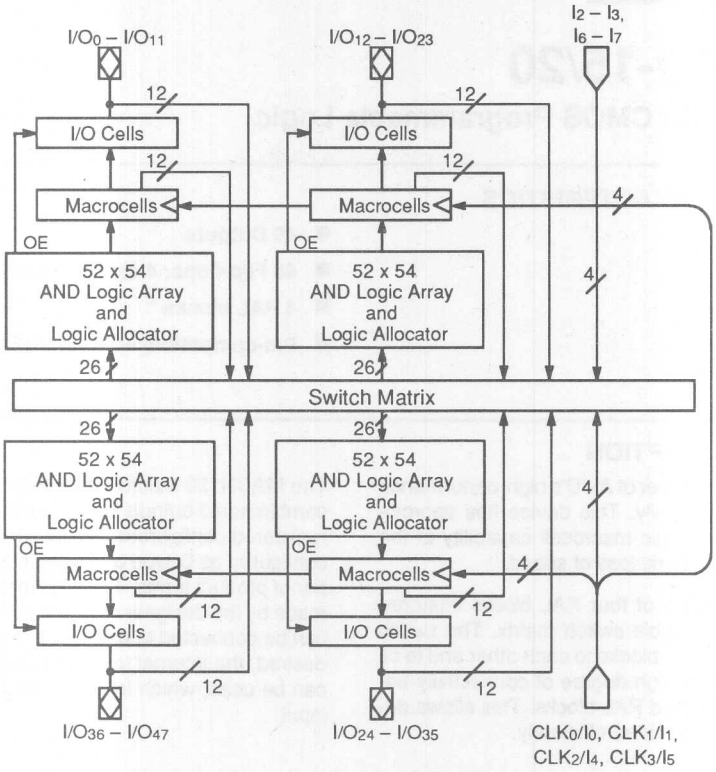
The MACH120 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately five times the logic macrocell capability of the popular PAL22V10 with no loss of speed.

The MACH120 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH120 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication# C14129 Rev. G Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM



FINAL COM'L: -15/20 MIL: -20

MACH130-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 64 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} external Commercial
  40 MHz f_{MAX} external Military
- 70 Inputs
- 64 Outputs
- 64 Flip-flops; 4 clock choices
- 4 "PAL26V16" Blocks with buried Macrocells
- Pin-compatible with MACH230, MACH435

GENERAL DESCRIPTION

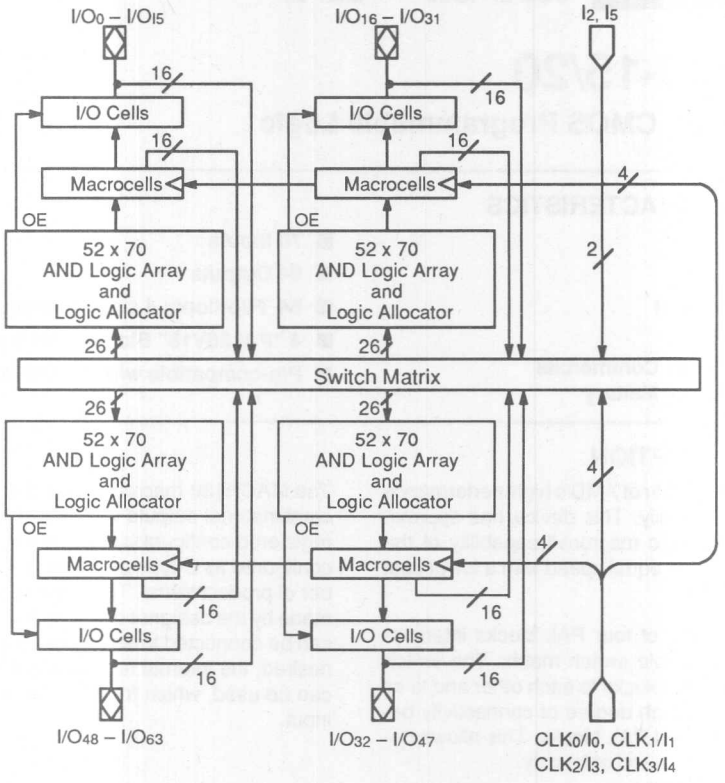
The MACH130 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH130 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH130 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication# C14131 Rev. F Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM



C14131F-1

FINAL COM'L: -10/12/15/20, Q-15/20 MIL: -20

MACH210A-10
MACH210-12/15/20
MACH210AQ-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 64 Macrocells
- 10 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 80 MHz f_{MAX} external Commercial
  40 MHz f_{MAX} external Military
- 38 Inputs; 210A Inputs have built-in pull-up resistors
- 32 Outputs
- 64 Flip-flops; 2 clock choices
- 4 "PAL22V16" blocks with buried macrocells
- Pin-compatible with MACH110, MACH215

GENERAL DESCRIPTION

The MACH210 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 with no loss of speed.

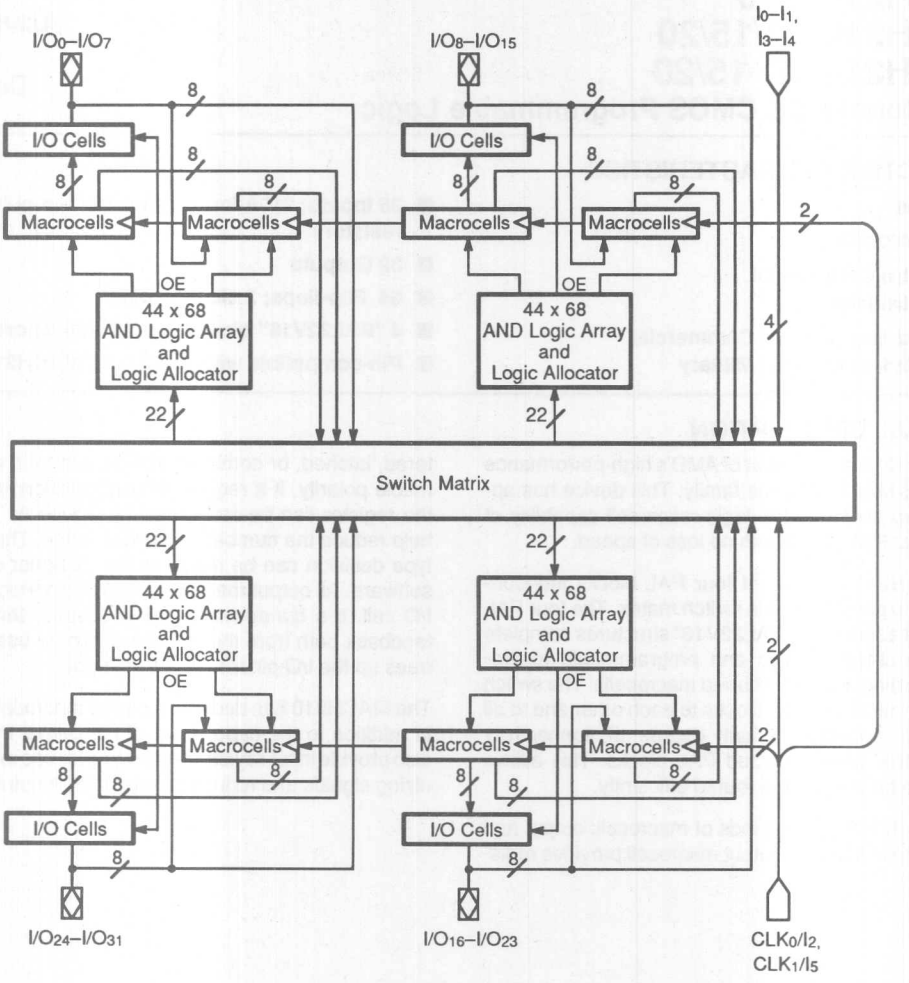
The MACH210 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH210 has two kinds of macrocell: output and buried. The MACH210 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH210 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

Publication# C14128 Rev. G Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM



14128G-1

ADVANCE INFORMATION COM'L: -15/20

MACHLV210A-15/20

High Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
  - — V_{CC} = +3.0 V to +3.6 V
- **10 mA standby power**
- **44 Pins**
- **64 Macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **38 Inputs with pull-up resistors**
- **32 Outputs**
- **64 Flip-flops; 2 clock choices**
- **4 "PAL22V16" blocks with buried macrocells**
- **Pin-, function-, and JEDEC-compatible with MACH210**
- **Pin-compatible with MACH110, MACH215**

GENERAL DESCRIPTION

The MACHLV210A is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell. It is architecturally identical to the MACH210, with the addition of I/O pull-up resistors and low-voltage, low-power operation.

The MACHLV210A provides 3.3 V operation with low-power CMOS technology. At 10 mA maximum standby current, the MACHLV210A is ideal for low-power applications.

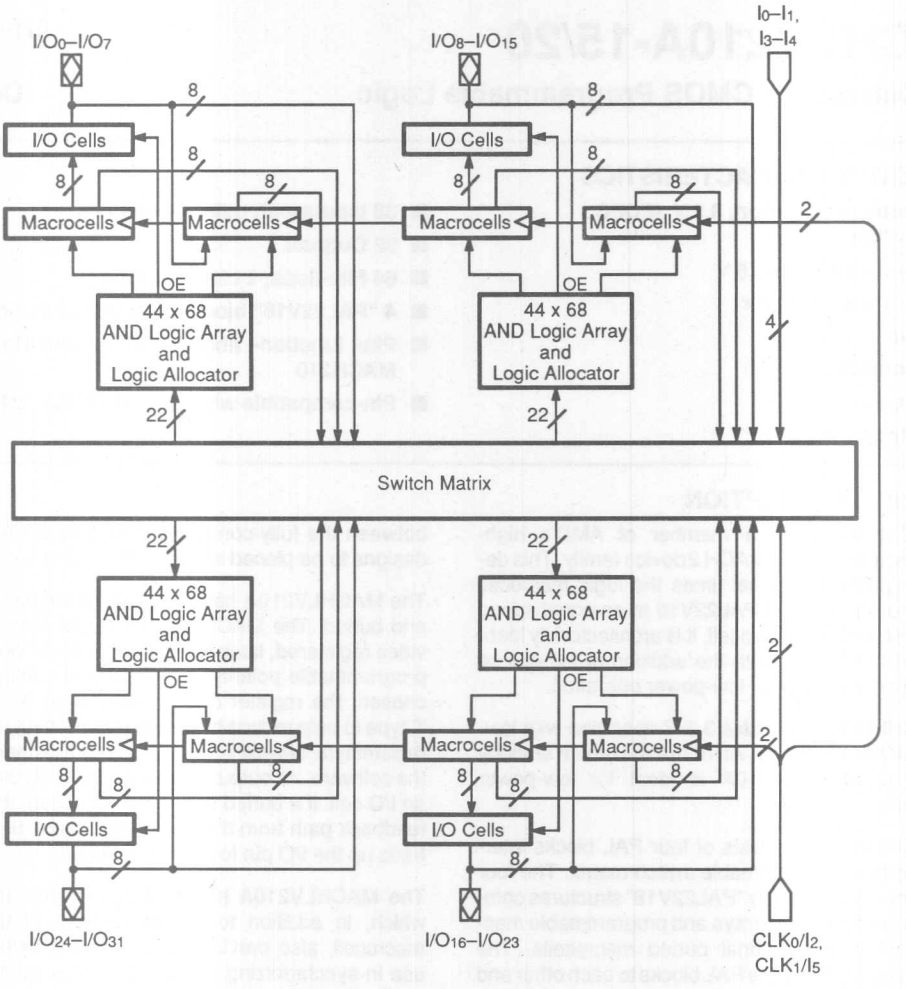
The MACHLV210A consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACHLV210A has two kinds of macrocell: output and buried. The MACHLV210A output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACHLV210A has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

Publication# C17908 Rev. A Amendment /0
Issue Date: June 1993

BLOCK DIAGRAM



17908A-1

FINAL

COM'L: -12/15/20

MACH220-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 96 Macrocells
- 12 ns t_{PD}
- 66.7 MHz f_{MAX} external
- 56 Inputs with pull-up resistors
- 48 Outputs
- 96 Flip-flops; 4 clock choices
- 8 PAL blocks with buried macrocells
- Pin-compatible with MACH120

GENERAL DESCRIPTION

The MACH220 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately nine times the logic macrocell capability of the popular PAL22V10 with no loss of speed.

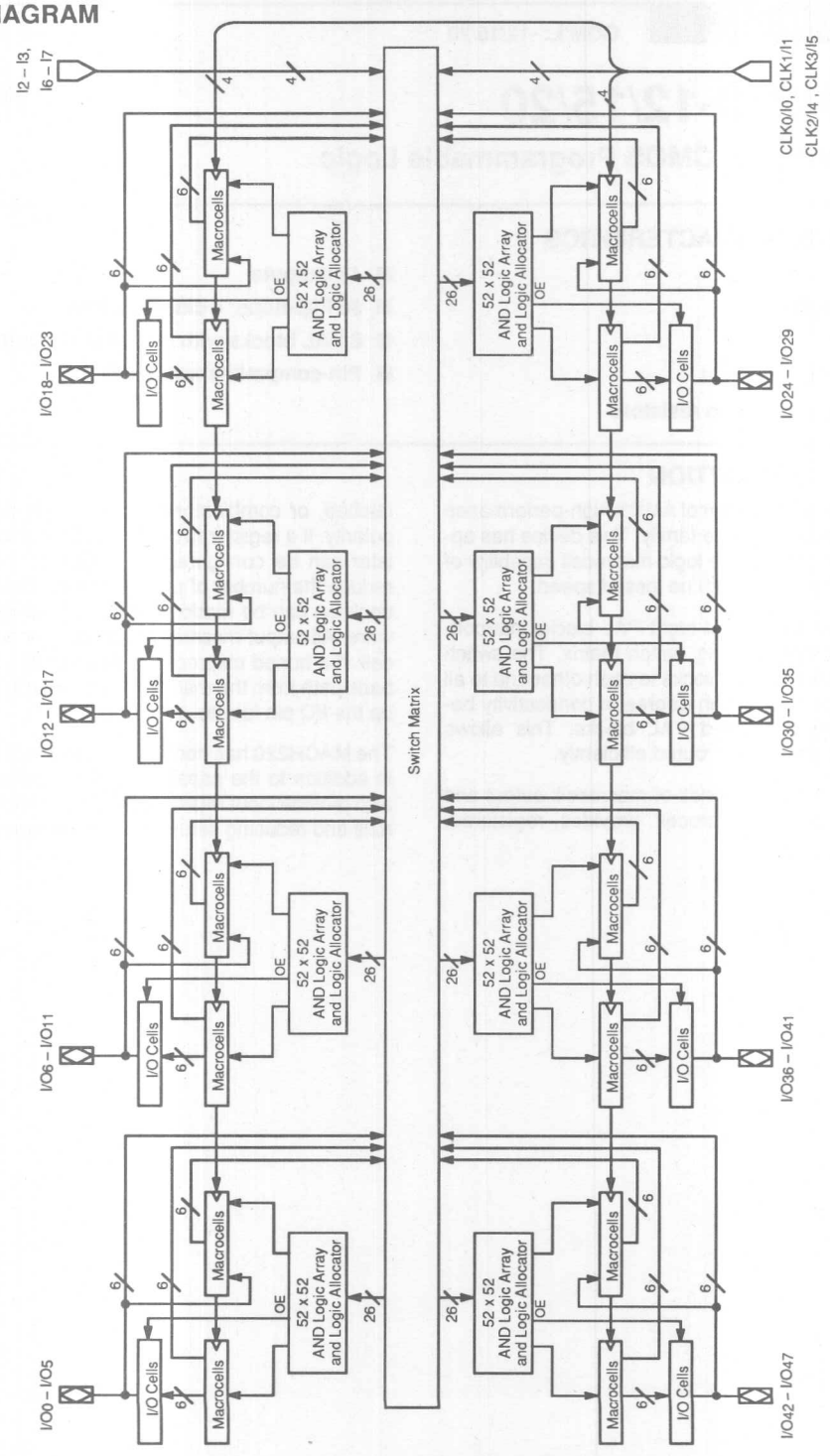
The MACH220 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH220 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH220 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

Publication# C14130 Rev. G Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM



FINAL | COM'L: -15/20

MACH230-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 128 Macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 70 Inputs
- 64 Outputs
- 128 Flip-flops; 4 clock choices
- 8 "PAL26V16" blocks with buried macrocells
- Pin-compatible with MACH130, MACH435

GENERAL DESCRIPTION

The MACH230 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately twelve times the logic macrocell capability of the popular PAL22V10 with no loss of speed.

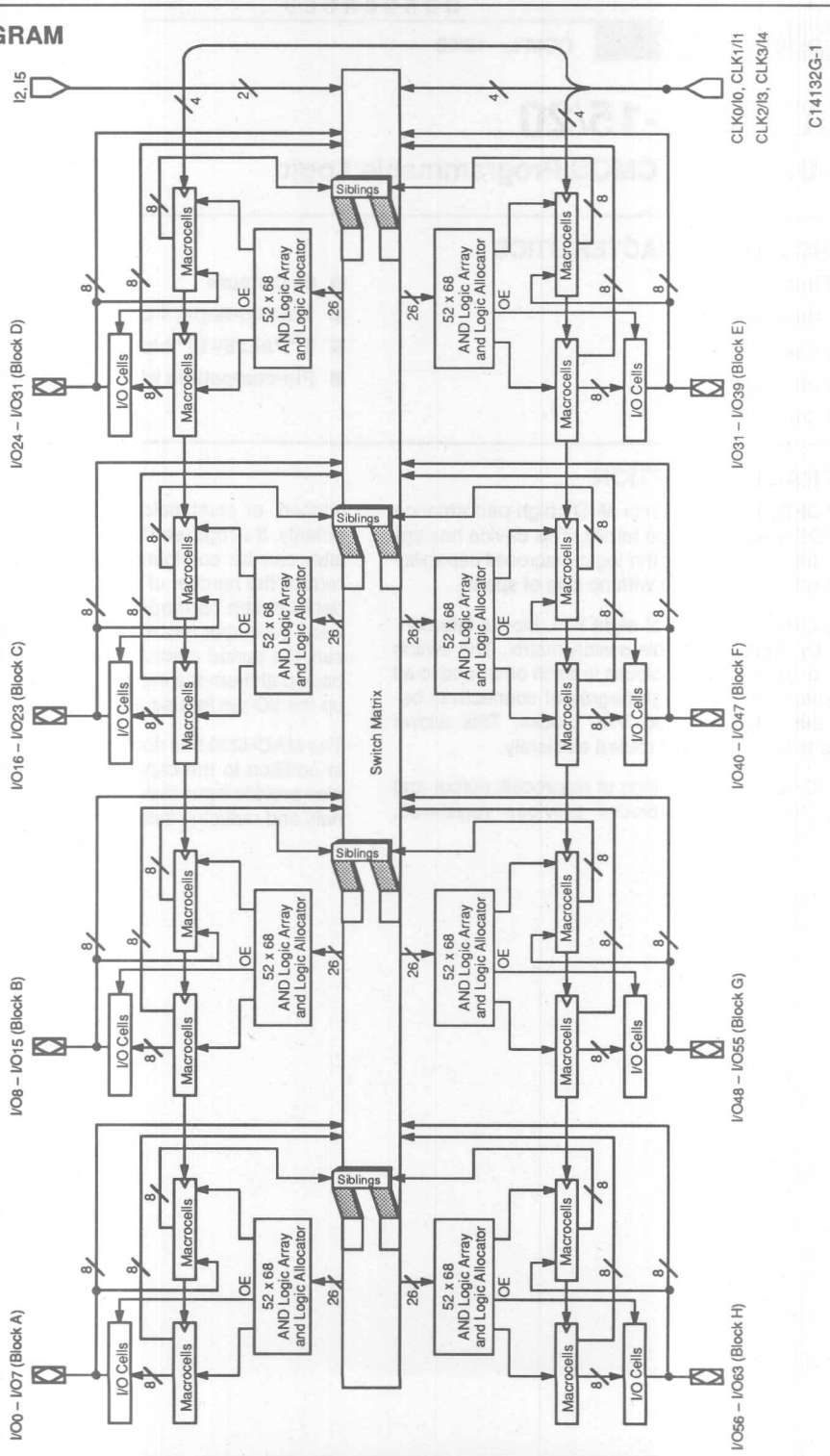
The MACH230 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH230 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH230 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

Publication# C14132 Rev. G Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM



CONDENSED

FINAL COM'L: -12/15/20

MACH215-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Output Macrocells
- 32 Input Macrocells
- Product terms for:
  - — Individual flip-flop clock
  - — Individual asynchronous reset, preset
  - — Individual output enable
- 12 ns t_{PD}
- 67 MHz f_{MAX} external
- 38 Inputs with pull-up resistors
- 32 Outputs
- 64 Flip-flops
- 4 "PAL22RA8" blocks with buried macrocells
- Pin-compatible with MACH110, MACH210

GENERAL DESCRIPTION

The MACH215 is a member of AMD's high-performance EE CMOS MACH device family. This device has approximately three times the capability of the popular PAL20RA10 with no loss of speed.

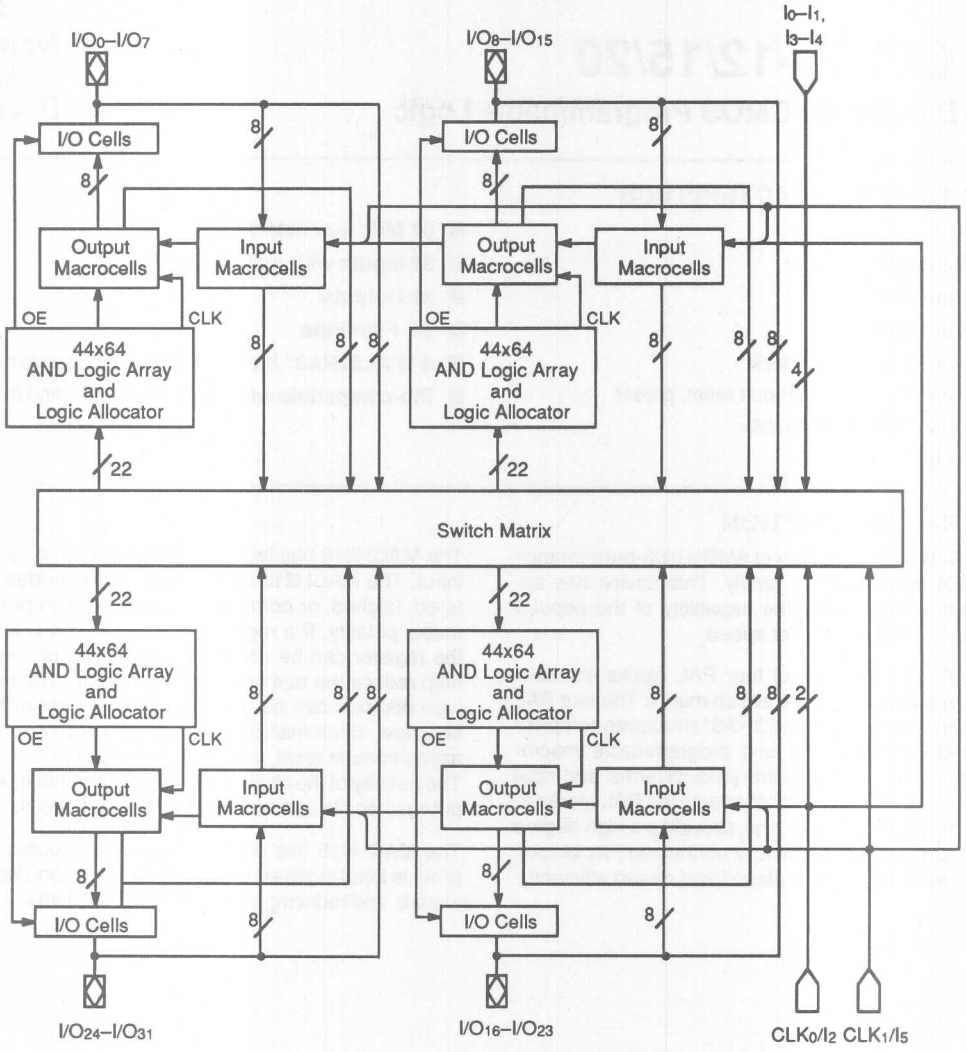
The MACH215 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22RA8" structures complete with product-term arrays and programmable macrocells, individual register control product terms, and input registers. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH215 has two kinds of macrocell: output and input. The MACH215 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. Each macrocell has its own dedicated clock, asynchronous reset, and asynchronous preset control. The polarity of the clock signal is programmable. All output macrocells can be connected to an I/O cell.

The MACH215 has dedicated input macrocells which provide input registers or latches for synchronizing input signals and reducing setup time requirements.

Publication# C16751 Rev. C Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM



C16751C-1

FINAL

MACH 3 and 4 Device Families

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density electrically-erasable CMOS PLD families**
- **Predictable design-independent 15- and 20-ns speeds**
- **High density, pin count**
  - — 3500–10,000 PLD Gates
  - — 84–208 Pins
  - — 96–384 Registers
- **Input and output switch matrices increase ability to hold a fixed pinout**
- **JTAG, 5-V in-circuit programmability on devices with more than 84 pins**
- **Synchronous and asynchronous modes available for each macrocell**
  - — Clock generator in each PAL block for programmable clocks, edges in either mode
  - — Individual clock, initialization product terms in asynchronous mode
- **Central, input, and output switch matrices**
  - — 100% Routability with 80% Utilization
- **Up to 20 product terms per function**
- **96–256 configurable macrocells**
  - — D/T/J-K/S-R Registers, latches
  - — Synchronous or asynchronous mode
  - — Programmable polarity
  - — Reset/preset swapping
- **XOR gate available**
- **Registered/latched inputs on MACH 4 series**
- **Extensive third-party software and programmer support through FusionPLD partners**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	PLD Gates	Max Inputs	Max Outputs	Max Flip-Flops	JTAG/ 5 V Prog	Speed
MACH 3 Family								
MACH355	132	96	3500	102	96	96	Y	15, 20
MACH 4 Family								
MACH435	84	128	5000	70	64	192	N	15, 20, Q-25
MACH445	100	128	5000	70	64	192	Y	15, 20
MACH465	208	256	10,000	146	128	384	Y	15, 20

GENERAL DESCRIPTION

The MACH (Macro Array CMOS High-speed/density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced electrically-erasable CMOS technology to offer a device with many times the logic capability of the industry's most popular existing PAL device solutions at comparable speed and cost.

The second-generation MACH devices provide approximately three times the density and register count, and two times the amount of I/O of the original MACH 1 and 2 families. By increasing the pin count, adding functionality, and improving routing, the MACH 3 and 4 families build upon the strength of the MACH architecture without sacrificing predictable timing.

Their unique architecture makes these devices ideal for replacing large amounts of TTL, PAL-device, glue, and gate-array logic. They are the first devices to provide such increased functionality with completely predictable, deterministic speed.

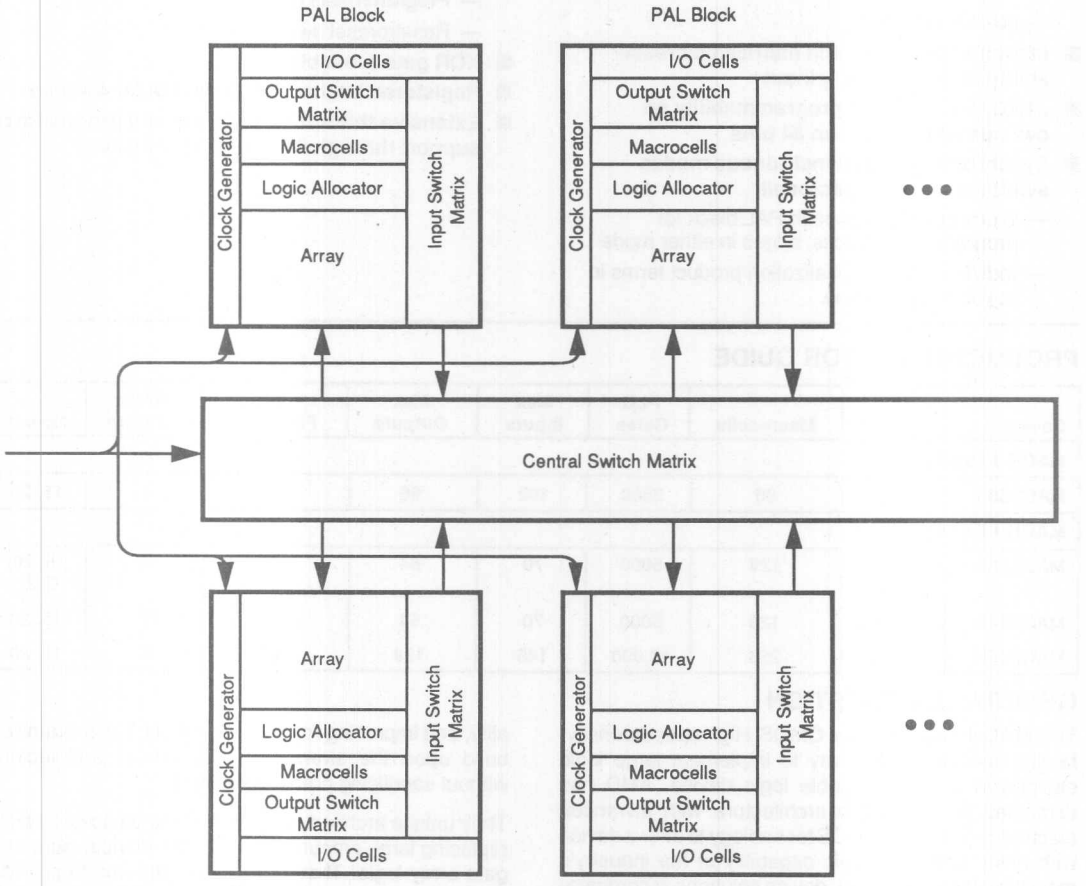
The MACH devices consist of PAL blocks interconnected by a programmable central switch matrix (Figure 1). Designs that consist of several intercon-

nected functional modules can be efficiently implemented by placing the modules into PAL blocks. Designs that are not as modular can also be readily implemented since the central switch matrix provides a very high level of connectivity between PAL blocks.

The use of input and output switch matrices allows logic to be implemented independent of pin connections. This allows greater flexibility when making initial pin assignments for PCB layout, or when trying to maintain the pinout through design changes. The internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

AMD's FusionPLD program allows MACH device designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide timely, accurate, quality support. This ensures that a designer does not have to buy a complete new set of tools for each new device, but rather can use the tools with which he or she is already familiar. The MACH devices can programmed on conventional PAL device programmers. Devices with pin counts greater than 84 have an additional 5-V programming algorithm option that can be implemented with the devices soldered onto the board.

MACH devices are manufactured using AMD's state-of-the-art advanced CMOS electrically-erasable process for high performance and logic density. CMOS EE technology provides 100% testability, reducing both prototype development costs and production costs.



17466A-1

Figure 1. MACH 3 and 4 Block Diagram

Design Methodology

Design tools for all MACH devices are widely available both from AMD and from third-party software vendors. AMD provides MACHXL™ software as a low-cost baseline tool set and works with third-party vendors to ensure broad MACH device support. MACHXL software is based on the popular PALASM® software package, with support dedicated to the higher-density MACH 3 and 4 devices. PAL devices, MACH 1 devices, and MACH 2 devices are supported by PALASM 4 software; MACH 3 and 4 devices are supported by MACHXL software. This allows designers to do MACH device designs using the same methodology that they would use to do any PLD or FPGA designs, whether with MACHXL software or any of the other popular PAL device or FPGA design packages.

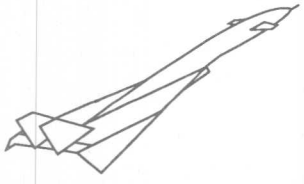
Design entry can be the same as that used for PAL, MACH 1, and MACH 2 devices. The basic logic processing steps are the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all approved software packages, and other options for simulating the timing and board-level behavior of the MACH devices are available. The end result is a JEDEC file that can be downloaded to a programmer for device configuration.

MACH device design methodology differs somewhat from that of a PAL device due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture, state machine equations, Boolean equations, or behavioral languages—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. The overall device utilization provided by the fitter will vary from design to design, but in general significantly higher utilization can be expected from the MACH 3 and 4 families than from the MACH 1 and 2 devices due to the additional routing resources. In addition, MACH 3 and 4 device designs with higher utilization are more likely to retain the same pinout when design changes are made since the output switch matrix allows a pin to be driven by any of a number of macrocells.

AMD recommends allowing the software to decide the best fit and pin placement automatically for the first design iteration. This will provide the best chance of fitting. With this approach, large designs can be implemented incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. It is possible to "pre-place" signals, and, given the plentiful routing resources, pre-placement is very likely to be successful on the MACH 3 and 4 families. However, the most successful design fit can still be achieved by allowing the software as much fitting flexibility as possible.

The design is partitioned and placed into the MACH device by the software so as not to affect the performance of the design. With designs that do not fit it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or passing through the device more than once), but those tradeoffs must be specifically requested, and any additional delays are entirely predictable.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. A major role of the input and output switch matrices is to allow such changes without impacting the original pinout. Certain design changes may make it impossible to maintain the original pinout, but designs can easily target 80% utilization without seriously jeopardizing the ability to make design changes and maintain pinout.



FINAL

COM'L: -15/20, Q-25

MACH435-15/20, Q-25

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **84 Pins in PLCC**
- **128 Macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **70 Inputs with pull-up resistors**
- **64 Outputs**
- **192 Flip-flops**
  - — 128 Macrocell flip-flops
  - — 64 Input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **Pin compatible with MACH130, MACH230**

GENERAL DESCRIPTION

The MACH435 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH435 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH435 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

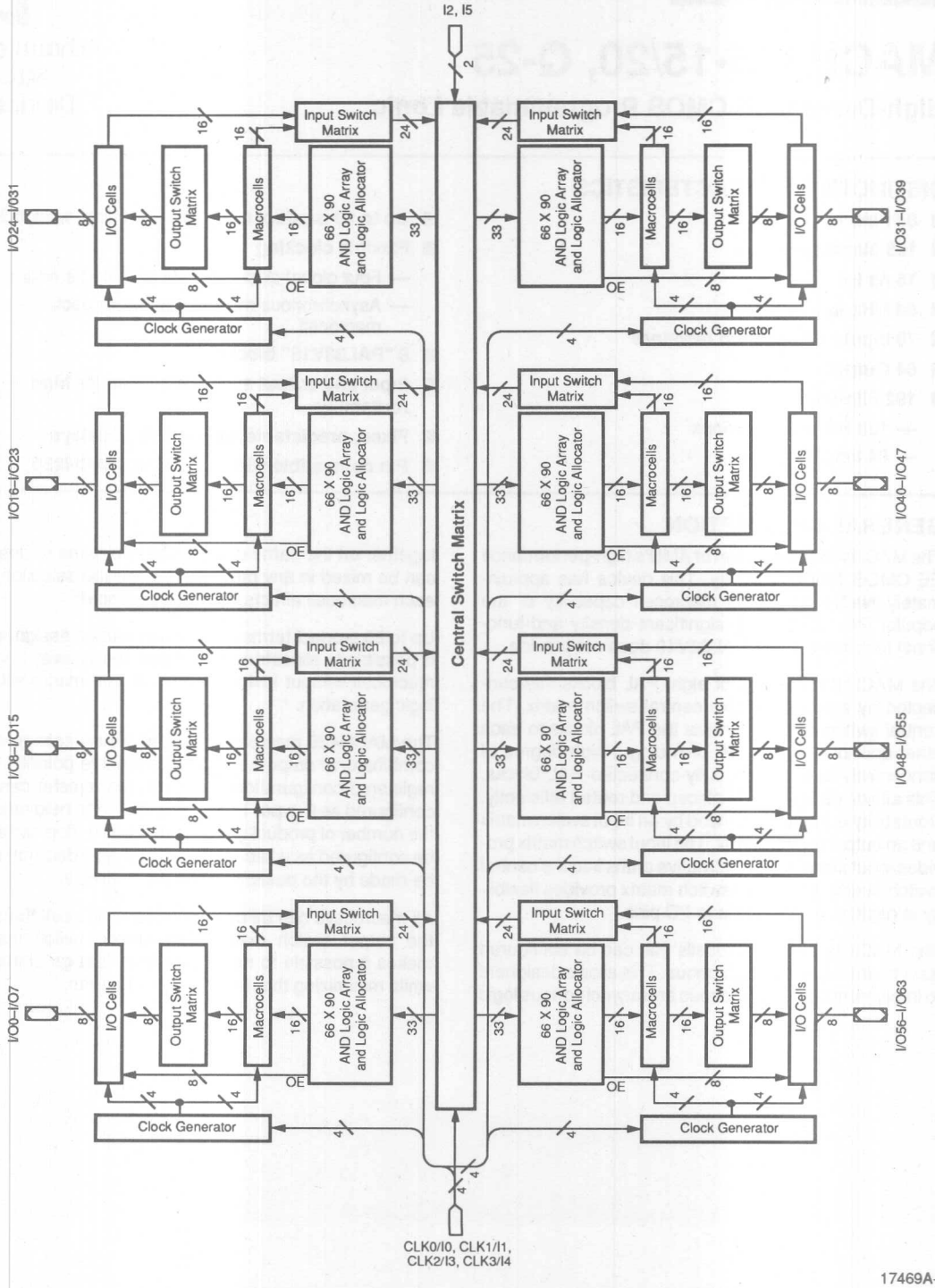
Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH435 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# C17469 Rev. B Amendment/0
Issue Date: June 1993

BLOCK DIAGRAM



17469A-1

ADVANCE INFORMATION COM'L: -15/20

MACH355-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 132 Pins in PQFP
- 96 Macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 102 Inputs with pull-up resistors
- 96 Outputs
- 96 Flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- JTAG, 5-V programmability
- 6 "PAL33V16" blocks
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays

GENERAL DESCRIPTION

The MACH355 is a member of AMD's high-performance EE CMOS MACH 3 family. This device has approximately nine times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH355 consists of six PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH355 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

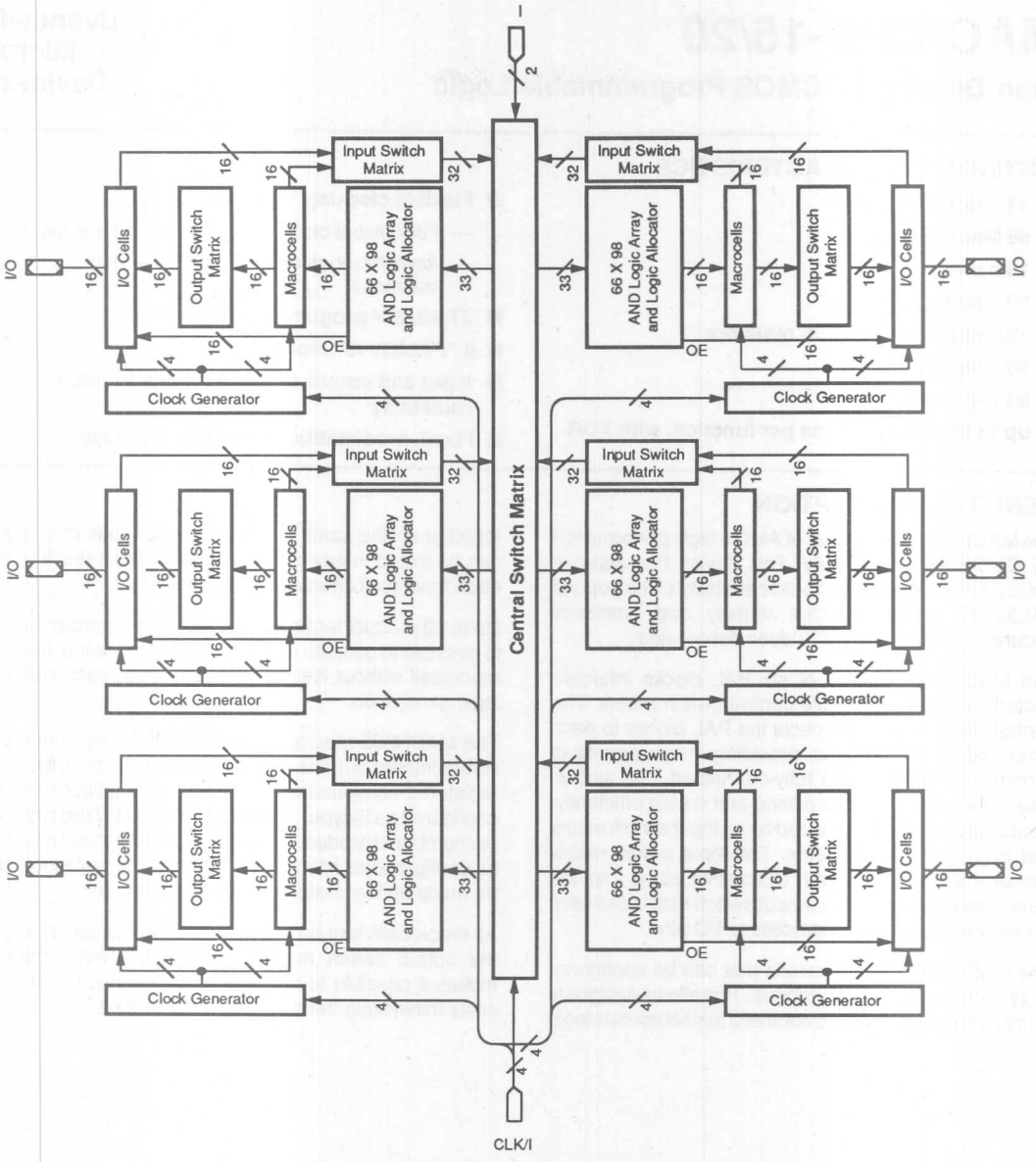
The MACH355 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# C17467 Rev. A Amendment /0
Issue Date: June 1993

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BLOCK DIAGRAM



C17467A-1

ADVANCE INFORMATION COM'L: -15/20

MACH445-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **100 pins in PQFP**
- **MACH435 with JTAG, 5-V programmability**
- **128 Macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **70 Inputs with pull-up resistors**
- **64 Outputs**
- **192 Flip-flops**
  - — 128 Macrocell flip-flops
  - — 64 Input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **JEDEC-file compatible with MACH435**

GENERAL DESCRIPTION

The MACH445 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide. It is architecturally identical to the MACH435, with the addition of JTAG and 5-V programmability capabilities.

The MACH445 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH445 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

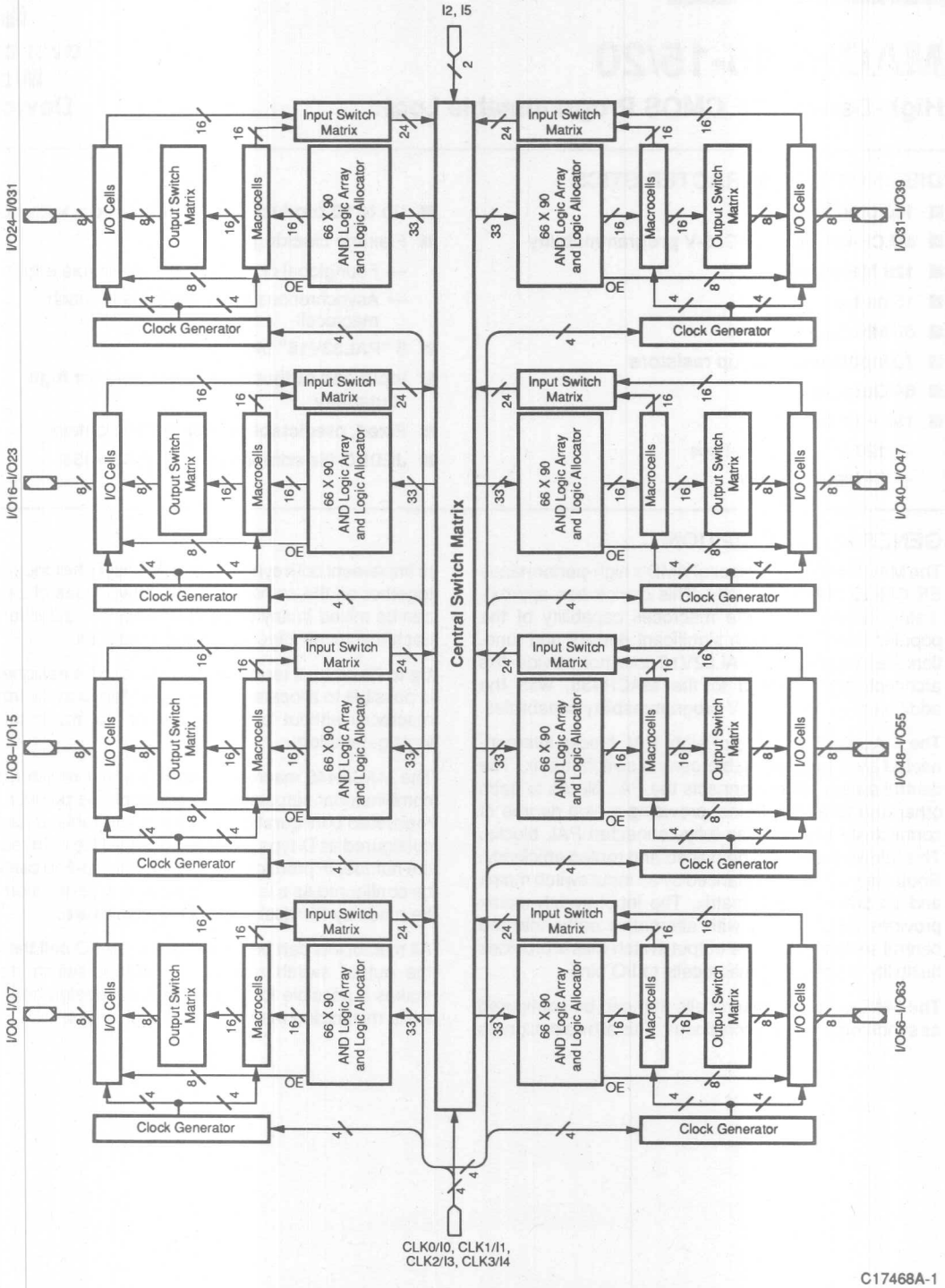
The MACH445 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# C17468 Rev. A Amendment /0
Issue Date: June 1993

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BLOCK DIAGRAM



C17468A-1

ADVANCE INFORMATION COM'L: -15/20

MACH465-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **208 pins in PQFP**
- **256 macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **146 Inputs with pull-up resistors**
- **128 Outputs**
- **384 Flip-flops**
  - — 256 Macrocell flip-flops
  - — 128 Input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **16 "PAL34V16" blocks**
- **JTAG, 5-V programmability**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**

GENERAL DESCRIPTION

The MACH465 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately 25 times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH465 consists of 16 PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH465 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

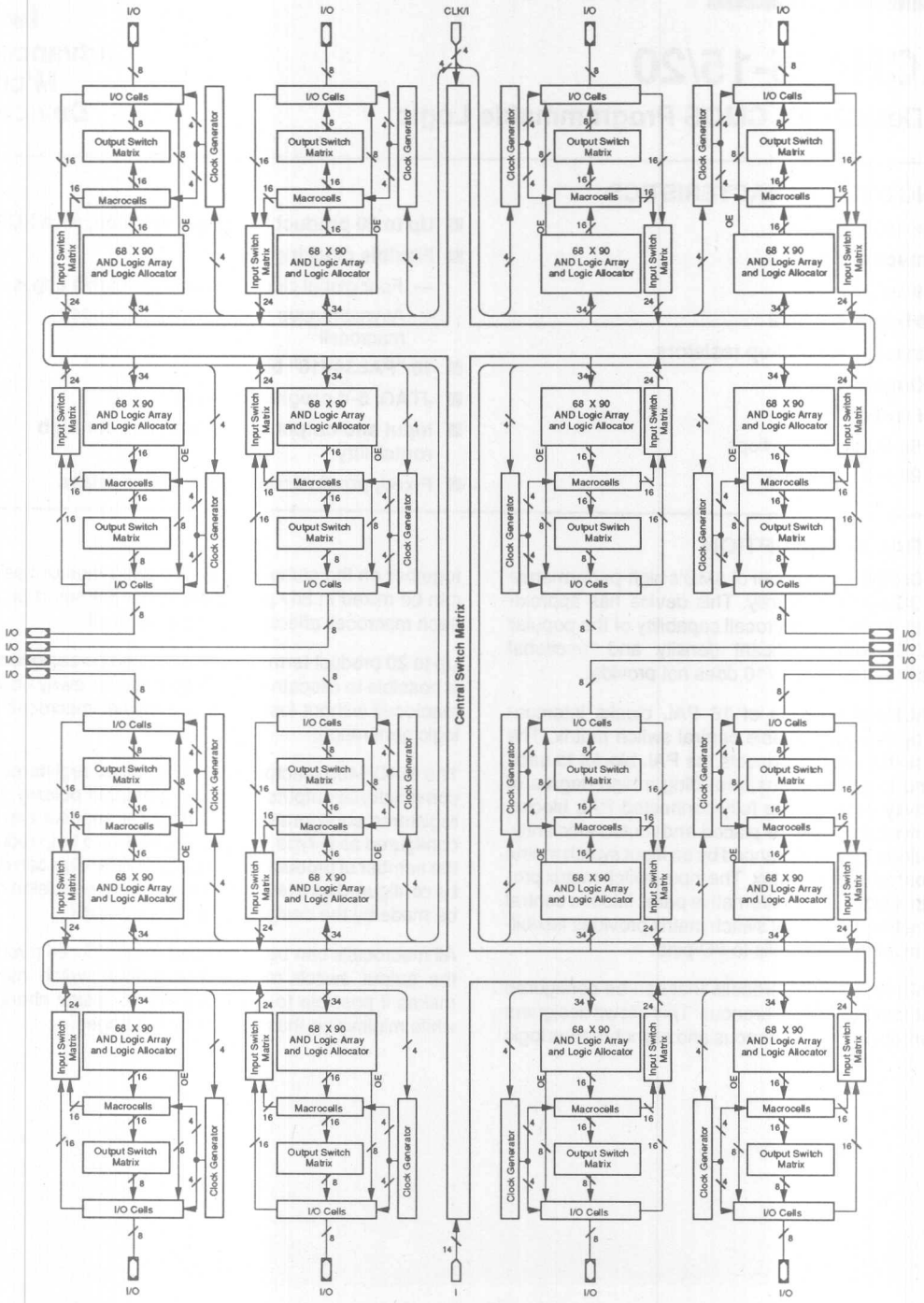
The MACH465 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# C17470 Rev. A Amendment /0
Issue Date: June 1993

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BLOCK DIAGRAM



C17470A-1

CHAPTER

4 GENERAL INFORMATION

Inside AMD's CMOS PLD Technology 4-3
Military PAL Devices 4-43
Military ProPAL Devices 4-52
Electrical Characteristic Definitions 4-54
f_{MAX} Parameters 4-57
Physical Dimensions 4-58


IMPORTANT
NOTES

Inside AMD's CMOS PLD Technology

Application Note
by Bryon Moyer, Applications Manager, Advanced Micro Devices, Inc.

Advanced Micro Devices

TECHNOLOGY DESCRIPTION

The EE CMOS technology used by AMD in programmable logic is a single-poly, double-metal n-well process. It has been optimized for high-speed programmable logic devices, which do not have the same density constraints that memories have. The basic characteristics of the EE4 process are:

- CMOS, n-well
- Grounded substrate
- Single-poly, dual metal
- 1.2 µm minimum feature
- 0.8 µm gate length (L_{eff})
- 180Å gate oxide thickness
- 90Å tunnel oxide thickness
- 1.4 µm contact dimension on wafer
- 3.2 µm metal 1 pitch
- 3.8 µm metal 2 pitch

The EE5 process is similar, except that L_{eff} is 0.65 µm.

CMOS PLDs use standard CMOS logic internally, with the addition of a programmable array. The output buffers of most devices are designed to be compatible with TTL circuits, and therefore have n-channel enhancement pull-up transistors. Exceptions to this are the zero-power devices and the PALCE610H-15, which have rail-to-rail switching outputs provided by a p-channel pull-up in the output buffer.

AMD's CMOS process for programmable logic is simplified by the absence of standard depletion-mode transistors in the more advanced processes. Depletion mode transistors are a vestige of NMOS design, and are not really needed. This results in the elimination of a mask and implant step, reducing the process cost and simplifying the structure.

Transistor Cross-Section

Figure 1 shows a cross-section of a basic inverter. This is a very straightforward structure. The gates consist of poly-silicon; the other connections are made with metal.

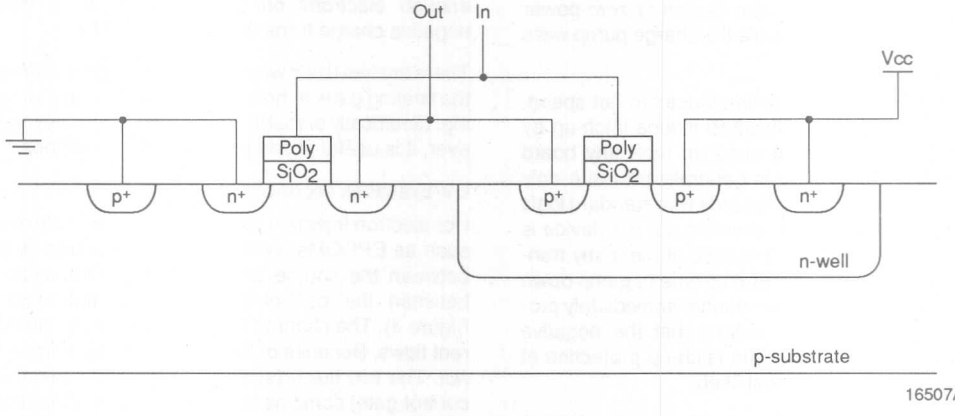
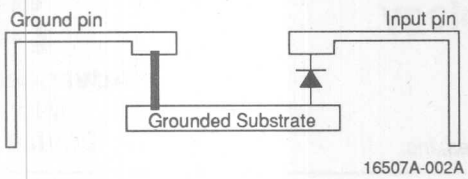


Figure 1. CMOS Inverter Cross-Section

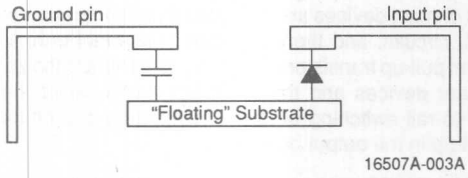
Substrate Voltage

There are two basic substrate configurations for CMOS PLDs: grounded substrate and floating (or negative) substrate, as shown in Figure 2. In the first case, the substrate is connected to ground; no voltage on the chip is more negative than ground. The substrate is directly hard-wired to the ground pin. In the second case, the substrate is capacitively coupled to ground. A charge pump pumps the substrate to a negative voltage, typically –3 V.

Publication# **16507** Rev. **A** Amendment /**0**
Issue Date: **February 1993**



a.



b.

Figure 2. Substrate Configurations: a. Grounded; b. Floating

AMD's CMOS process uses a grounded substrate. This means that no large charge pump is used to pump the substrate negative. This technology has several benefits. Providing effective clamp diodes is easier if the substrate is grounded; this helps protect against negative overshoot. A grounded substrate permits quieter operation on boards where the oscillation of a charge pump can radiate and disturb sensitive circuits. Also, this approach permits the design of zero-power parts that would not be possible if a charge pump were constantly running.

A negative substrate is sometimes used to get speed, and also makes it more difficult to induce latch-up by making the substrate more negative than any board voltage. However, latch-up is generally an issue only during power-up on standard boards with standard logic drivers. While the device is powering up, the device is most vulnerable to latch-up because of the many transients occurring. However, it takes time to pump down the substrate, so the substrate cannot immediately protect against latch-up. This means that the negative substrate approach provides no latch-up protection at the time when latch-up is most likely.

The only signal excursions into negative territory during normal operation will be from overshoot, and overshoot cannot induce latch-up because there is not enough energy. Negative overshoot is discussed in more detail below.

Thus the negative substrate has no practical advantages over a grounded substrate, and lacks the advantages of a grounded substrate. For this reason, none of AMD's CMOS PLDs use a negative substrate.

Erasable Technology

Any erasable CMOS technology is based upon the concept of stored charge. The charge is stored on a transistor with a *floating gate*—that is, a gate that has no connection. The transistor actually has two gates: one that floats, and one that acts as a control gate. The control gate is used to establish the field across the floating gate (see Figure 3).

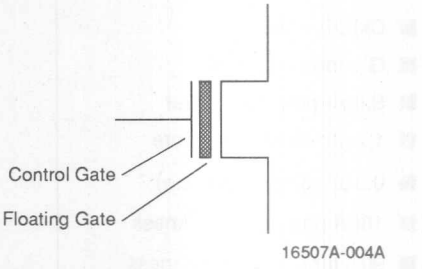


Figure 3. Floating-Gate MOS Transistor

In the programmed state, there is a net deficit of electrons in the floating gate. The resulting positive charge turns the transistor ON. In the erased state, there are enough electrons on the control gate so that the negative charge turns the transistor OFF.

There are two basic ways of transferring the charge onto the floating gate: a) hot electron injection, and b) tunneling. Electrically erasable devices rely on tunneling; however, it is useful to compare these two methods.

UV-Erasable Technology

Hot electron injection is used for *UV-erasable* devices, such as EPROMs. With this scheme, a bias is set up between the source and drain of the transistor, and between the control gate and the substrate (see Figure 4). The channel is pinched off, and a strong current flows. Because of the high fields, the electrons are *hot*. The two fields (source-to-drain, and substrate-to-control-gate) combine to form a field in a diagonal direction, but because of the oxide barrier, electrons cannot cross in that direction. Occasionally, electrons acquire enough energy to cross the barrier in the shortest direction: from the channel to the floating gate. This is referred to as *hot electron injection*.

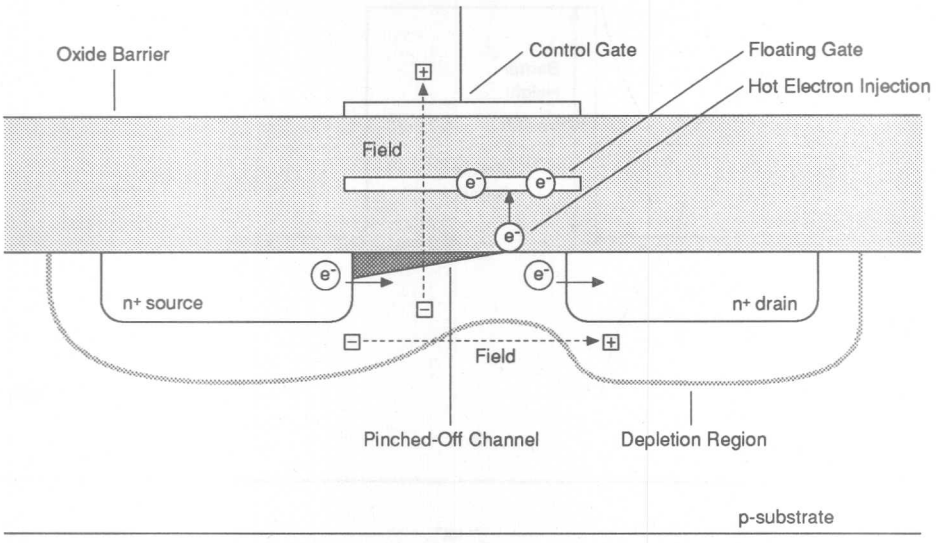


Figure 4. Programming by Hot-Electron Injection

Figure 5 shows the energy band diagram for the gate/channel interface. Because the fields give the electrons more energy, more electrons can cross the oxide barrier. The height of the barrier determines how easily charge can be transferred across.

Once an electron is on the other side of the oxide, it is on the floating gate, with no path. It is therefore effectively trapped, and remains there. During programming, large fields are set up so that a significant number of electrons are injected.

Erasing these devices requires exposure to ultraviolet light. The energy from the ultraviolet light causes the electrons to cross back over the oxide barrier, erasing the device. For this to happen, the device package must have a window that lets the ultraviolet light pass through.

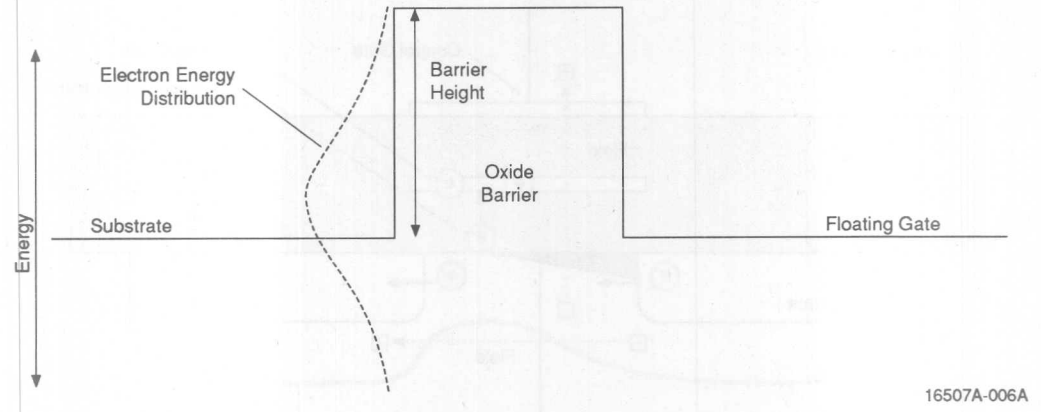
UV-erasable technology has a few distinct drawbacks. The fact that the parts require a window to be erased makes the devices much more expensive. Although they are usually available in plastic *one-time-programmable* (OTP) packages, they are then not erasable, and have no advantage over fuse technology. In addition, windowed devices take about 90 minutes to erase. This limits the number of times that the device can practically be reprogrammed and tested during manufacturing, limiting the amount of extra quality that can be provided by the erasability feature.

Electrically Erasable Technology

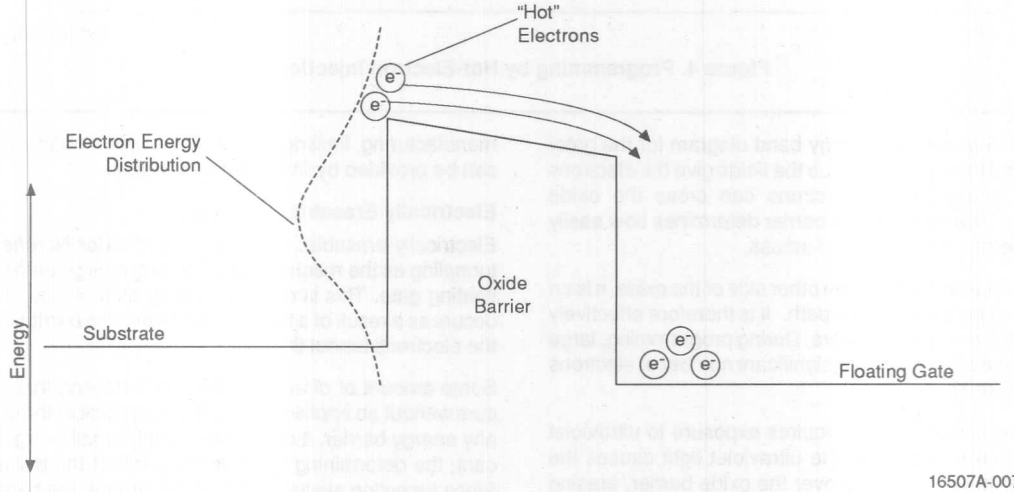
Electrically-erasable devices use *Fowler-Nordheim* tunneling as the mechanism for getting charge onto the floating gate. This is defined roughly as tunneling that occurs as a result of a field placed across the barrier that the electrons tunnel through.

Some amount of *direct* tunneling, or tunneling that occurs without an applied field, is always possible through any energy barrier. It may be extremely small or significant; the determining factor is the width of the barrier. Since tunneling electrons are going through the barrier instead of over it, the height of the barrier does not affect the amount of tunneling.

For an electrically-erasable cell, the tunnel oxide is about one third the thickness of the oxide of a UV-erasable part; therefore tunneling occurs at relatively low fields. Even so, the field used to cause tunneling is about five times the field used to cause hot-electron injection for UV parts. Note that tunneling is theoretically possible on a UV part, but a very high field is required, and the normal electron injection would swamp out any tunneling that would occur.



a.

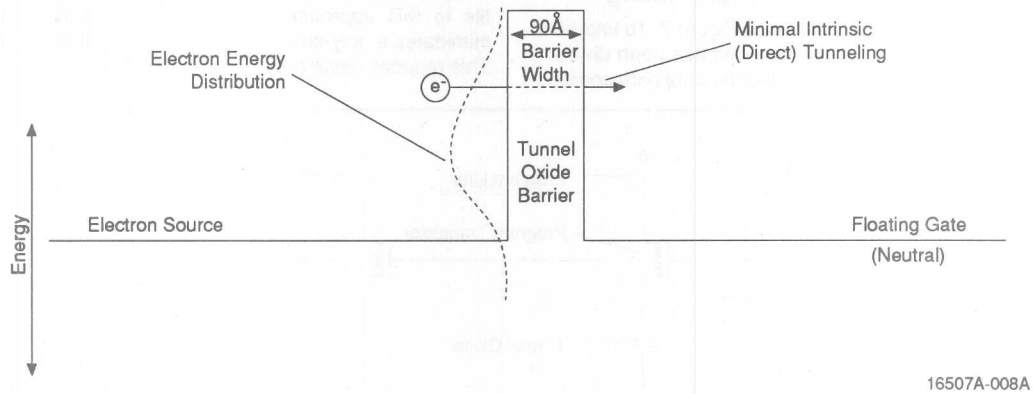


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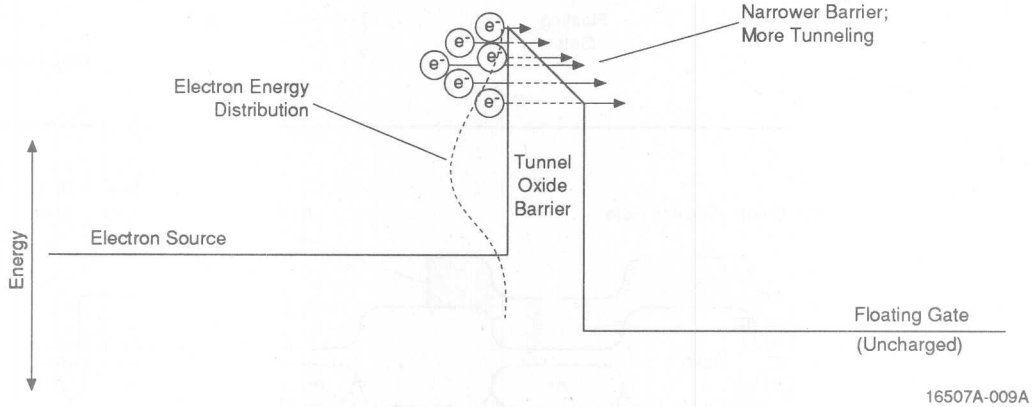
Figure 5. Energy Band Diagrams: a. Neutral Floating Gate; b. Hot-Electron Injection

Fowler-Nordheim tunneling involves placing a potential across the barrier, which distorts the band diagram as shown in Figure 6. The "angle" caused by the applied potential effectively thins part of the already-thin barrier, making tunneling easier. It is this tunneling under bias that is used to program electrically-erasable devices. Note that by reversing the bias, the tunneling can occur just as well in the opposite direction. This is what makes electrical erasure possible.

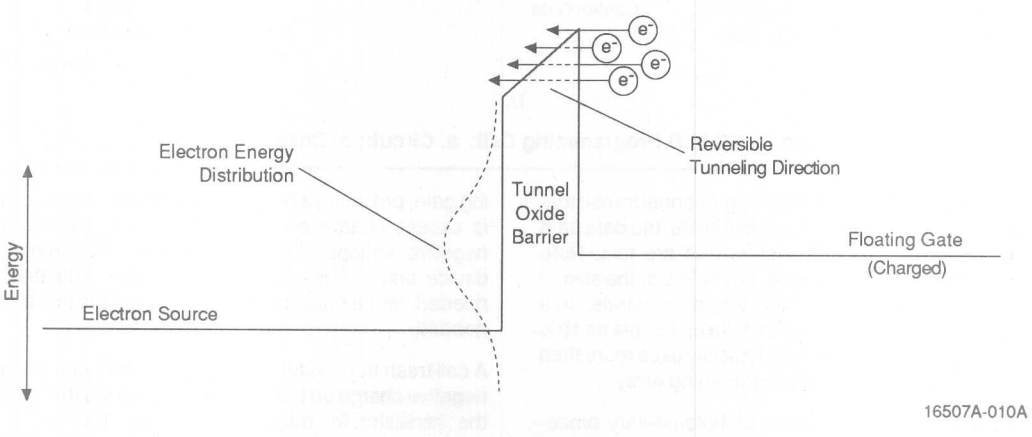
Electrical erasure has advantages over UV erasure both in cost and quality. Because the erasure is electrical, no expensive window is required in the package. This makes erasability cost-effective even in high-volume production quantities. In addition, the fast erasure allows AMD to reprogram the device many times, allowing many more paths to be tested than can be tested in a UV part. This provides much higher quality, especially in higher-density devices.



a.



b.



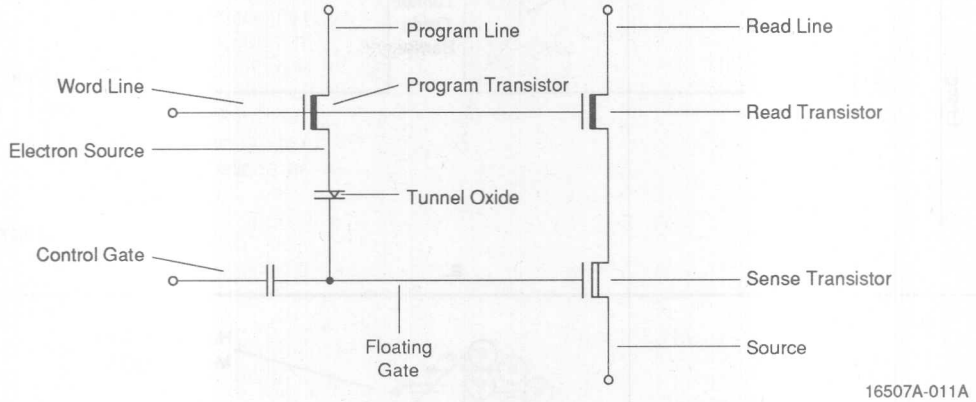
c.

Figure 6. Energy Band Diagrams: a. Direct Tunneling; b. Fowler-Nordheim Charging; c. Fowler-Nordheim Discharging

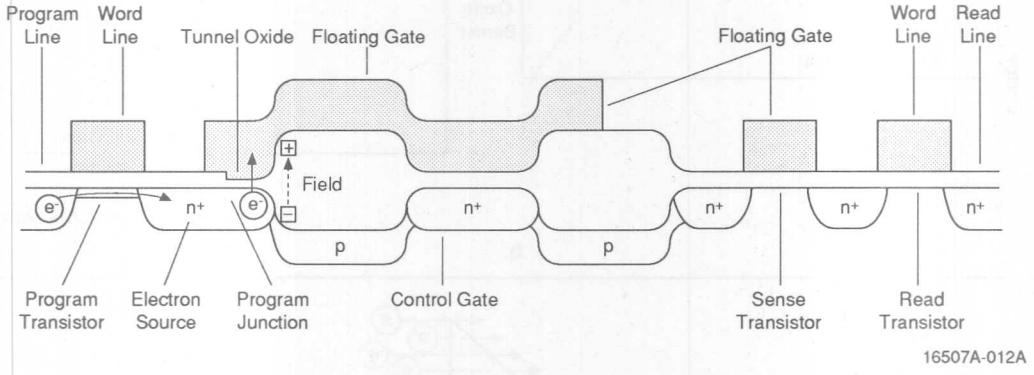
Cell Configuration and Programming

The programming cell is shown in Figure 7. To improve device speed, the programming cell has been divided into the programming portion and the data path portion.

In addition to speed, there are a number of other benefits to this approach. At the most basic level, this eliminates a poly-silicon layer, simplifying the process. This reduces costs and improves reliability.



a.



b.

Figure 7. EE PLD Programming Cell: a. Circuit; b. Cross-Section

The programming half requires long-channel transistors capable of sustaining high electrical fields; the data path requires short-channel transistors that are fast. Note that this does take more space, but in PLDs, the size of the cell is not a limiting factor as it is in memories. In a PLD, the programming array can take up as little as 10% of the die area, while a memory typically uses more than 90% of the die area for the programming array.

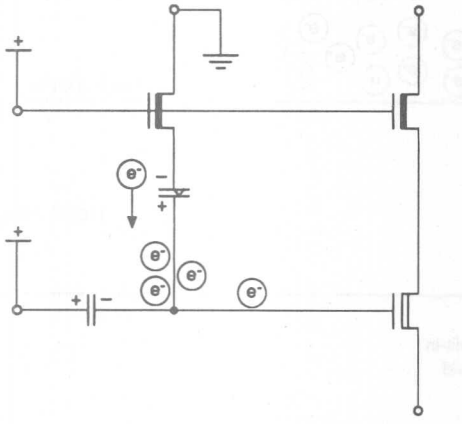
Programming and erasure are complementary procedures in EE technology. However, the sense of programming and the sense of erasing are perhaps opposite to what one might assume. A cell is considered to be programmed if there is a charge deficit on the floating gate, providing a positive voltage; it is erased if there is excess charge on the floating gate, generating a negative voltage. This means that programming a device only requires turning ON those cells that are needed, rather than turning off all of the cells that are not needed.

A cell fresh from wafer fabrication has no net positive or negative charge on the gate. To balance the threshold of the transistor for reliable turn-on and turn-off, a *cell implant* is used to center the threshold voltage near 0 V. Programming and erasing involve either removing electrons from the conduction bands of the poly-silicon gate or adding excess electrons, providing a net charge that

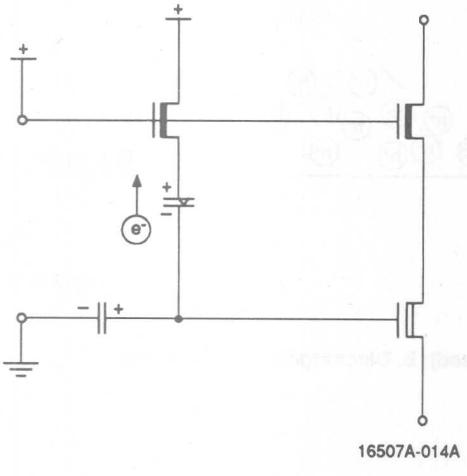
will move the gate voltage solidly on one side or the other of the threshold voltage.

When programming or erasing the device, a voltage is applied between the program and control gate nodes. The direction of the voltage determines whether the cell is erased or programmed.

When erasing, the control gate is given a positive voltage, and the program node is grounded. This attracts electrons from the program transistor across the tunnel oxide to the floating gate, turning the read transistor OFF (see Figure 8a).



a.



b.

Figure 8. Cell Biasing: a. Charging; b. Discharging

When programming the cell, the program node voltage is elevated, and the control gate is grounded, reversing the electron flow, as indicated in Figure 8b. Enough electrons flow off the floating gate to leave a net positive charge; this turns the transistor ON.

AMD has modified the programming cell to increase programming efficiency and has a patent on the resulting circuit. On traditional devices, the source node is grounded during programming. On AMD's devices, the source node is raised to the same potential as the control gate, as shown in Figure 9. This increases the *coupling ratio* of the cell. The coupling ratio is the percentage of the applied field that appears across the tunnel oxide. When the source is grounded, the field across the tunnel oxide is reduced (since there is another capacitor in parallel with the tunnel oxide). By raising the source voltage, more of the field is available for programming. The coupling ratio can therefore be thought of as a measure of the programming efficiency; since the efficiency is higher, lower voltages are required for programming.

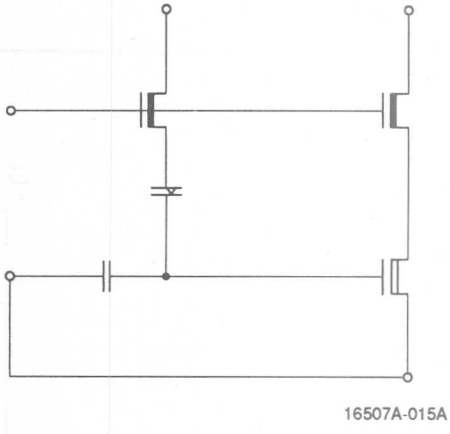
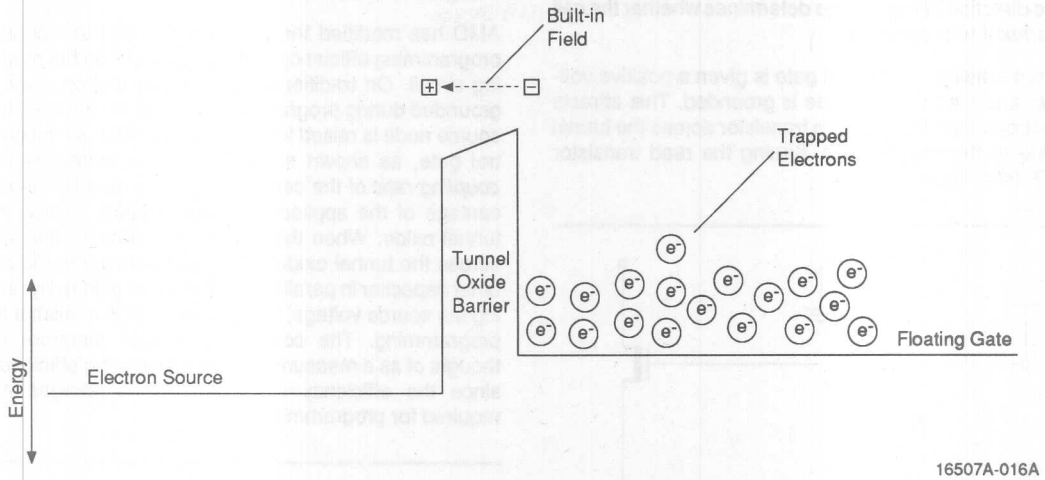


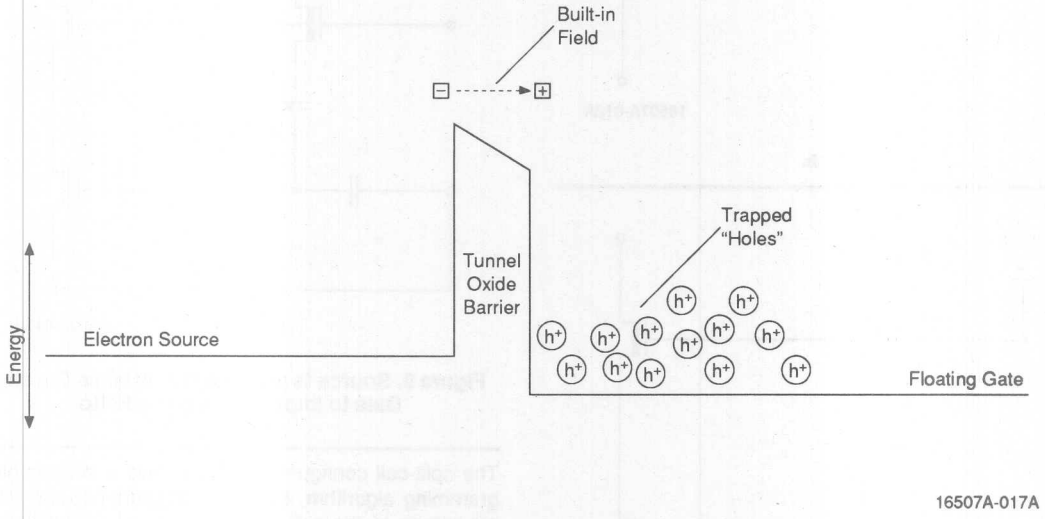
Figure 9. Source is at Same Potential as Control Gate to Improve Coupling Ratio

The split-cell configuration also allows a simpler programming algorithm, since the programmer can take advantage of the self-limiting nature of programming and erasure. The split cell places the read cell gate and the floating cell gate in "parallel" with each other. Therefore the floating cell can be either completely charged (with a net excess of electrons) or completely discharged (with a net deficit of electrons, or an excess of holes), as shown in the energy diagrams in Figure 10. This is simple to do, since the electrons that have crossed the barrier set up a field that opposes further tunneling. As more electrons cross the barrier the opposing field grows strong enough to block more

electrons from tunneling (Figure 11). Regardless of the state of the floating cell, the select line will turn on or off the read transistor; the cell will only be read, however, if both the read transistor and the the floating transistor are ON.

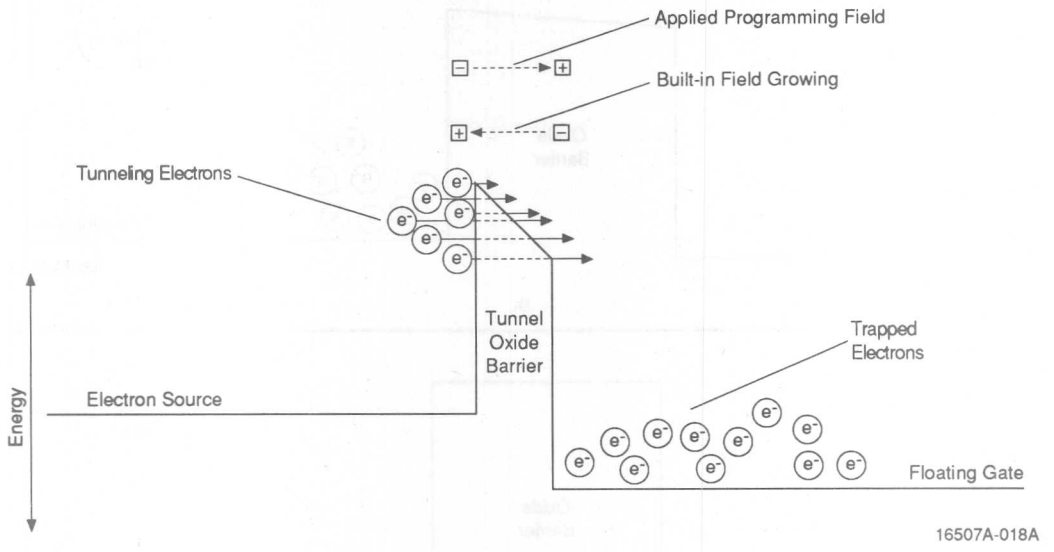


a.

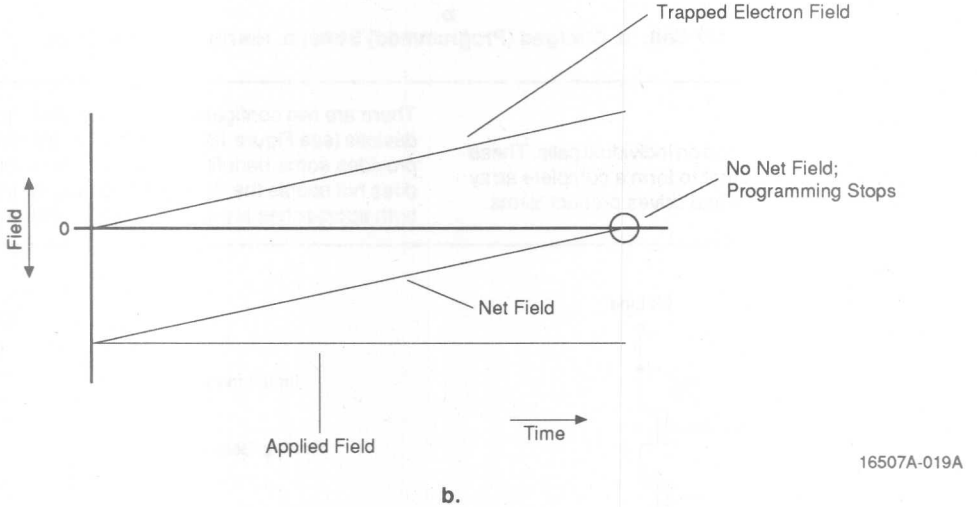


b.

Figure 10. Stable EE Cell: a. Charged (Erased); b. Discharged (Programmed)



a.



b.

Figure 11. Self-Limiting Programming and Erasure: a. Energy Band Diagram; b. Fields vs Time

In standard one-transistor cells, the two gates are actually in "series". If the floating gate is charged, then the transistor is OFF, regardless of the state of the select line. In order to read the cell, the floating gate has to be neutralized so that the select line controls the transistor (Figure 12). If the floating gate were completely discharged, then the transistor would be ON regardless of the state of the select line. The programming algorithm is therefore more complicated, since the amount of charge removed must be monitored to ensure that just enough charge is removed to neutralize the floating gate.

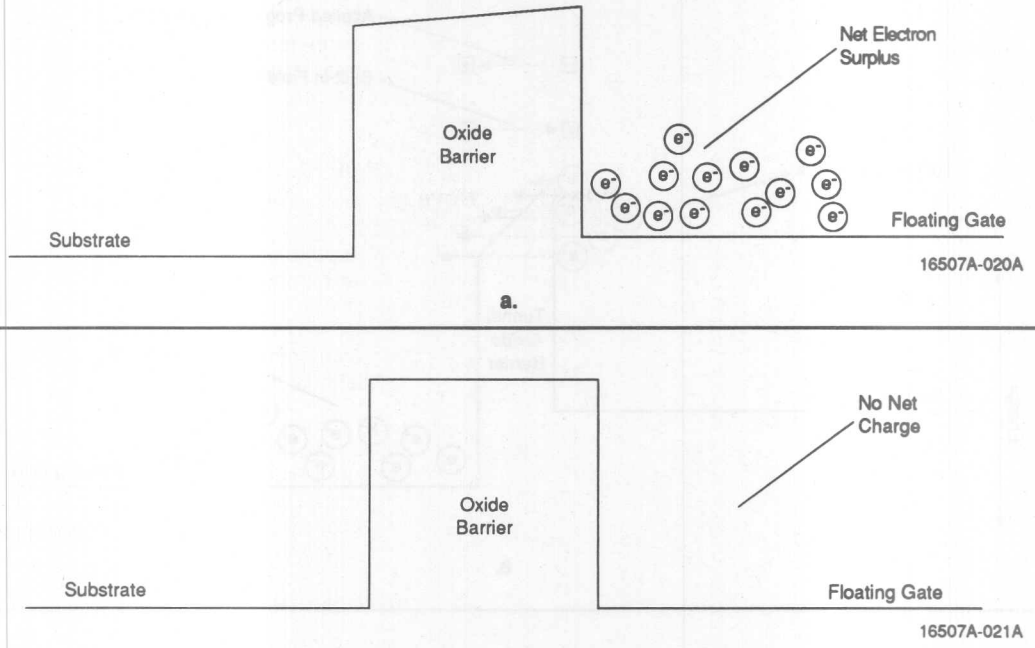


Figure 12. UV Cell: a. Charged (Programmed) State; b. Neutral (Erased) State

Array Configuration

The discussion above focused on individual cells. These cells must be hooked together to form a complete array that is driven by input lines and drives product terms.

There are two configurations used in AMD's EE CMOS devices (see Figure 13). The configuration in Figure 13b provides some benefit because the parasitic capacitor does not couple the input line and the product term, but both approaches are actively used in designs.

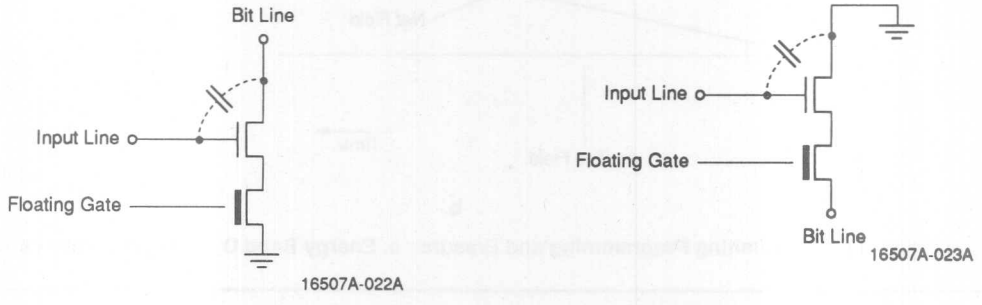


Figure 13. Two Array Configurations: a. Bit Line at the Drain; b. Bit Line at the Source

PROGRAM INTEGRITY

Reliable programming of PLDs requires the use of well-calibrated, quality programming equipment. To ensure that the device is correctly programmed, the correct voltages and times must be applied.

As discussed above, it is impossible to over-charge or over-discharge the programming cell since the mechanism is self-limiting. This provides more leeway and makes the programming algorithms less sensitive to programmer variations. This ultimately provides higher, more consistent programming yields under real-life production programming conditions.

However, if the cell is under-programmed or under-erased, an insufficient amount of charge might transfer onto or off of the floating gate. When programming, this might not turn the read cell ON sufficiently, potentially slowing down the device. In the case of erasure, the read cell might be partially ON if it is not completely erased. This may cause "disconnected" inputs to appear partially connected. Thus it is important to ensure that the programming pulsewidths are long enough to provide adequate programming.

If the programming voltages are slightly inaccurate, CMOS devices often can still be programmed correctly. However, excessive voltage might cause device damage if breakdown voltages are exceeded. Extremely low voltages might fail to engage the programming circuitry completely.

Because of the need for accurate programming, and for ensuring that the programming algorithms are up-to-date, we certify programmers that meet strict criteria for all products through our FusionPLD[SM] program. AMD guarantees the performance of any device when programmed on an approved programmer. For a list of FusionPLD partners, please refer to the FusionPLD Catalog.

Data Retention

In an electrically erasable device, the floating cell is programmed by forcing electrons to tunnel through the tunnel oxide into the floating gate. Ideally, these trapped electrons mean that the device remains programmed indefinitely. Actually, the charge cannot remain indefinitely, but its lifetime is normally extremely long. The stability of the program charge is called *data retention*; that is, the ability of the device to retain its charge as programmed.

There are two basic leakage mechanisms: direct tunneling and thermal leakage. These mechanisms occur independent of whether the cell was programmed by electron injection or tunneling. The amount of direct tunneling is a function of the potential across the tunnel oxide, and is generally very low. Leakage is normally dominated by thermal charge decay.

On one side of the energy barrier, there are electrons with a distribution of energies (see Figure 14). Some have enough energy to escape over the top of the barrier. As the temperature is raised, more electrons achieve the energy required to overcome the barrier.

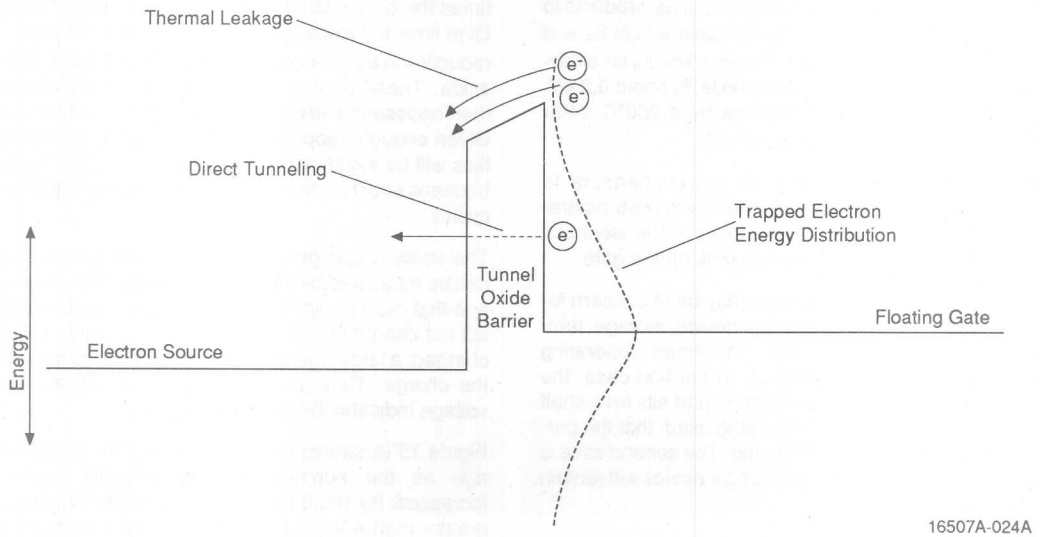


Figure 14. Data Loss Mechanisms

The tendency of the gate to leak can be modelled as an Arrhenius function, which means the formula for the programming "decay time" t_d has the form:

$$t_d = Ke^{E_a/kT}$$

where

E_a is the intrinsic *activation energy*

T is the temperature in Kelvin
k is Boltzmann's constant
K is a scaling constant.

If we can measure the rate at two known temperatures, then:

$$\frac{t_{d1}}{t_{d2}} = \frac{Ke^{E_a/kT_1}}{Ke^{E_a/kT_2}}$$

Note that the constant K drops out, so we need not be concerned with it's specific value. From this we find that

$$E_a = \frac{T_2 \ln t_{d1} - T_1 \ln t_{d2}}{k T_1 T_2}$$

This lets us measure E_a, which should be constant for a given process. The higher the value of E_a, the longer the decay time will be. This is because E_a roughly represents an energy "barrier" that must be overcome for an electron to leak away. The higher the barrier, the fewer electrons have the energy to overcome E_a.

Charge leakage can be aggravated by poor quality tunnel oxide. Defects in the oxide provide a lower energy path for discharging, effectively lowering E_a. Baking a device accelerates this leakage, and identifies devices with weak oxide. AMD uses a bake for all EE products to ensure that the production devices have a high E_a and therefore good data retention. The average E_a for all devices, including those with weak oxide, is about 0.8 eV. After eliminating the weak devices by a 250°C 24-hr bake, the average E_a is about 1.8 eV.

Data retention time depends on the temperature to which the devices are exposed. The higher the temperature, the shorter the decay time because the electrons have more energy, and more can leak off the gate.

There are two temperatures that may be of concern for different reasons: the maximum device storage temperature (150°C) and the maximum operating temperature (125°C for military). In the first case, the idea is to know that if a programmed part sits on a shelf for some period of time before being used, that the program will remain intact for that time. The second case is intended to give an idea of how long a device will remain operational in-system.

Using the equation above to solve for the decay time at these temperatures, the result is several decades for the storage temperature, and even longer for the operating temperature. For room temperature, the exponential nature of the function makes the decay time increase to centuries.

AMD specifies 10 years at the maximum storage temperature (an industry standard for EPROMs and EEPROMs), and 20 years in-system under worst-case military conditions. That the calculated numbers are so much higher builds confidence in the numbers specified. In general, the typical end-of-life failure mechanisms that affect all devices (and which are unrelated to the EE cells) will cause device wear-out before the program data is lost.

The integrity of the charge in the electrically erasable cell also stands up to any electrical fields that exist in surrounding equipment. For charge to be transferred off, or onto, the floating gate, a field must be placed across the oxide. Such a field cannot be generated outside the programming mode; an external field, no matter how strong, cannot set up the programming mode.

The charge might also be pulled through some other oxide if the field were large enough. However, to remove the charge through anything but the tunnel oxide requires an external field so high that the rest of the device would break down before any cell charge were ever lost. This would occur on any device, programmable or not. Therefore any external field strong enough to remove charge from a floating cell will destroy the rest of the device first.

Cell Endurance

Another factor that affects data retention in the long term is the cell endurance. The endurance is the number of times the device can been erased and reprogrammed. Over time, the oxide can wear out, resulting in a gradual reduction in E_a. This occurs as defects are created in the oxide. These defects trap electrons; these electrons then oppose the field that is required for programming. Given enough trapped charges, the established potentials will be insufficient for programming. This typically happens after hundreds of thousands of reprogramming cycles.

The ability to charge up a cell with good data retention can be measured by the *margin voltage*. This is the voltage that must be applied to the control gate to counteract the charge on the floating gate. If the gate is highly charged, a larger margin voltage is needed to overcome the charge. Thus, put simplistically, a higher margin voltage indicates better cell charging.

Figure 15 illustrates measurements of the margin voltage as the number of program/erase cycles is increased. By 100,000 cycles, the margin voltage still is greater than 4 V; for the cell to fail, the margin voltage must fall to below about 1 V.

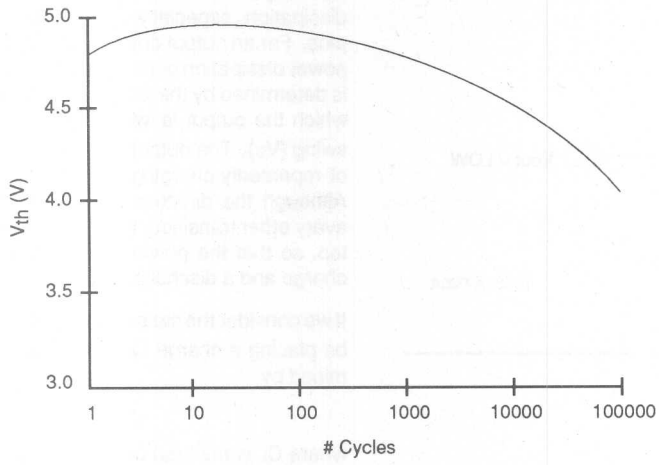


Figure 15. Cell Endurance: Margin Voltage Solid After 100,000 Program/Erase Cycles

For EEPROMs, which often are reprogrammed in-system, it is important to know how many thousands of times the device can be reprogrammed. However, most EE PLDs are not intended to be programmed in-system, and probably are programmed very few times. Most production units are programmed only once by the user. Prototypes might be programmed tens of times at most. Therefore we specify a maximum number of 100 erase/reprogram cycles.

This does not imply that the devices are weaker than EEPROMs; it is just that more extensive testing would have to be done to justify specifying a larger number. Since this larger number is not needed, a cost savings is realized because of the test simplification. Note that the devices are actually programmed hundreds of times in testing before they are shipped out, giving outstanding programming and functional yields; however, the number of erase/reprogram cycles specified refers only to programming done by the user.

DEVICE CHARACTERISTICS

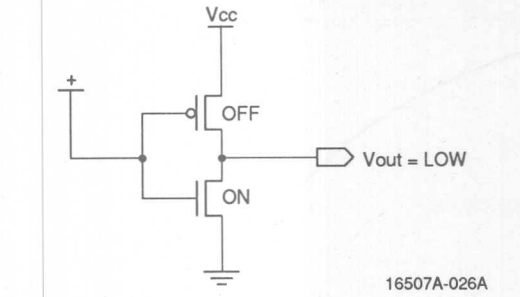
Power Dissipation

CMOS technology is associated with low power, and indeed, all CMOS PLDs provide lower power than their bipolar counterparts. However, most PLDs do not provide the zero-standby power that standard CMOS logic parts provide.

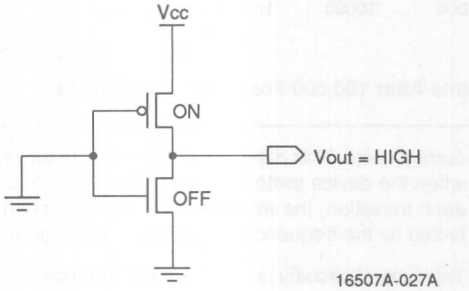
The basic CMOS inverter lowers operating power because at any given time, only one of the two transistors can be fully ON. The other is OFF and blocks the flow of DC current. Thus, when the device is in a stable state, no current can flow. While the device is switching, both transistors are partially ON, allowing for a transient current spike. This means that power is consumed only when the device switches. Because a spike occurs for each transition, the average power consumption is affected by the frequency of operation (see Figure 16).

This type of circuitry is found throughout most of a PLD circuit. However, one portion of the PLD circuit does not use a standard CMOS inverter: the programmable array. One of the necessary elements of zero-power operation is that the output of the inverter have a voltage swing from ground to V_{CC}, so-called *rail-to-rail* operation. In the array, such a wide swing makes the propagation delays too long. To speed up the device, the sense amps that determine the state of a product term are designed to have a much more limited swing. This means the sense amps are constantly drawing power, even when not switching. These are the half- and quarter-power CMOS PLDs; their power consumption is still less than that of a bipolar PLD. Since most CMOS PLDs are used in TTL sockets, the CMOS PLDs work well.

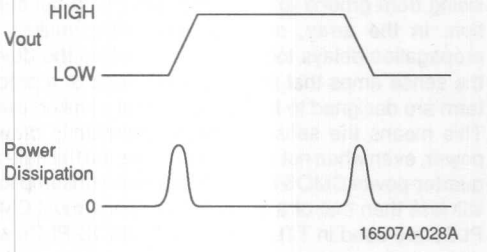
For designs that require the absolute lowest-power operation, the half- and quarter-power CMOS PLDs are inadequate. *Zero-power* PLDs have been designed to address this range of applications. These devices operate by turning off the sense amps in the array if no signals switch for a period of time. If the transition detectors at the inputs indicate that some signal is changing, then the array is activated to process the incoming data. In this manner, the average operating power consumption can be reduced, especially at low frequencies, and the standby power consumption is negligible (less than 15 µA). The only penalty is a small wake-up delay of a few nanoseconds.



a.



b.



c.

Figure 16. CMOS Inverter Power Dissipation: a. V_{OUT} = Static LOW; b. V_{OUT} = Static HIGH; c. Dynamic Power Dissipation

I_{CC} vs V_I and Loading

The greatest external contributors to I_{CC} are the input HIGH level (V_{IH}) and the output load.

As the V_{IH} drops from its ideal level of V_{CC}, the inverter starts to draw current. The worst case scenario would be a V_{IH} at the minimum of 2.0 V, which could contribute some 5 mA per input buffer to the power consumption.

The output load can have a dramatic effect on power dissipation, especially on devices that have many I/O pins. For an output driving a purely capacitive load, the power dissipation contributed by the load for one output is determined by the load capacitance, the frequency at which the output is switching, and the output voltage swing (V_S). The output stage will go through a process of repeatedly charging and discharging the capacitor. Although the direction of charge flow reverses itself every other transition, the relative voltage change does too, so that the power contribution is the same for a charge and a discharge.

If we consider the case of charging the capacitor, we will be placing a charge Q_L on the capacitor that is determined by

$$Q_L = C_L V_O$$

where C_L is the load capacitance and V_O is the output voltage. The current contribution from this is

$$i = \frac{dQ_L}{dt}$$
$$= C_L \frac{dV_O}{dt}$$

In one half the output transition period t_P, the change in output voltage will be equal to the output swing V_S. This means that

$$i = C_L \frac{V_S}{\frac{t_P}{2}}$$
$$= 2C_L \frac{V_S}{t_P}$$
$$= 2C_L V_S f_O$$

where f_O is the frequency at which the output is switching.

The power dissipation is the product of the current and the voltage. Since the voltage is changing during the time that the power is being dissipated, we can approximate by dividing the voltage swing by 2. This gives

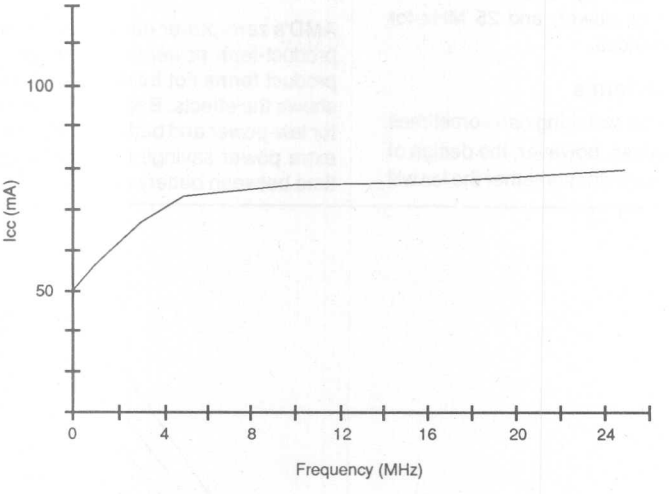
$$P = iv$$
$$= 2C_L V_S f_O \frac{V_S}{2}$$
$$= 2C_L V_S^2 f_O$$

This means that for a 100-output device (PLD or any other device) with each output driving 35 pF loads, where the output swing is 3 V and the output frequency is 50 MHz, the power dissipation contributed only by the load will be about 1.6 W regardless of the power dissipation of the chip itself.

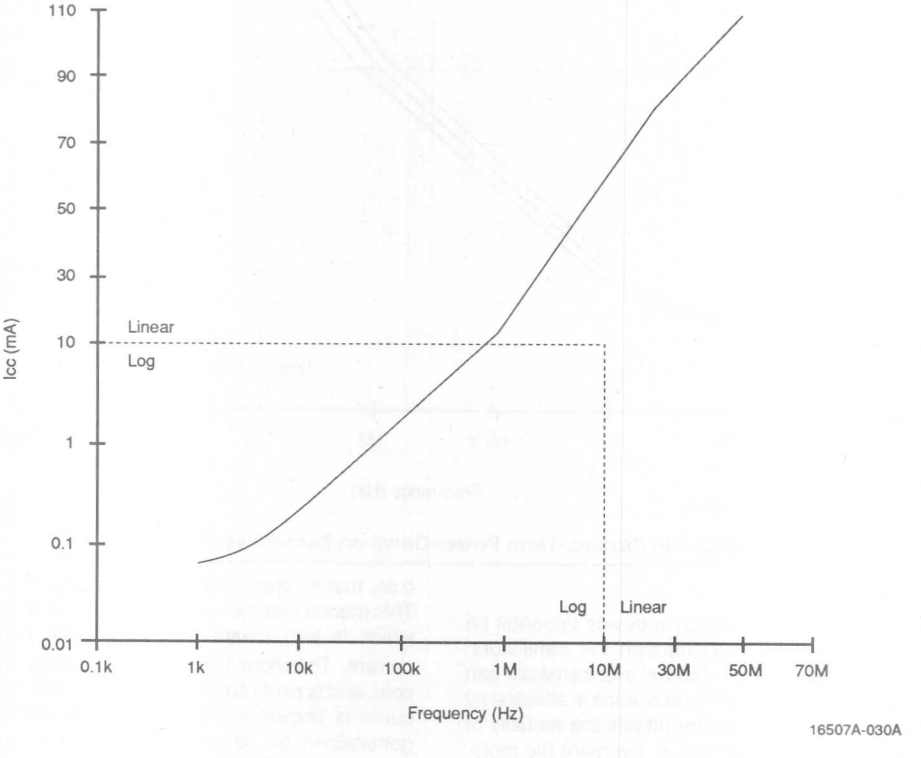
I_{CC} vs Frequency

The operating current increases with frequency for both standard and zero-power CMOS devices. The

difference is the current at low frequencies. A standard device typically can draw 35 mA at 0 MHz; a zero-power device typically draws less than 10 µA. Figure 17 shows typical curves for standard and zero-power devices.



a.



b.

Figure 17. Icc vs frequency: a. Half-Power Device; b. Zero-Power Device

with existing specifications, the 16V8 and 20V8 have their I_{CC} specified at a frequency level: 15 MHz for devices with t_{PD} of 15 ns or slower, and 25 MHz for 10 ns, 7.5 ns, and faster devices.

I_{CC} vs Number of Product-Terms

The number of product terms switching can sometimes affect I_{CC}. On standard devices, however, the design of the particular sense amp determines whether the I_{CC} will

standpoint, the change in I_{CC} due to different numbers of product terms is negligible.

AMD's zero-power devices have been designed with a product-term power-down feature that turns off those product terms not being used. The graph in Figure 18 shows the effects. Because these devices are intended for low-power and battery-operated use, the substantial extra power savings can significantly help extend the time between battery charges.

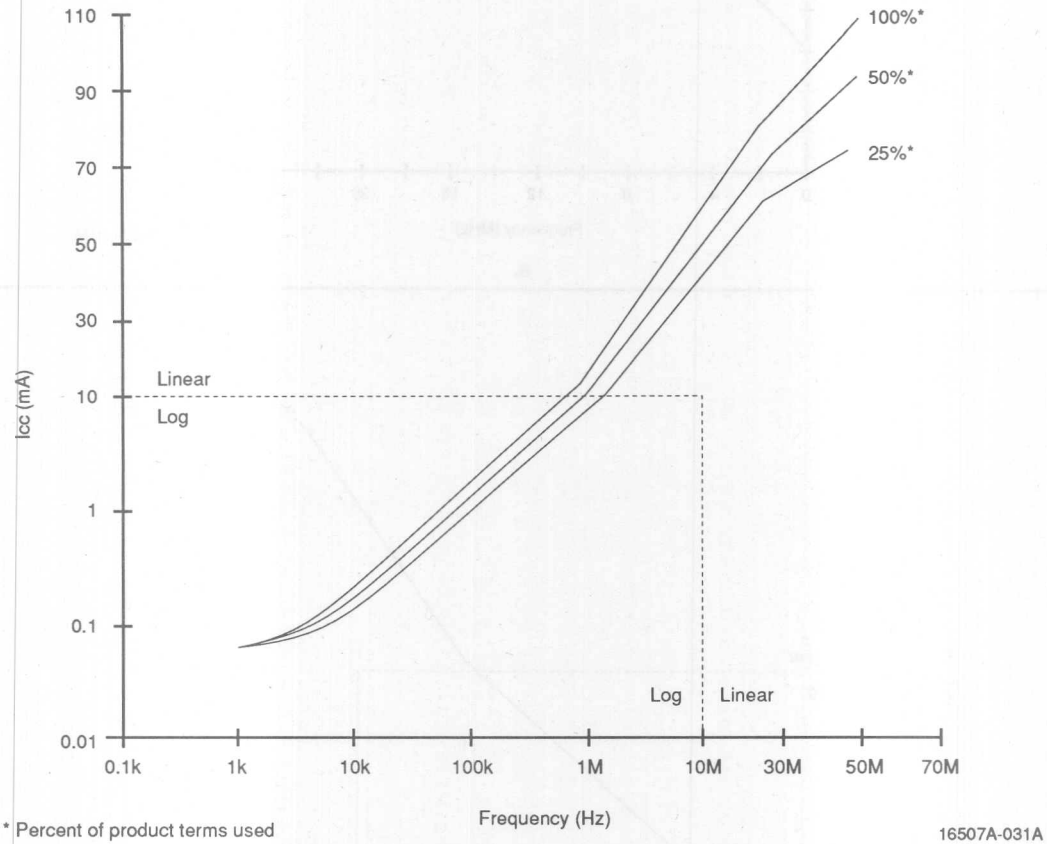
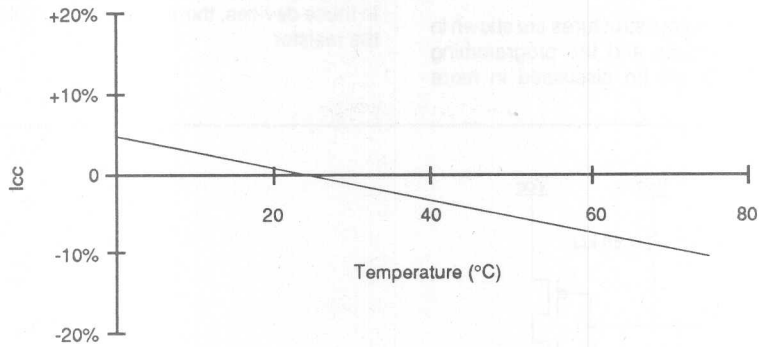


Figure 18. Product-Term Power-Down on Zero-Power Devices

I_{CC} vs Temperature

The amount of current drawn by a device depends on how much current can pass through the transistors. Simplistically speaking, the channel of a transistor can be modelled as a resistor. The resistance is affected by temperature, since temperature affects the mobility of electrons. The hotter the device is, the more the molecules are vibrating around, and the harder it is for electrons to pass through without a collision with a molecule; that is, electrons are less mobile in a hot device. This means that the resistance of the channel is higher, which in turn means that the device conducts less current. Therefore I_{CC} is greatest when the device is cold, and is minimized when the device is hot. A typical curve is shown in Figure 19. This curve has been generalized by normalizing the current to the room temperature current.



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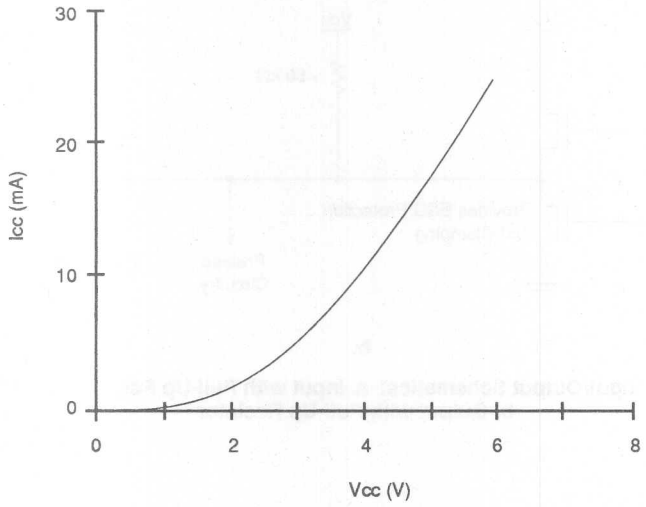
Figure 19. Icc vs Temperature, Normalized to Room Temperature

Icc vs Vcc

The variation of Icc with changes in Vcc should come as no surprise; as Vcc increases, so does Icc. This means that the power consumption actually increases roughly as the square of Vcc, since power consumption can be expressed as

$$P = V_{CC} I_{CC} = \frac{V_{CC}^2}{R_{eff}}$$

where R_{eff} is defined as $\frac{V_{CC}}{I_{CC}}$. This is a simplification, of course, since R_{eff} is non-linear, and varies with Vcc. A typical Icc vs Vcc curve is shown in Figure 20.



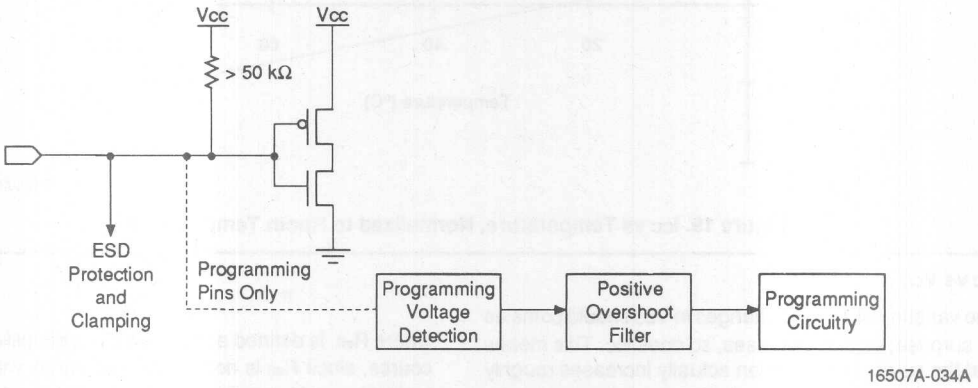
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Figure 20. Icc vs Vcc

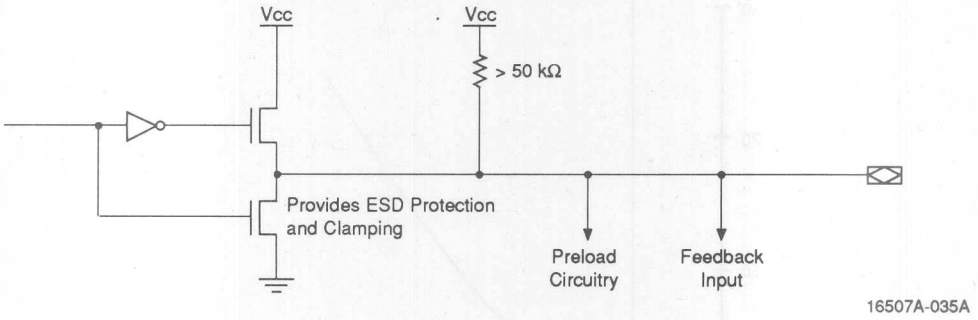
Input/Output Structures

The basic input and input/output structures are shown in Figure 21. The ESD circuits and the programming voltage detection circuits will be discussed in more detail later.

Newer devices have pull-up resistors as shown below. In these devices, there is also a transistor in series with the resistor.



a.



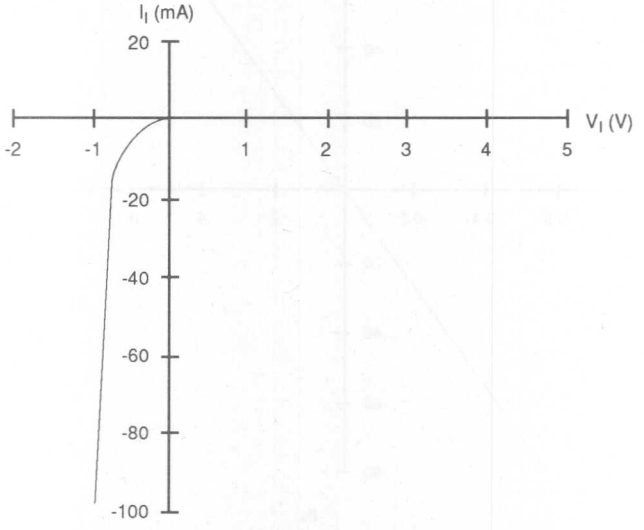
b.

Figure 21. Equivalent Input/Output Schematics: a. Input with Pull-Up Resistor and Overshoot Filter; b. Output with Pull-Up Resistor

I-V curves

Figure 22 shows a typical I-V curve for an input buffer. Within the range of normal input signals, the input buffer has extremely high impedance, with diodes and MOS transistors that turn on when the input is below ground. On higher speed devices, this has the effect of a high-speed diode capable of clamping negative overshoot on noisy signals.

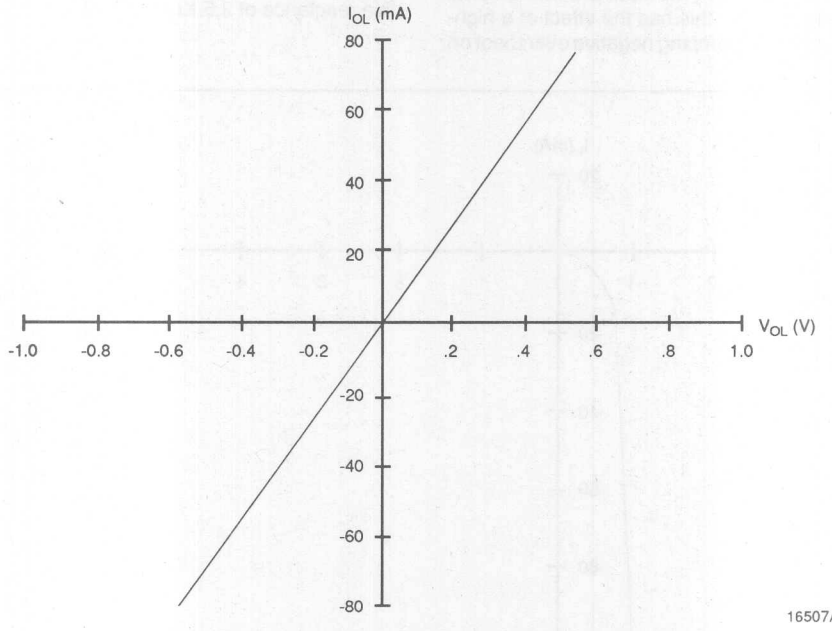
Since the input is effectively a capacitor, the impedance has no real component; the imaginary portion falls with increasing frequency. A typical device has an input capacitance of 8 pF at 1 MHz. Assuming a capacitance around 8 pF at higher frequencies, this yields a capacitive reactance of 2.5 KΩ at 50 MHz.



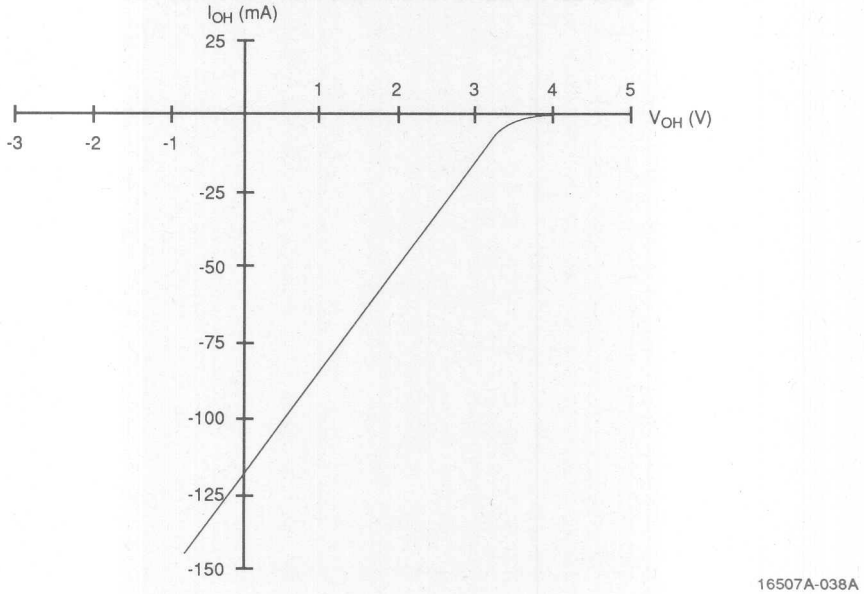
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Figure 22. I-V Curve for an Input with No Pull-Up Resistor

Figure 23 shows typical I-V curves for high and low TTL-style outputs. The impedance of a low output is about 10 Ω; a high output has an impedance of about 30 Ω. The fact that the impedances are somewhat more symmetric than those found on a bipolar device makes it a bit easier to terminate long traces accurately.



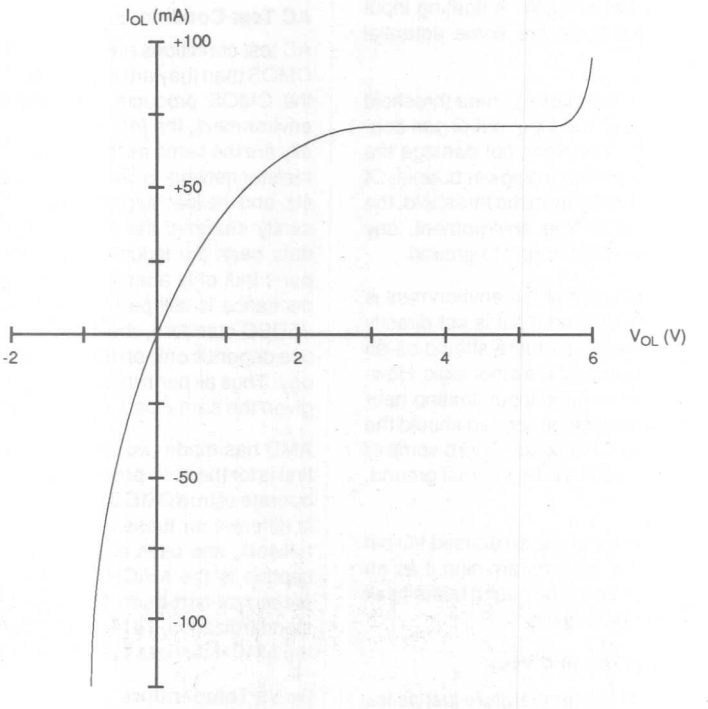
a.



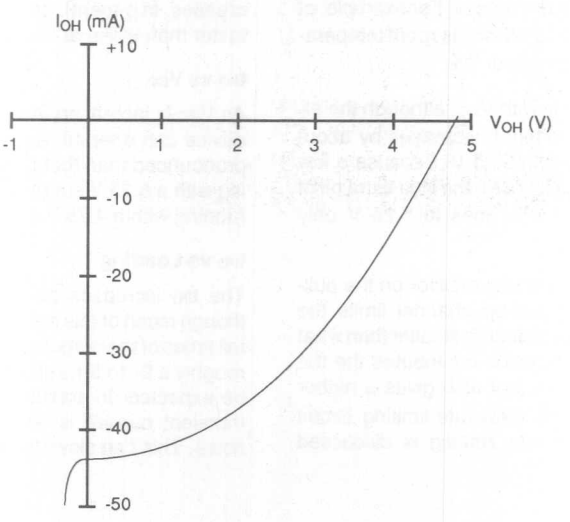
b.

Figure 23. I-V Curves for a TTL-Style Output with No Pull-Up Resistor: a. Output LOW; b. Output HIGH

Figure 24 shows the curves for rail-to-rail switching outputs. The p-channel impedance, when the output is HIGH ranges from 200 Ω when extremely heavily loaded to about 50 Ω when lightly loaded. The n-channel impedance is lower, at about 10 Ω.



a.



b.

Figure 24. I-V Curves for a CMOS-Style Output: a. Output LOW; b. Output HIGH

Open Inputs

Newer devices have input pull-up resistors with a minimum resistance of 50 kΩ. When unused, these inputs can be left unconnected. With older devices, an unused input should be pulled HIGH or LOW. A floating input may cause no trouble, but there are some potential concerns.

First, if an input is floating with its voltage near threshold (1.5 V for a TTL-style device), the input buffer can conduct tens of mA of current. This does not damage the device, but must be calculated into the power budget. Of course, as the input moves away from the threshold, the current decreases. In a noise-free environment, any floating inputs will generally tend to drift to ground.

The second concern is the fact that the environment is not usually noise-free. The unused input is not directly connected to any internal logic, so there should be no interference between the input and the other logic. However, if there is noise on an unused input floating near threshold, internal noise could be generated should the input buffer start to oscillate. This could disturb some of the surrounding circuitry as well as the internal ground, compounding the problem.

On a device without pull-up resistors, an unused I/O pin can be pulled HIGH or LOW by programming it as an output with constant value 1 or 0. The output buffer itself then acts as the pull-up or pull-down.

Output Drive vs Temperature and V_{CC}

The output drive varies with the temperature just as I_{CC} does. As the temperature increases, electron mobility decreases, cutting the drive. Likewise, the drive increases as the temperature decreases. For example, at 75° I_{OL} decreases by about 18% from its room temperature value; I_{OH} decreases by about 7%.

The drive also varies directly with V_{CC}, although the effect is most pronounced on I_{OH}; it increases by about 18% when taken from 5.0 V to 5.25 V. Because a low output transistor is already ON hard, the little extra bit of drive that its gate gets as V_{CC} goes to 5.25 V only increases I_{OL} by about 3%.

There is no explicit current-limiting resistor on the pull-up. The resistance of the pull-up channel limits the current. The fact that this resistance is smaller than what one might find in a bipolar device contributes the the more symmetric impedances, but also gives a higher short-circuit current I_{SC}. The slew-rate-limiting circuit also limits the drive; slew rate limiting is discussed below.

AC Parameters

AC parameters vary with a number of conditions. The data sheet specs pick one set of conditions that act as a benchmark for confirming the guaranteed performance, but as the application changes the conditions, the actual system performance may change for the better or worse.

AC Test Conditions

AC test conditions are sometimes treated differently for CMOS than they are for bipolar. However, since most of the CMOS products are designed to work in a TTL environment, the test conditions that AMD uses generally are the same as those used for bipolar devices. The resistor network is chosen to match the output drive levels, and the load capacitor is normally 50 pF. JEDEC recently changed the load standards from what had to date been the industry de facto standard, but for TTL parts this only affects the resistor values; a 50 pF capacitance is still part of the standard. Note that in the JEDEC standard, the decision affecting which load to use depends only on the interface level, not the technology. Thus all parts intended to operate at TTL levels are given the same load, whether bipolar or CMOS.

AMD has made two exceptions to the 50-pF load. The first is for the zero-power devices, which are designed to operate at true CMOS levels. The JEDEC load standard is different for these devices; it has a different resistor network, and uses a 30-pF capacitor. The second exception is the MACH family: in this density range, a precedent had been set at 35 pF, prior to the JEDEC standardization. To be compatible with existing devices, the MACH devices are measured with 35 pF loads.

t_{PD} vs Temperature

Propagation delays decrease (that is, they speed up) at colder temperatures for the same reasons that I_{CC} increases. In general, devices at 0°C operate about 15% faster than those at 75°C.

t_{PD} vs V_{CC}

As V_{CC} is increased, more power is available, and the device can operate faster. However, the effect is less pronounced than that of temperature. A device operating with a 5.25 V supply runs about 4% faster than one running with a 4.75 V supply.

t_{PD} vs Loading

The t_{PD} increases as the device load increases, although much of this results from the increase in rise and fall times of the outputs. For every 50 pF change in load, roughly a 2- to 5-ns change in the rise and fall time can be expected. In addition, as the load increases, more transient current is switched, creating more internal noise. This can slow the speed path inside the chip.

Power-Up Reset

Power-up reset is a feature that forces a device to power up into a known state. Without this feature, the power-up state is not known. Power-up reset helps make system initialization and testing simpler.

The ramp rate of V_{CC} is not critical to the power-up reset function. However, there are two other requirements: the supply ramp must be monotonic, and the clock must be suppressed until power-up is complete.

The monotonicity requirement basically says that there should be no low-going glitches in the power-up ramp (Figure 25). The danger in such glitches is that if the timing and voltage are just right, the registers themselves may think that the device powered down temporarily, causing them to lose their state. If the glitch is fast enough, however, the power-up reset circuit may not notice the glitch, and may think that everything is proceeding just fine. At the end, the registers may be in a random state. Even if the power glitches low enough for long enough to shut down all circuits, the power-up timing must be restarted from the end of the glitch.

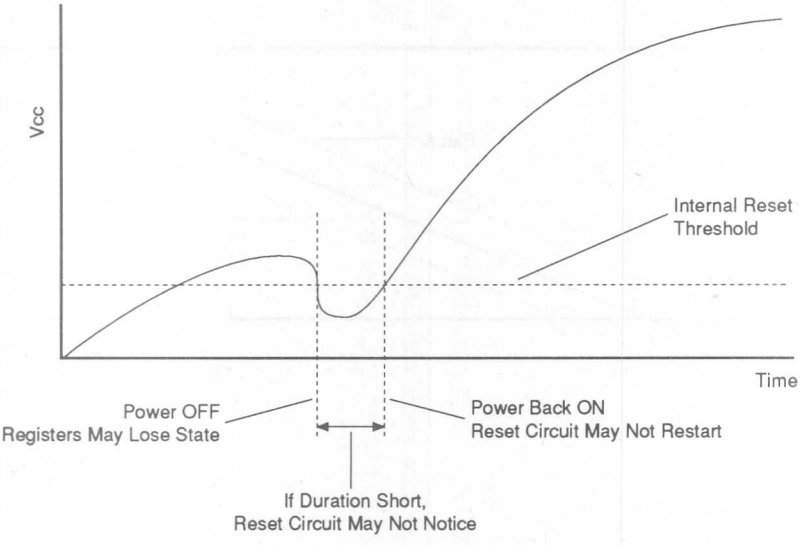
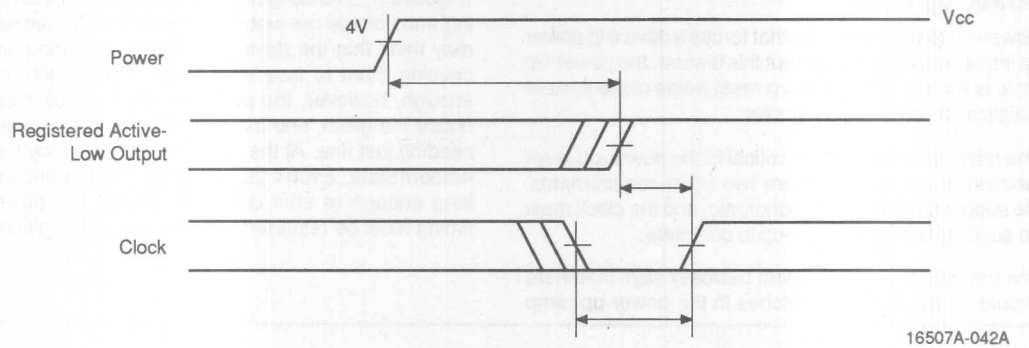


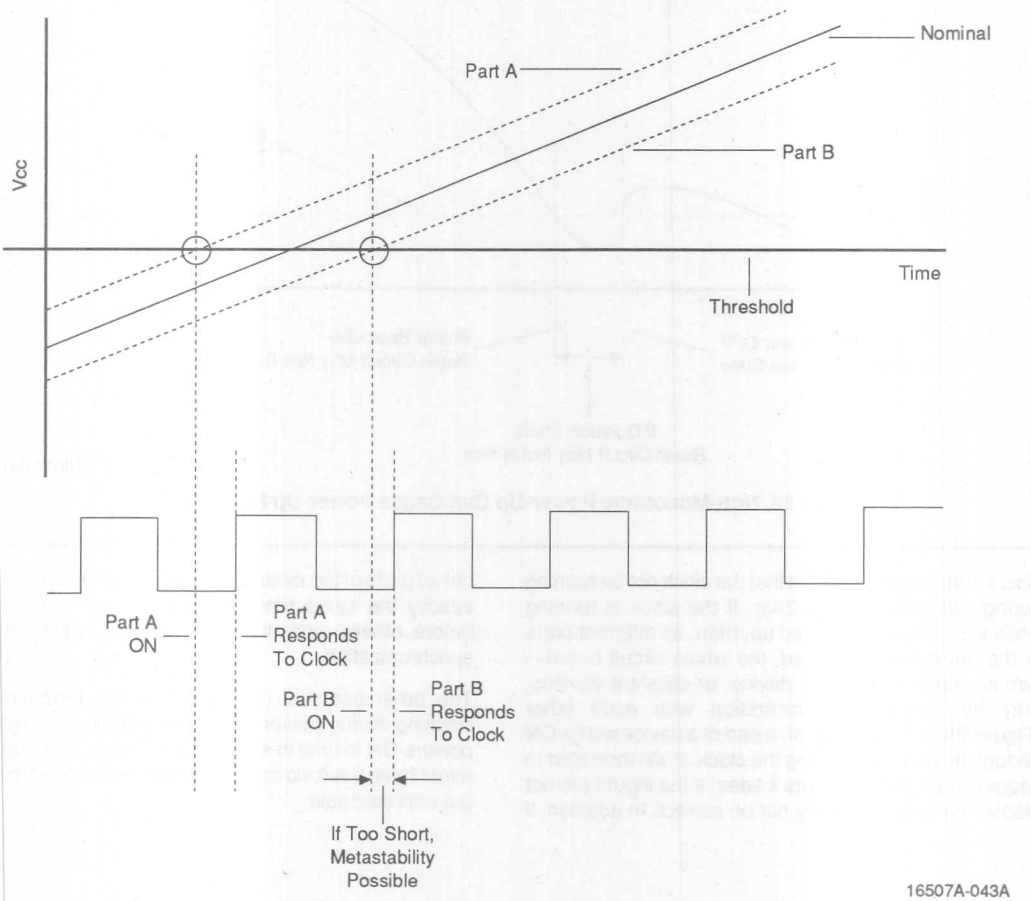
Figure 25. Non-Monotonic Power-Up Can Cause Power-Up Reset To Fail

There is also a requirement that the clock not be running during power-up (Figure 26a). If the clock is running while the device is powered up, then, as different parts of the device—and, indeed, the whole circuit board—turn on, parts of a single device, or different devices, may be out of synchronization with each other (Figure 26b). At some point, a part of a device will be ON enough to start recognizing the clock. It will then start to sequence as per the inputs it sees. If the inputs are not stable, the sequence may not be correct. In addition, if not all parts of the circuit or board recognize the clock at exactly the same time, some parts will start cycling before others, and the whole system will be out of synchronization.

The other potential (although remote) problem with clocking during power-up is metastability. If a register powers ON in time to see the clock edge, its setup time might have been violated, making the results at the output unpredictable.



a.



b.

Figure 26. Clocking During Power-Up Reset: a. Correct Operation; b. Free-Running Clock Places Part B One Clock Cycle Out of Sync with Part A

Powered-Down Characteristics

Some applications place the CMOS PAL device in a situation where it is itself powered down, but it is driving or is driven by other devices that are still powered up. This is especially typical of devices that are talking directly to a bus (Figure 27).

The characteristics of the device in such a condition depend on how the power was removed. There are two ways of removing power:

- opening up the V_{CC} line (e.g., if V_{CC} is fused, and the fuse blows; Figure 28)
- grounding V_{CC} (Figure 29)

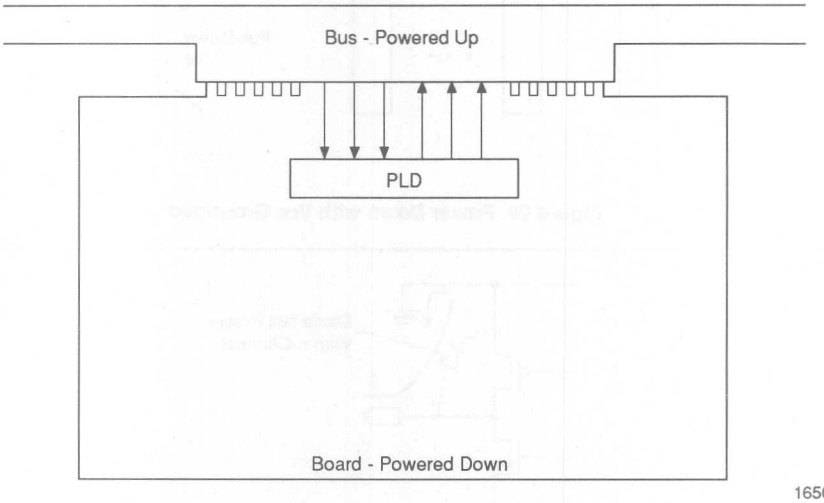


Figure 27. Powered-Down Device with Active Inputs and Outputs

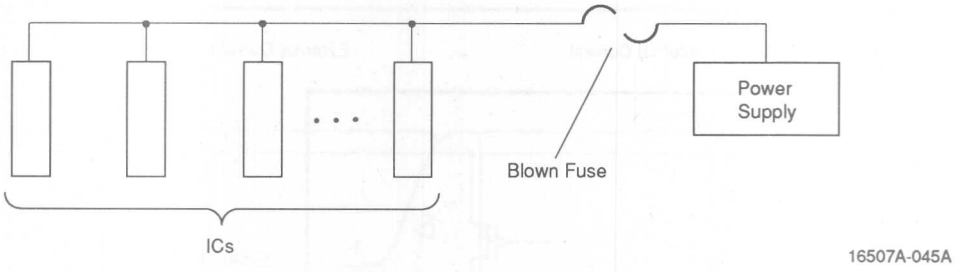


Figure 28. Power Down with V_{CC} Open

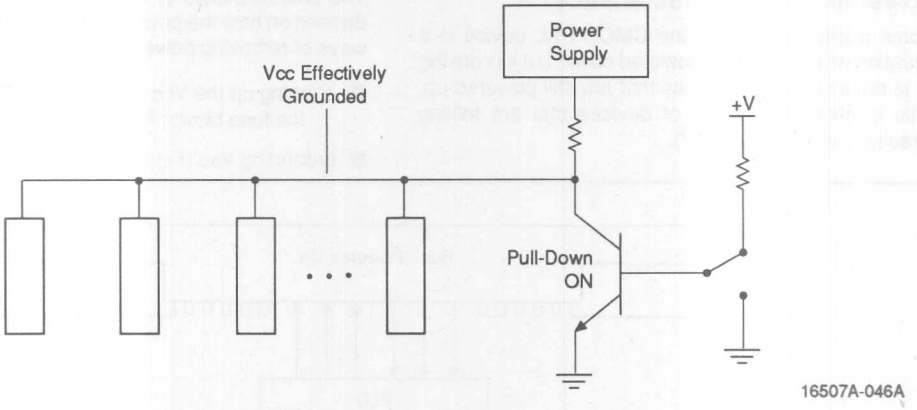
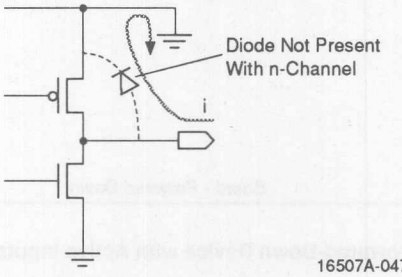
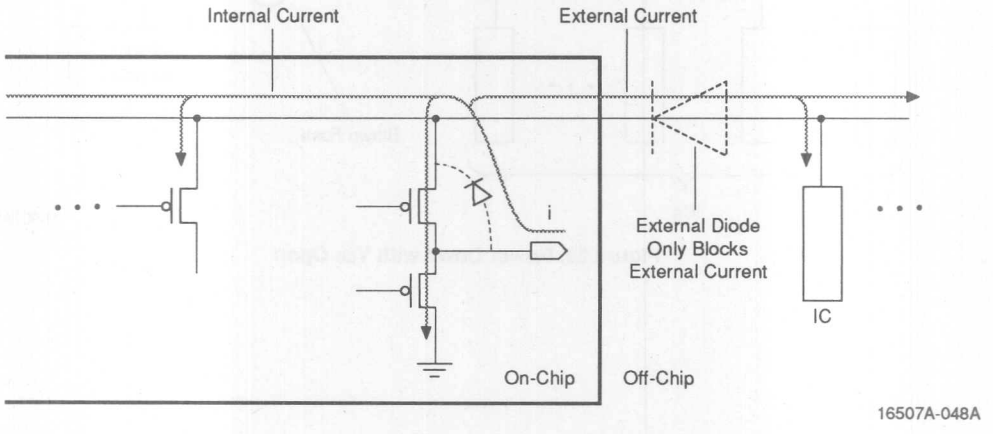


Figure 29. Power Down with V_{CC} Grounded



a.

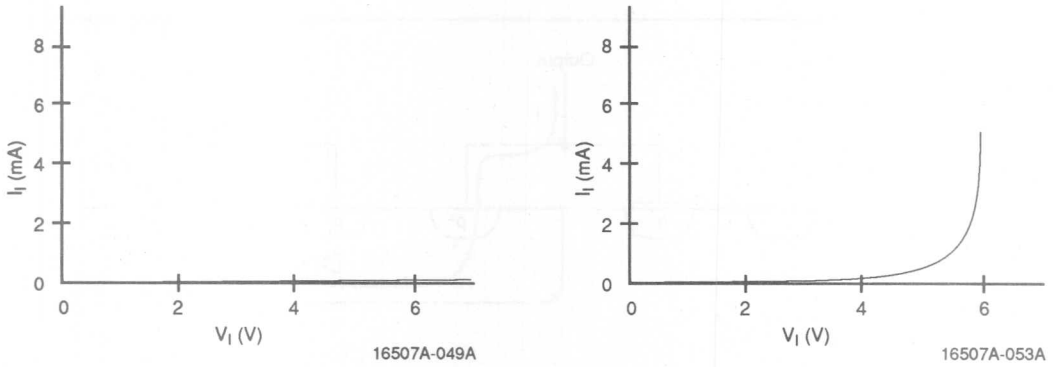


b.

Figure 30. Powered-Down Current Paths with P-Channel Pull-Up: a. V_{CC} Grounded; b. V_{CC} Open

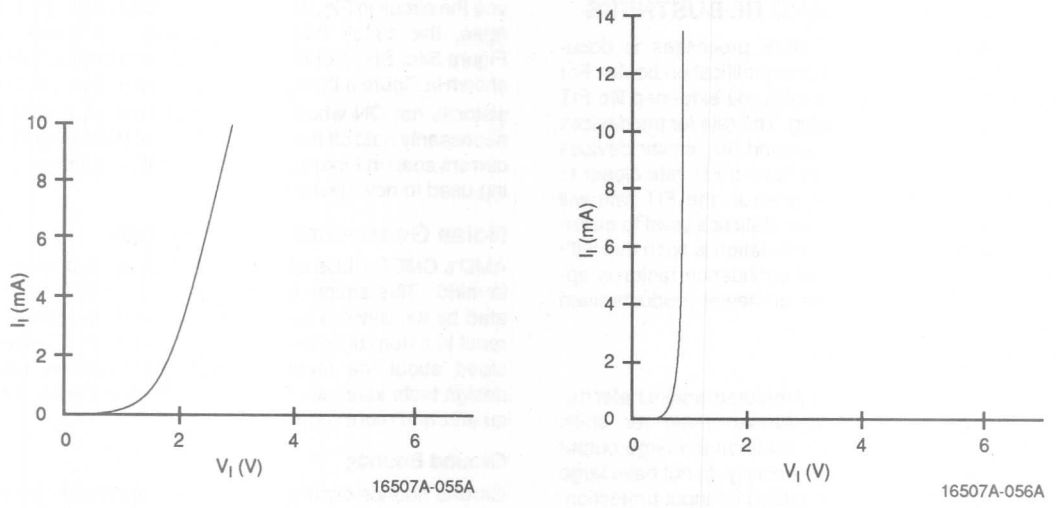
It is important to know whether, for a given device, there is some kind of path from the pin to Vcc when Vcc is lower than the pin voltage. If any current can flow, it is not necessarily catastrophic, but there can be some effect. If Vcc is grounded, then there is a direct path to ground for any current flowing from the pin to Vcc (Figure 30a). If Vcc is open, then the only path from Vcc to ground is through the device itself, and through the Vcc lines of any other devices on the same Vcc line (Figure 30b). In the latter case, the pin is essentially powering up the device(s) itself; realistically, it cannot provide enough power to drive the chip, and this could result in the pin being loaded down.

Most of AMD's CMOS PLDs have no such path when powered down. Figures 31 and 32 show the I-V curves of inputs and I/O pins while Vcc is open and Vcc is grounded. Figure 31 is for TTL-compatible devices, which have n-channel pull-ups on the outputs. Figure 32 is for the HC/HCT-compatible zero-power devices and the PALCE610H-15, which have p-channel pull-ups.



a. b.

Figure 31. Power-Down Characteristics of TTL-style CMOS Inputs and Outputs: a. Standard; b. Older ESD Structure



a. b.

Figure 32. Power-Down Characteristics of CMOS-Style Output: a. Vcc Open; b. Vcc Grounded

Note that for most of the TTL-compatible devices, there is no leakage on the pins. This means that signals on a pin are not affected by the powered-down device. Therefore it can be safely connected to an active bus. It also allows for safe *hot insertion*, where the device (or the board that contains the device) is plugged into a socket that has V_{CC} applied.

As a result of one of the ESD structures (which are discussed below), some devices do conduct some current when V_{CC} is powered down (Figure 31b). Newer devices do not have this characteristic.

With the HC/HCT-compatible devices, the input structures are the same as for TTL devices, but the outputs conduct because of the p-channel pull-up. There is a parasitic diode between the output and V_{CC} (Figure 33). This can cause latch-up if the output voltage is higher than V_{CC}. Thus it is not recommended that devices with p-channel outputs be directly connected to a bus if the device will be powered down while the bus is active. Hot-insertion of these devices should also be avoided.

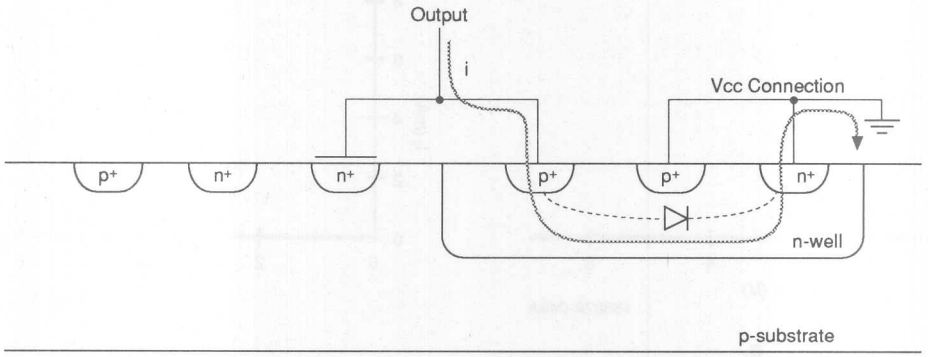


Figure 33. Parasitic Diode in CMOS-Style Outputs

DEVICE INTEGRITY AND ROBUSTNESS

The reliability of AMD's CMOS processes is documented in product and process qualification books. For EE4 process products generally, the extended life FIT rate is under 100 and declining. The rate for the devices with 2000 hours burn-in is around 30; similar devices with only 1000 hours burn-in have a FIT rate closer to 100. With more burn-in experience, the FIT rate will decline even further due to the statistics used to calculate FIT rates. The FIT rate calculation is such that with fewer burn-in hours, a lower confidence factor is applied, giving higher FIT rates on newer products even when there are no failures.

ESD

Every pin on the devices is protected against electrostatic discharge (ESD), a formal name for static electricity shocks. Output pins rely on the large output drivers as protection. Inputs normally do not have large drivers, so a circuit must be added for input protection. These input protection circuits also provide clamping against negative overshoot.

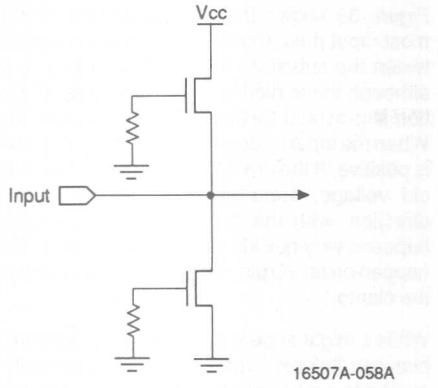
All new devices make use of the structures in Figures 34a and 34c for ESD protection. Most input pins use the circuit in Figure 34a. On pins requiring high voltages, the circuit has been modified as shown in Figure 34c. Some older devices have the configuration shown in Figure 34b. Because the active pull-down transistor is not ON when V_{CC} is disconnected, it cannot necessarily hold off the ESD transistors; this causes the current seen in Figure 31b. This circuit is no longer being used in new devices.

Noise Generation and Sensitivity

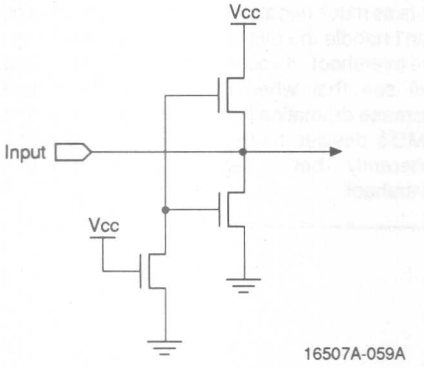
AMD's CMOS PLDs are designed with noise concerns in mind. This affects both the amount of noise generated by the devices and the way in which the devices react to externally-generated noise. As more is understood about the nature of system-level noise, new design techniques are being used to make the devices quieter and more robust.

Ground Bounce

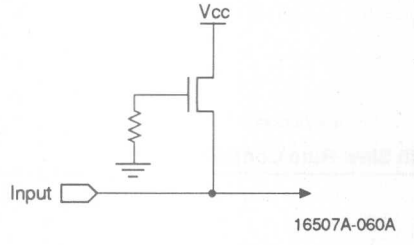
Ground bounce occurs when many outputs simultaneously switch from HIGH to LOW. This occurs because of the fact that CMOS devices generally have outputs that switch very quickly. If left uncontrolled, ground bounce can make a device with many outputs unusable.



a.



b.



c.

Figure 34. ESD Protection: a. Standard; b. Older Version; c. Supervoltage Pins

Ground bounce is generated by the natural parasitic inductance in the ground lead (see Figure 35). When a large current surge goes through the inductor, the high $\frac{di}{dt}$ induces a voltage that puts the ground level on the chip at a higher voltage than the ground level seen on the board.

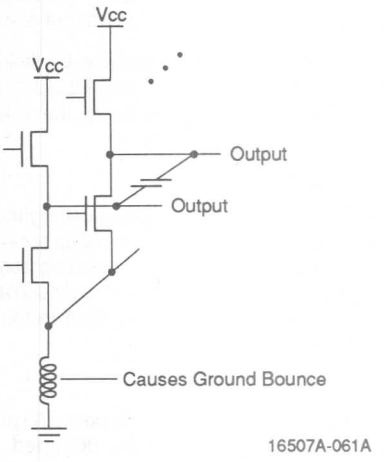


Figure 35. Origins of Ground Bounce

Any output that is at a static LOW level maintains a V_{OL} with respect to the chip ground. If the chip ground is bouncing with respect to the board ground, the LOW output will track the moving chip ground and will also appear to bounce (see Figure 36). This is sometimes seen as a glitch by the next device. Even if there is no output glitch, instances of high ground bounce can slow the performance of the internal circuits by temporarily starving them of power. In extreme cases, this can interrupt the internal circuits.

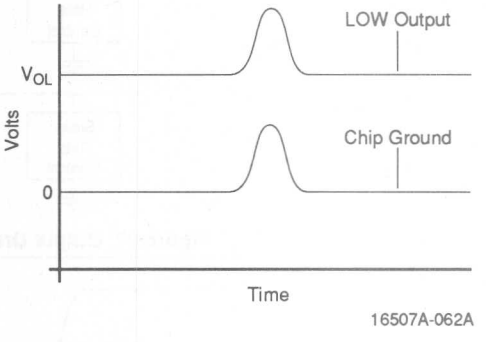


Figure 36. Symptoms of Ground Bounce

Excess ground bounce can be handled in two ways: by limiting the amount of ground inductance and by reducing the $\frac{di}{dt}$. Inductance can be reduced by improving the configuration of the ground pin. On AMD's 28-pin devices with many outputs (PALCE24V10 and PALCE26V12), the ground pin has been moved from

the corner to the center of the DIP package, effectively reducing the inductance by a factor of about four.

Ground bounce is also controlled by limiting the slew rate of all the output drivers (see Figure 37). This slows down the fall time and reduces the rate of current change by as much as 25%.

Overshoot Sensitivity

Overshoot is a form of noise usually generated when signal traces act as transmission lines but have not been adequately terminated. The resulting reflections can cause significant overshoot, with as much as double the intended swing applied to the input in the negative or positive direction.

Negative Overshoot

Negative overshoot (Figure 38) poses no problems for a device that has been carefully designed. There is no detrimental effect as long as no unexpected parasitic behavior occurs due to the fact that ground is no longer the most negative voltage. However, the ringing that usually follows overshoot can slow down system performance, since the system has to wait for the ringing to subside.

Clamp diodes are useful for stealing the energy present in the ringing, and cutting the ringing short. A fast clamp reacts to the overshoot as it occurs, cuts the amplitude of the overshoot, and reduces or eliminates ringing. Figure 39 shows the ESD protection circuit used on most input pins. Parasitic p-n junction diodes exist between the substrate and the n-type source and drain, although these diodes are relatively slow. Faster reaction is provided by the n-channel devices themselves. When the input is too negative, the gate-to-drain voltage is positive. If the drain is more negative than the threshold voltage, the transistors turn on in the reverse direction, with the drains acting as a sources. This happens very quickly and acts as a clamp. This will also happen on an I/O pin, with the low output driver acting as the clamp.

While it might appear that parts with negative substrate bias can "tolerate" more negative overshoot, it is really more accurate to say that these parts *allow* more negative overshoot, since there is no clamping. If there are effective input clamps, which are possible with a grounded substrate, then it will look like the part never gets as much negative overshoot. This does not mean it can't handle the overshoot; it means that it is clamping the overshoot. If you take the part out of the socket, you will see that when unclamped, the overshoot will increase dramatically, as illustrated in Figure 40. Since AMD's devices have a grounded substrate, they are inherently better equipped to handle negative overshoot.

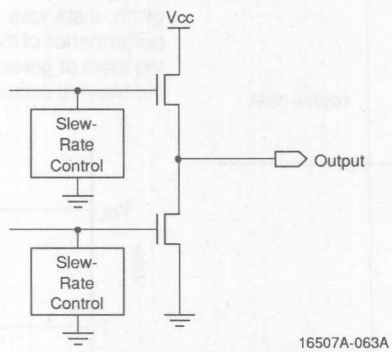


Figure 37. Output Drivers with Slew-Rate Control

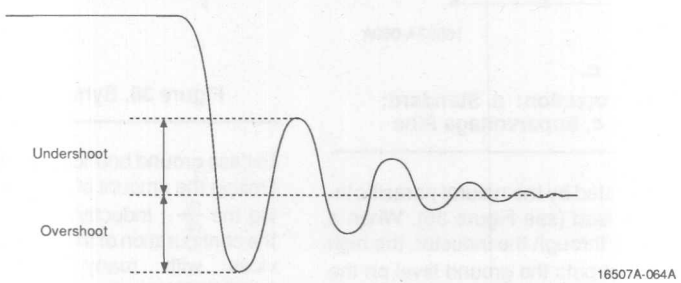
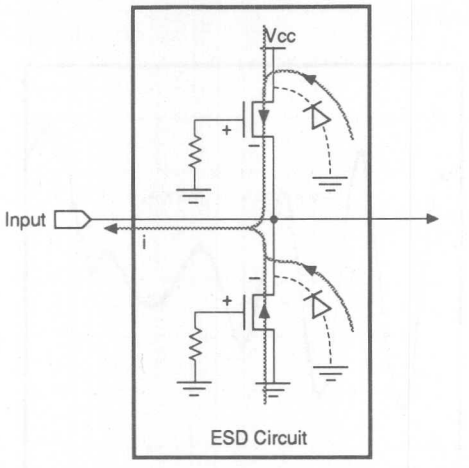
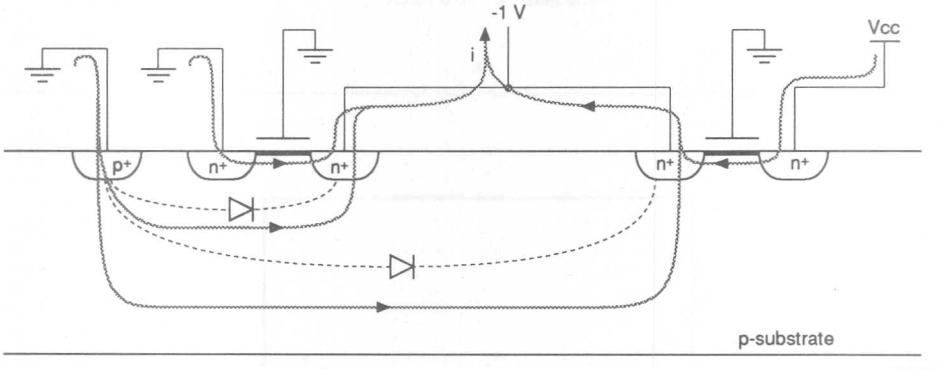


Figure 38. Definition of Negative Overshoot and Undershoot



16507A-065A

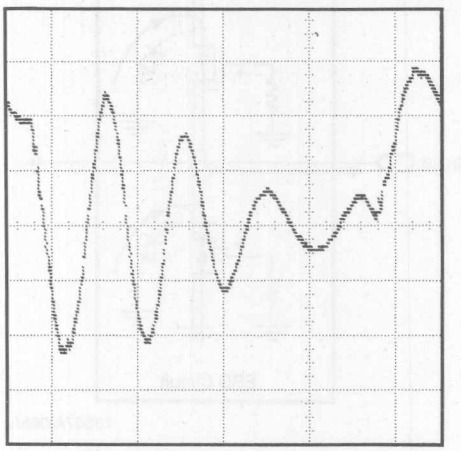
a.



16507A-066A

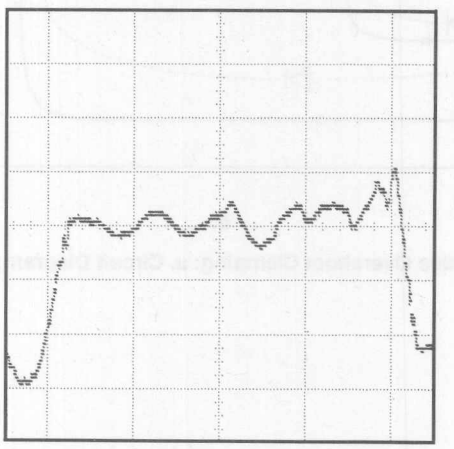
b.

Figure 39. Negative Overshoot Clamping: a. Circuit Diagram; b. Cross-Section



Ch. 1 = 2.000 volts/div
Timebase = 50.0 ns/div

a.



Ch. 1 = 2.000 volts/div
Timebase = 50.0 ns/div

b.

Figure 40. The Effect of Clamping: a. Signal Driving Empty Socket; b. Signal Driving Same Socket with CMOS PAL Device in It

Positive Overshoot

Large amounts of positive overshoot (Figure 41) can be a problem on most PLDs, regardless of technology or vendor. This is because most PLDs are programmed using *supervoltages*, and the pins therefore have supervoltage detectors that turn on the programming or test circuits, and potentially disable parts of the normal operating circuitry.

If there is too much positive overshoot, the signal can travel into the programming voltage range, briefly activating the programming circuitry. This can result in functional interruptions, such as outputs momentarily starting to disable or going from HIGH to LOW.

For earlier devices, the problem can only be avoided by revising the design to reduce the overshoot. A particular design in a particular device might work, but this might be because that device has no supervoltage function on that particular pin. But if you use an alternate source with different supervoltage pins, the design might not work.

New AMD CMOS devices incorporate a filter, or delay circuit, that delays the reaction of the programming circuit for about 100 ns. This is enough to reject overshoot signals, which usually last for less than 30 ns. Positive overshoot wil not cause any functional interruptions on devices with this protection (see Figure 42).

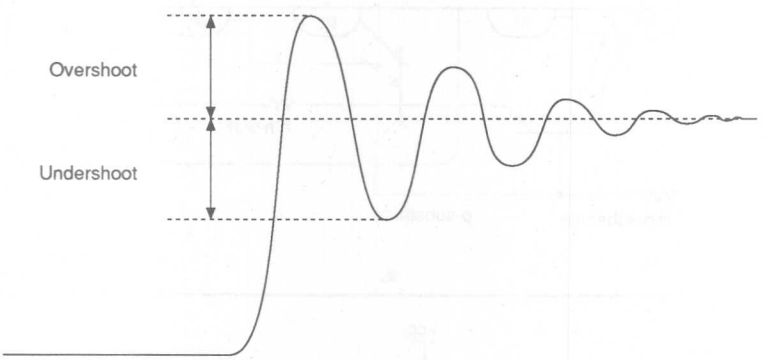


Figure 41. Definition of Positive Overshoot and Undershoot

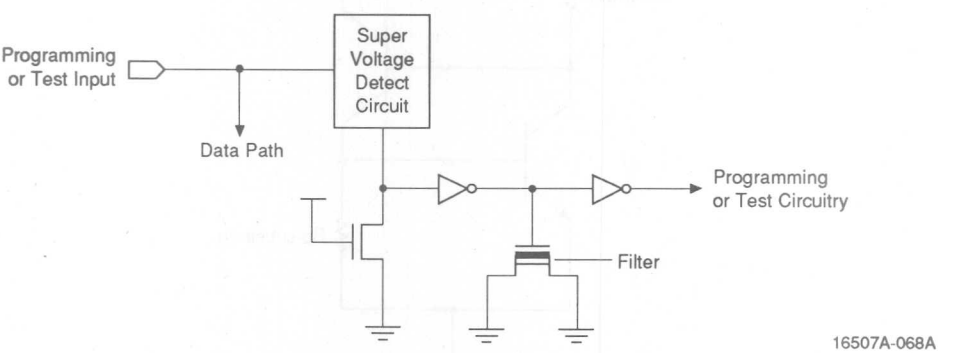
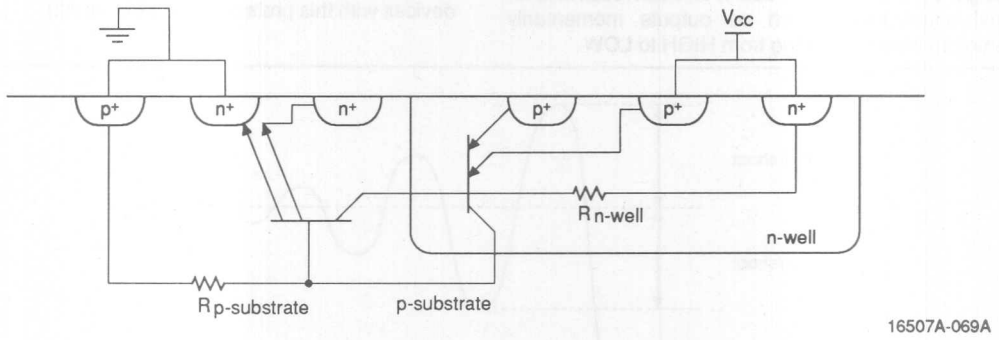


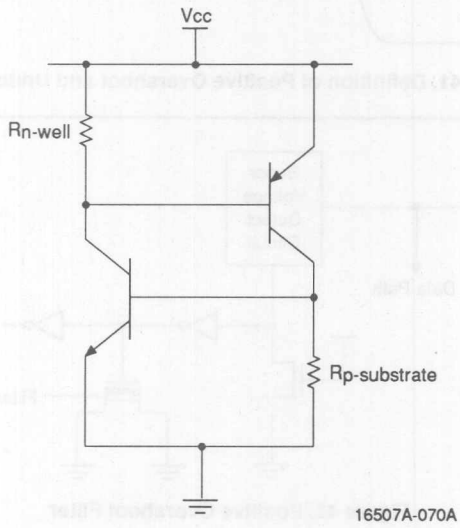
Figure 42. Positive Overshoot Filter

Latch-up occurs as a result of parasitic bipolar transistors between the n-channel and p-channel devices (see Figure 43a). These transistors form a parasitic SCR (see Figure 43b), which turns ON when triggered, conducting large amounts of current. It is usually impossible to shut OFF without removing all power from the device. The amount of current drawn is so high that it can either overload a power supply or, if the power supply can supply huge amounts of current, destroy the device.

enough current drawn to cause the SCR to turn on. This condition usually occurs when hot-socketing a vulnerable part; i.e., plugging a part into a powered up board or inserting a board into a powered-up system. When this happens, the inputs and V_{CC} power up uncontrolled, and there is a risk of latch-up.



a.



b.

Figure 43. Latchup Mechanism: a. Cross-Section; b. Equivalent Schematic

TTL-compatible outputs are intrinsically less susceptible to latch-up, since they have no p-channel pull-up. This accounts for nearly all of AMD's CMOS PLDs; these devices can be used for hot-insertion.

For true CMOS outputs, the SCR is an intrinsic part of the CMOS structure and cannot be eliminated. The SCR must be made as difficult as possible to turn ON by using guard rings and very carefully laying out input and output circuits. All of AMD's CMOS devices are guaranteed to endure a current pulse of 100 mA into or out of the pin without inducing latch-up; most devices can actually withstand over 500 mA. Since AMD's zero-power parts

and the PALCE610H-15 have true CMOS outputs, hot insertion is not recommended.

COMPATIBILITY WITH BIPOLAR

Most of the CMOS PLDs are designed to be compatible with TTL circuits; indeed, many designers have replaced bipolar TTL devices with a CMOS equivalent. Often this can be done blindly without affecting system performance. The interface levels are compatible and should pose no problems. Even the zero-power parts have been designed with input buffers that can respond to TTL or CMOS signals.

However, when making such a conversion, some details require attention, especially in cases where a straight conversion appears not to work.

Ground Bounce

Because CMOS devices generally have higher output slew rates, designs having many outputs switching at the same time (particularly if the outputs are heavily loaded) can cause more ground bounce than that generated by a comparable TTL device. It is important to use devices with output slew rate control.

The slew-rate-limiting circuits help minimize the occurrence of conversion problems, but even when the output slew rate is limited, the signal still can switch more quickly than that from a TTL output. If a design cannot be modified to accommodate the faster edge rates, this ground bounce may make a conversion unfeasible. If design changes are possible, any of the following can be tried:

- Limit the number of outputs that can switch at once.
- Reduce the loading on the outputs.
- Go to a lower-lead-inductance package (like a PLCC).
- Ensure that the ground path on the circuit board has low inductance.

Overshoot

The other possible problem when converting from bipolar to CMOS is reaction to signal overshoot in a noisy system. This is only an issue if the CMOS device has no overshoot protection. Overshoot sensitivity is not specifically related to CMOS, but results from programming algorithms being different between the technologies. This also can occur when changing between bipolar vendors, or when changing between CMOS vendors. If the noise on a signal can disturb supervoltage circuitry, this can be troublesome.

Different devices have different sensitivities; this accounts for some of the apparent incompatibility. However, the culprit usually is the fact that supervoltages appear on different pins for different devices, and the supervoltage functions vary. Thus, overshoot on one pin of a particular bipolar device might have had no effect. Once that device is changed (whether to CMOS or any other device that has no overshoot filter), the new device might react to the overshoot and cause problems.

The solution is to ensure that all signals are clean and have minimal overshoot, making them compatible with any device. Signal noise reduction can be accomplished most effectively by controlling the impedance of the signal traces and terminating correctly. As an alternative, if the driving device has extremely fast edge rates, it can be replaced with a device that has better controlled output slew rates.

Direct JEDEC File Conversions from Bipolar to CMOS

With some CMOS devices (most notably the PALCE16V8 and PALCE20V8), converting logic from a bipolar device is particularly simple once the noise issues have been addressed. This can be done in the programmer or by conversion software. It only affects the JEDEC file; the source file is not required. Generally, this is recommended only for designs whose source file is not available. If the source file is available, it is recommended that you change the device type in the source file, and then recompile to generate a new JEDEC file. This permits better documentation and revision control, since the source file is then consistent with the JEDEC file being used in production.

SUMMARY

By concentrating on the needs of CMOS PLD users, AMD has developed industry-leading CMOS technology that can provide cost-effective PLDs of unequalled quality, reliability, and performance. AMD provides value through:

- AMD-owned fabs, for better control of quality, reliability, volume, and costs
- electrical erasure, for higher quality and lower cost
- the highest performance available
- robust technology that is quiet and yet tolerant of noise
- an extremely broad offering of products; low and high density, low and zero power

This application note has detailed many of the aspects of the technology that make it superior to any alternatives. This, together with the information in the individual data sheets, qualification books, and a crew of applications engineers, should provide answers to your questions as you make use of AMD's CMOS PLD technology.

INDEX

charge pump
- latch-up protection ... 4-4
- negative substrate ... 4-3
- noise ... 4-4

compatibility with bipolar ... 4-37
- ground bounce ... 4-37
- input thresholds ... 4-37
- JEDEC file conversion ... 4-37
- overshoot ... 4-37

contact dimension ... 4-3
control gate ... 4-4 et seq
coupling ratio ... 4-9
data retention ... 4-13
- Arrhenius function ... 4-14
- bake ... 4-14
- effect of external fields ... 4-14
- thermal leakage ... 4-13
- value of activation energy ... 4-14

depletion mode transistor ... 4-3
endurance ... 4-14
ESD ... 4-30
- powered down ... 4-30
- overshoot clamping ... 4-32

FIT rates ... 4-30
floating gate ... 4-4 et seq
FusionPLD program ... 4-13
gate length ... 4-3
gate oxide thickness ... 4-3
ground bounce ... 4-31, 4-37
- ground lead inductance ... 4-31, 4-37

hot electron injection ... 4-4
hot insertion ... 4-30, 4-36, 4-37
I-V curves ... 4-21
impedances ... 4-21
input pull-ups ... 4-24
inputs
- connection to array ... 4-12, 4-13
- ESD protection ... 4-30
- floating ... 4-24
- hot insertion ... 4-30
- I-V curves ... 4-21
- impedance ... 4-21
- overshoot clamping ... 4-30, 4-32
- overshoot filter ... 4-35
- powered down ... 4-29
- pull-up resistors ... 4-24
- state during power-up ... 4-25
- structure ... 4-20
- transition detectors ... 4-15
- TTL, CMOS compatibility ... 4-37
- voltage level ... 4-16

power consumption ... 4-15
JEDEC file conversion ... 4-37
JEDEC load standard ... 4-24
latch-up ... 4-36
hot insertion ... 4-30
negative substrate ... 4-4
relationship to overshoot ... 4-4
L_{eff} ... 4-3
MACH output load ... 4-24
margin voltage ... 4-14
metal interconnect ... 4-3
pitch ... 4-3
minimum feature ... 4-3
n-well structure ... 4-3
noise ... 4-30
ground bounce ... 4-31
overshoot sensitivity ... 4-32
latch-up ... 4-36
outputs
as ESD protection ... 4-30
as overshoot clamp ... 4-32
behavior due to overshoot ... 4-35
compatibility with TTL, HC/HCT ... 4-3, 4-37
current limiting ... 4-24
drive ... 4-24
floating ... 4-24
ground bounce ... 4-31
HC/HCT-compatible ... 4-30
hot insertion ... 4-30
I-V curves ... 4-22
impedance ... 4-22
load ... 4-24
power dissipation ... 4-15
powered down ... 4-27
pull-up transistors ... 4-3
rail-to-rail ... 4-3, 4-23
rise and fall times ... 4-24
role in latch-up ... 4-30, 4-21
short-circuit current ... 4-36
slew rate ... 4-24, 4-37
structure ... 4-20
TTL-compatible ... 4-30
overshoot
causes ... 4-32
clamping ... 4-3, 4-21, 4-30, 4-32
CMOS vs bipolar ... 4-37
filter ... 4-35
negative ... 4-4, 4-21, 4-30, 4-32
positive ... 4-35

INDEX (continued)

relationship to latch-up 4-4
overshoot clamping 4-5, 4-21, 4-30, 4-32
role of ESD structure 4-30
poly-silicon interconnect 4-3
elimination of second layer 4-8
power dissipation 4-15
frequency 4-16
input voltage 4-16
output loading 4-18
product terms 4-18
temperature 4-18
Vcc 4-19
power-up
latch-up 4-4
reset 4-25
power-up reset 4-25
powered-down characteristics 4-27
programmable array 4-3
area 4-8
configuration 4-12
power consumption 4-15
programmers 4-13
programming cell . . . . 4-8 et seq
data retention 4-13
endurance 4-14
implant 4-8
programming and erasure mechanisms . . . . 4-8 et seq
self-limiting programming 4-9, 4-13
underprogramming, undererasure 4-13
propagation delay 4-24
rise and fall times 4-24
reliability 4-30
SCR 4-36
substrate 4-3
as source of electrons for UV parts 4-4
floating, negative 4-3
grounded 4-3
overshoot clamping 4-33
supervoltages 4-35
transmission lines 4-32
tunnel oxide
cell endurance 4-14
coupling ratio 4-9
data retention 4-13
field across 4-6
thickness relative to UV 4-6
tunneling 4-6
direct 4-6, 4-13
Fowler-Nordheim 4-6
UV-erasable devices 4-4
compared with EE 4-6
yields, programming and functional 4-13

INDEX (continued)

testing to ensure 4-6, 4-14
zero-power devices 4-4, 4-15
compatibility with TTL 4-37
hot insertion 4-37
I-V curves 4-23
output load 4-24
power dissipation 4-15
product-term power down 4-18
rail-to-rail operation 4-3, 4-15, 4-23
role of grounded substrate 4-3


PAL

Military PAL Devices

Advanced Micro Devices

Advanced Micro Devices' Military Programmable Array Logic (PAL) devices provide state machine and combinatorial logic solutions processed to military criteria. We offer the largest number of Standard Military Drawing PAL products in the industry.

Applications for our configurable PAL architectures include counters, shift registers, accumulators, control sequence generators, decoders, multiplexers, adders, memory mapped I/O and much more. These designs go into radar systems, missile guidance, avionics, airport graphic terminals, parallel processors, military computer hardware, and product obsolescence solutions, just to name a few.

Military PAL Device Menu

Family	Part Number	Package	Technology	Inputs	I/O	Outputs	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
16R8	PAL16L8-10 PAL16R8-10 PAL16R6-10 PAL16R4-10	/BRA /B2A	TTL	10 8 8 8	6 Comb – 2 Comb 4 Comb	2 Comb 8 Reg 6 Reg 4 Reg	7 8 7,8 7,8	10	10	210
	PAL16L8-12 PAL16R8-12 PAL16R6-12 PAL16R4-12	/BRA /B2A						12	47.6	210
	PAL16L8B PAL16R8B PAL16R6B PAL16R4B	20L, J, W						20	28.5	180
	PAL16L8B-2 PAL16R8B-2 PAL16R6B-2 PAL16R4B-2							30	20	90
	PAL16L8A PAL16R8A PAL16R6A PAL16R4A							30	20	180
	PAL16L8B-4 PAL16R8B-4 PAL16R6B-4 PAL16R4B-4							50	13.3	55
20R8	PAL20L8-10 PAL20R8-10 PAL20R6-10 PAL20R4-10	/BLA, /B3A	TTL	14 12 12 12	6 Comb – 2 Comb 4 Comb	2 Comb 8 Reg 6 Reg 4 Reg	7 8 7,8 7,8	10	50	210
	PAL20L8-12 PAL20R8-12 PAL20R6-12 PAL20R4-12							12	41.7	210
	PAL20L8-15 PAL20R8-15 PAL20R6-15 PAL20R4-15							15	35.7	210

Military PAL Device Menu (Continued)

Family	Part Number	Package	Technology	Inputs	I/O	Outputs	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
20R8	PAL20L8B	24JS, W, 28L	TTL	14	6 Comb	2 Comb	7	20	28.5	210
	PAL20R8B			12	–	8 Reg	8			
	PAL20R6B			12	2 Comb	6 Reg	7,8			
	PAL20R4B			12	4 Comb	4 Reg	7,8			
	PAL20L8A							30	20	210
	PAL20R8A									
	PAL20R6A									
	PAL20R4A									

Universal PAL Devices

Family	Part Number	Package	Technology	Inputs	I/O	Product Terms/Output	Features	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
22V10	PAL22V10-12	/BLA, /BKA	TTL	12	10 Macro	8-16	Varied Term	12	50	200
	PAL22V10-20	/B3A					Distribution	20	31.2	200
	AmPAL22V10A							30	22	180
	AmPAL22V10							40	16.5	180
	PALCE22V10H-15		EE CMOS					15	50	120
	PALCE22V10H-20							20	33.3	120
	PALCE22V10H-25							25	26.3	100
	PALCE22V10H-30							30	25	100
20V8	PALCE20V8H-15	/BLA, /B3A	EE CMOS	12	8 Macro	8	GAL® Device Equivalent	15	41.6	130
	PALCE20V8H-20							20	33.3	130
	PALCE20V8H-25							25	25	130
16V8	PALCE16V8H-15	/BRA, /B2A	EE CMOS	8	8 Macro	8	GAL® Device Equivalent	15	41.6	130
	PALCE16V8H-20							20	33.3	130
	PALCE16V8H-25							25	28.6	130

Asynchronous PAL Device

Family	Part Number	Package	Technology	Inputs	Macro	Product Terms/Output	Clock Cells	Other Features	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
610	PALCE610H-20	/BLA, /B3A	EE CMOS	4	16	8	Program-mable	J-K Flip-Flops	20	35.8	90

MACH Family (Macro Array CMOS High-density)

Family	Part Number	Package	Technology	Inputs	Output Macro	Buried Macros	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
MACH 1	MACH110–20	44CQFP	EE CMOS	6	32	–	0–12	20	40	170
MACH 1	MACH130–20	84CQFP	EE CMOS	6	64	–	0–12	20	40	220
MACH 2	MACH210–20	44CQFP	EE CMOS	6	32	32	0–16	20	40	195

Standard Military Drawing Program

AMD is an active participant in the Standard Military Drawing (SMD) Program. The idea behind the SMD Program is to standardize MIL-STD-883, Class B microcircuits. The advantage to the user is that SMDs are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Standard Military Drawings should always be considered to improve availability over source control drawings. It is standard practice at AMD to convert our 883, Class B processing to SMDs for all products which we are approved to supply. AMD then dual marks these devices with both the SMD number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and Distributor channels.

AMD will continue to work closely with DESC, generating new drawings, which will provide a steady flow of advanced technology products to standardize specifications.

Product Introduction Procedures

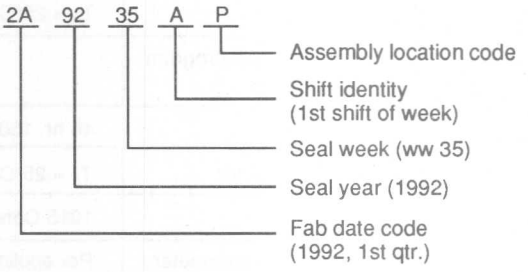
All new military products released by the Programmable Logic Products Division must successfully pass MIL-STD-883 Class B processing prior to new product announcement. This practice allows us to do checkout of bonding diagrams, electrical test tapes and burn circuits in a manufacturing environment. Programmability is checked when applicable. Our Engineering Department reviews electrical data to insure performance and yields to military data sheet limits are acceptable, prior to new product release. This procedure allows AMD to keep manufacturing start-up problems to a minimum on new product orders.

Manufacturing and Screening Locations

MIL-STD-883 Class B products, and orders to source control drawings, are assembled at our Penang, Malaysia facility. This facility is qualified by AMD Quality Department, as well as by many of our customers, to manufacture non-MIL-STD-883 Class B products. Conformance to MIL-STD-883 requirements is routinely monitored through audits at the Penang facility.

Assembly location as well as fabrication and seal date codes are included in AMD's part marking.

Example:



Assembly Location Codes:

Blank	Sunnyvale
M	Manila
P	Penang

Standard Military Flow Chart

Screening	Class B	Requirements
Assembly	Offshore assembly	
Internal visual	2010 cond. B	100%
Temperature cycling	1010	100%
Constant acceleration	2001 test cond. D or E Y1 orientation only	100%
Interim electrical parameter (1)	Per applicable device (1) specification T_A = 25°C only	100%
*100 Cycles bulk program and erase (2)		100%
*Bake	48 hr. 150°C	100%
*Post bake electric	T_A = 25°C	100%
Burn In	1015 Cond. C or D	100%
Post electrical parameters	Per applicable device specification T_A = 25°C only	100%
Percent defect allowable	DC Parameters PDA = 5% or 1 device whichever is greater	
Final electrical parameters (hot and cold extremes)	Per applicable device specification	100%
Seal A) Fine B) Gross	1014 Cond, A or B cond C	100%
Group A lot	5005 Class B	Sample every lot
Group B inspection lot Group C Group D External visual	5005 Class B 5005 Class B 5005 Class B 2009	Every lot Every 4 qtrs. of fab date code Every 52 weeks 100%

*EE CMOS Devices

(1) Programming and verification are performed at 25°C only

(2) May be performed at wafer sort.

Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"

Mil-0-9858, "Quality Program Requirements"

Mil-1-45208, "Inspection System Requirements"

Quality Assurance

The Programmable Logic Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of MIL-STD-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 slash sheet sample plans and approved SMD sample plans.

Product Qualification/Quality Conformance Inspection (QCI)

AMD has a quality conformance testing program in accordance with MIL-STD-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that AMD, as a minimum, conduct qualification testing per Company Policy specification on Product Reliability Qualification (00–021). Once qualified, each package type (from each assembly line) and device (by technology group as delineated in MIL-M-38510) are incorporated into AMD Quality Conformance Inspection program which utilizes the requirements of MIL-STD-883.

When military programs do not require that QCI data be run on the specific lot shipped, AMD Quality Conformance program allows customers to obtain generic data on all product families manufactured by AMD Generic Qualification Data enables customers to eliminate costly qualification and destruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following product data is available:

Group B – Package Related Tests

- QCI is performed in line on each inspection lot.
- Purpose: To monitor assembly and device package integrity.

Group C – Product/Process Related Tests

- Group C is performed based on fab date code, at least every four quarters.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and the parametric performance for each product technology.

Group D – In-Depth Package Related Tests

- QCI is conducted every 52 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Process Audits

Process Audits are performed in accordance with Mil-M-38510, Appendix A, (self audits) by the Quality Assurance Department.

Electrostatic Discharge Control Procedures

AMD fully employs static control procedures throughout its facilities.

All manufacturing areas where product is processed or handled including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.

All product is moved throughout our facilities and shipped to customers in static shielded containers.

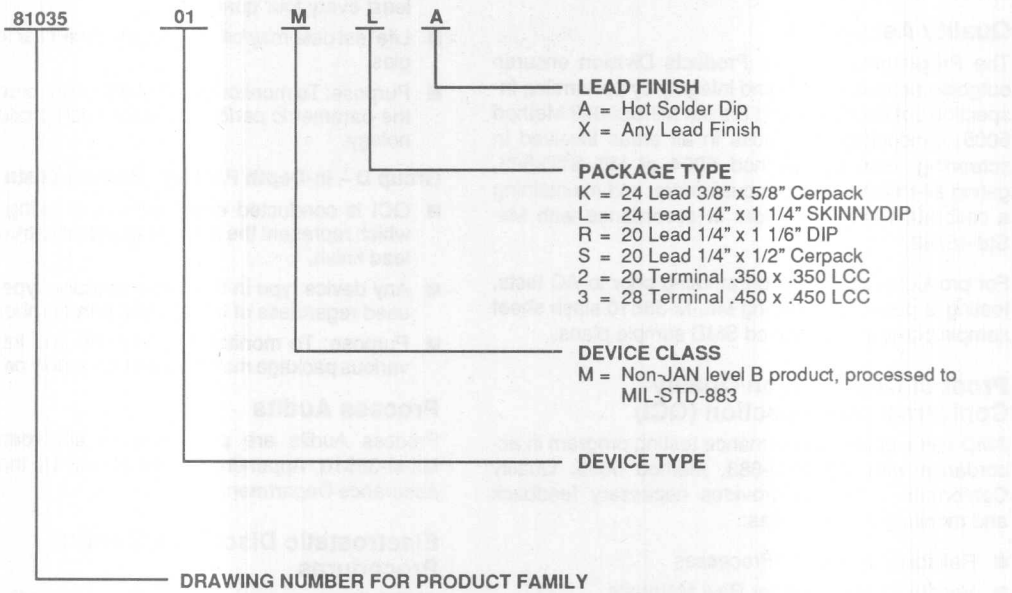
In addition, AMD distributors must demonstrate that they meet the same stringent standards regarding ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by AMD's Quality Assurance Department.

An ESD identifier is marked on all products per MIL-STD-883 1.2.1 b (30). All shipping containers are labeled with an ESD Caution Message. ESD procedures are continually reviewed, to ensure that our customers receive only the highest quality product from AMD.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



PART NUMBER INTERPRETATION:
When ordering to Military Drawing numbers, the lead finish designator (last letter in part number) is commonly called out as "X." This is a way of stating that the customer will accept the standard manufacturer's lead finish for the package orders. "X" is not a lead finish designator in itself, therefore, when product is shipped, the actual lead finish designator will be marked on the devices.

Military SMDs

Military Drawing	AMD Part Number	Military Drawing	AMD Part Number
8103501RA	PAL10H8MJ/883B	84129033A	PAL20R6AML/883B
81035012A	PAL10H8ML/883B	8412903KA	PAL20R6AMW/883B
8103501SA	PAL10H8MW/883B	8412904LA	PAL20R4AMJS/883B
8103502RA	PAL12H6MJ/883B	84129043A	PAL20R4AML/883B
81035022A	PAL12H6ML/883B	8412904KA	PAL20R4AMW/883B
8103502SA	PAL12H6MW/883B	8412905LA	PAL20L10AMJS/883B
8103503RA	PAL14H4MJ/883B	84129053A	PAL20L10AML/883B
81035032A	PAL14H4ML/883B	8412905KA	PAL20L10AMW/883B
8103503SA	PAL14H4MW/883B	8412906LA	PAL20X8AMJS/883B
8103504RA	PAL16H2MJ/883B	84129063A	PAL20X8AML/883B
81035042A	PAL16H2ML/883B	8412906KA	PAL20X8AMW/883B
8103504SA	PAL16H2MW/883B	8412907LA	PAL20X10AMJS/883B
8103505RA	PAL16C1MJ/883B	84129073A	PAL20X10AML/883B
81035052A	PAL16C1ML/883B	8412907KA	PAL20X10AMW/883B
8103505SA	PAL16C1MW/883B	8412908LA	PAL20X4AMJS/883B
8103506RA	PAL10L8MJ/883B	84129083A	PAL20X4AML/883B
81035062A	PAL10L8ML/883B	8412908KA	PAL20X4AMW/883B
8103506SA	PAL10L8MW/883B	8412909LA	PAL20L8A-2MJS/883B
8103507RA	PAL12L6MJ/883B	84129093A	PAL20L8A-2ML/883B
81035072A	PAL12L6ML/883B	8412909KA	PAL20L8A-2MW/883B
8103507SA	PAL12L6MW/883B	8412910LA	PAL20R8A-2MJS/883B
8103508RA	PAL14L4MJ/883B	84129103A	PAL20R8A-2ML/883B
81035082A	PAL14L4ML/883B	8412910KA	PAL20R8A-2MW/883B
8103508SA	PAL14L4MW/883B	8412911LA	PAL20R6A-2MJS/883B
8103509RA	PAL16L2MJ/883B	84129113A	PAL20R6A-2ML/883B
81035092A	PAL16L2ML/883B	8412911KA	PAL20R6A-2MW/883B
8103509SA	PAL16L2MW/883B	8412912LA	PAL20R4A-2MJS/883B
8103607RA	PAL16L8AMJ/883B	84129123A	PAL20R4A-2ML/883B
81036072A	PAL16L8AML/883B	8412912KA	PAL20R4A-2MW/883B
8103607SA	PAL16L8AMW/883B	8506501RA	PAL16L8A-4MJ/883B
8103608RA	PAL16R8AMJ/883B	85065012A	PAL16L8A-4ML/883B
81036082A	PAL16R8AML/883B	8506501SA	PAL16L8A-4MW/883B
8103608SA	PAL16R8AMW/883B	8506502RA	PAL16R8A-4MJ/883B
8103609RA	PAL16R6AMJ/883B	85065022A	PAL16R8A-4ML/883B
81036092A	PAL16R6AML/883B	8506502SA	PAL16R8A-4MW/883B
8103609SA	PAL16R6AMW/883B	8506503RA	PAL16R6A-4MJ/883B
8103610RA	PAL16R4AMJ/883B	85065032A	PAL16R6A-4ML/883B
81036102A	PAL16R4AML/883B	8506503SA	PAL16R6A-4MW/883B
8103610SA	PAL16R4AMW/883B	8506504RA	PAL16R4A-4MJ/883B
8103612RA	PAL16R8A-2MJ/883B	85065042A	PAL16R4A-4ML/883B
81036122A	PAL16R8A-2ML/883B	8506504SA	PAL16R4A-4MW/883B
8103612SA	PAL16R8A-2MW/883B	5962-8515501RA	PAL16L8BMJ/883B
8103613RA	PAL16R6A-2MJ/883B	5962-85155012A	PAL16L8BML/883B
81036132A	PAL16R6A-2ML/883B	5962-8515501SA	PAL16L8BMW/883B
8103613SA	PAL16R6A-2MW/883B	5962-8515502RA	PAL16R8BMJ/883B
8103614RA	PAL16R4A-2MJ/883B	5962-85155022A	PAL16R8BML/883B
81036142A	PAL16R4A-2ML/883B	5962-8515502SA	PAL16R8BMW/883B
8103614SA	PAL16R4A-2MW/883B	5962-8515503RA	PAL16R6BMJ/883B
8412901LA	PAL20L8AMJS/883B	5962-85155032A	PAL16R6BML/883B
84129013A	PAL20L8AML/883B	5962-8515503SA	PAL16R6BMW/883B
8412901KA	PAL20L8AMW/883B	5962-8515504RA	PAL16R4BMJ/883B
8412902LA	PAL20R8AMJS/883B	5962-85155042A	PAL16R4BML/883B
84129023A	PAL20R8AML/883B	5962-8515504SA	PAL16R4BMW/883B
8412902KA	PAL20R8AMW/883B	5962-8515505RA	PAL16L8B-2MJ/883B
8412903LA	PAL20R6AMJS/883B	5962-85155052A	PAL16L8B-2ML/883B

Military Drawing	AMD Part Number	Military Drawing	AMD Part Number
5962-8515505SA	PAL16L8B-2MW/883B	5962-8680401KA	PAL18L4MW/883
5962-8515506RA	PAL16R8B-2MJ/883B	5962-8680402LA	PAL12L10MJS/883B
5962-85155062A	PAL16R8B-2ML/883B	5962-86804023A	PAL12L10ML/883B
5962-8515506SA	PAL16R8B-2MW/883B	5962-8680402KA	PAL12L10MW/883B
5962-8515507RA	PAL16R6B-2MJ/883B	5962-8680403LA	PAL14L8MJS/883B
5962-85155072A	PAL16R6B-2ML/883B	5962-86804033A	PAL14L8ML/883B
5962-8515507SA	PAL16R6B-2MW/883B	5962-8680403KA	PAL14L8MW/883B
5962-8515508RA	PAL16R4B-2MJ/883B	5962-8680404LA	PAL16L6MJS/883B
5962-85155082A	PAL16R4B-2ML/883B	5962-86804043A	PAL16L6ML/883B
5962-8515508SA	PAL16R4B-2MW/883B	5962-8680404KA	PAL16L6MW/883B
5962-8515509RA	PAL16L8DMJ/883B	5962-8680405LA	PAL20L2MJS/883B
5962-85155092A	PAL16L8DML/883B	5962-86804053A	PAL20L2ML/883B
5962-8515509SA	PAL16L8DMW/883B	5962-8680405KA	PAL20L2MW/883B
5962-8515510RA	PAL16R8DMJ/883B	5962-8680406LA	PAL20C1MJS/883B
5962-85155102A	PAL16R8DML/883B	5962-86804063A	PAL20C1ML/883B
5962-8515510SA	PAL16R8DMW/883B	5962-8680406KA	PAL20C1MW/883B
5962-8515511RA	PAL16R6DMJ/883B	5962-8753001LA	PAL20S10MJS/883B
5962-85155112A	PAL16R6DML/883B	5962-87530013A	PAL20S10ML/883B
5962-8515511SA	PAL16R6DMW/883B	5962-8753001KA	PAL20S10MW/883B
5962-8515512RA	PAL16R4DMJ/883B	5962-8753002LA	PAL20RS10MJS/883B
5962-85155122A	PAL16R4DML/883B	5962-87530023A	PAL20RS10ML/883B
5962-8515512SA	PAL16R4DMW/883B	5962-8753002KA	PAL20RS10MW/883B
5962-85155132A	PAL16L8-12/B2A	5962-8753003LA	PAL20RS8MJS/883B
5962-8515513RA	PAL16L8-12/BRA	5962-87530033A	PAL20RS8ML/883B
5962-85155142A	PAL16R8-12/B2A	5962-8753003KA	PAL20RS8MW/883B
5962-8515514RA	PAL16R8-12/BRA	5962-8753004LA	PAL20RS4MJS/883B
5962-85155152A	PAL16R6-12/B2A	5962-87530043A	PAL20RS4ML/883B
5962-8515515RA	PAL16R6-12/BRA	5962-8753004KA	PAL20RS4MW/883B
5962-85155162A	PAL16R4-12/B2A	5962-8767101LA	PAL20L8BMJS/883B
5962-8515516RA	PAL16R4-12/BRA	5962-87671013A	PAL20L8BML/883B
5962-85155172A	PAL16L8-10/B2A	5962-8767101KA	PAL20L8BMW/883B
5962-8515517RA	PAL16L8-10/BRA	5962-8767102LA	PAL20R8BMJS/883B
5962-85155182A	PAL16R8-10/B2A	5962-87671023A	PAL20R8BML/883B
5962-8515518RA	PAL16R8-10/BRA	5962-8767102KA	PAL20R8BMW/883B
5962-85155192A	PAL16R6-10/B2A	5962-8767103LA	PAL20R6BMJS/883B
5962-8515519RA	PAL16R6-10/BRA	5962-87671033A	PAL20R6BML/883B
5962-85155202A	PAL16R4-10/B2A	5962-8767103KA	PAL20R6BW/883B
5962-8515520RA	PAL16R4-10/BRA	5962-8767104LA	PAL20R4BMJS/883B
5962-8605301LA	AmPAL22V10A/BLA	5962-87671043A	PAL20R4BML/883B
5962-86053013A	AmPAL22V10A/B3A	5962-8767104KA	PAL20R4BMW/883B
5962-8605301KA	AmPAL22V10A/BKA	5962-8767107LA	PAL20L8-15/BLA
5962-8605302LA	AmPAL22V10/BLA	5962-87671073A	PAL20L8-15/B3A
5962-86053023A	AmPAL22V10/B3A	5962-8767108LA	PAL20R8-15/BLA
5962-8605302KA	AmPAL22V10/BKA	5962-87671083A	PAL20R8-15/B3A
5962-8605304LA	PAL22V10-20/BLA	5962-8767109LA	PAL20R6-15/BLA
5962-86053043A	PAL22V10-20/B3A	5962-87671093A	PAL20R6-15/B3A
5962-8605304KA	PAL22V10-20/BKA	5962-8767110LA	PAL20R4-15/BLA
5962-88063053A	PAL22V10-12/B3A	5962-87671103A	PAL20R4-15/B3A
5962-8605305KA	PAL22V10-12/BKA	5962-8767111LA	PAL20L8-12/BLA
5962-8605305LA	PAL22V10-12/BLA	5962-87671113A	PAL20L8-12/B3A
5962-8680301LA	PAL20RA10MJS/883B	5962-8767112LA	PAL20R8-12/BLA
5962-86803013A	PAL20RA10ML/883B	5962-87671123A	PAL20R8-12/B3A
5962-8680301KA	PAL20RA10MW/883B	5962-8767113LA	PAL20R6-12/BLA
5962-8680401LA	PAL18L4MJS/883B	5962-87671133A	PAL20R6-12/B3A
5962-86804013A	PAL18L4ML/883B	5962-8767114LA	PAL20R4-12/BLA

Military SMDs (continued)

Military Drawing	AMD Part Number	Military Drawing	AMD Part Number
5962-87671143A	PAL20R4-12/B3A	5962-8983902RA	PALCE16V8H-20E4/BRA
5962-8767115LA	PAL20L8-10/BLA	5962-89839032A	PALCE16V8H-15E4/B2A
5962-87671153A	PAL20L8-10/B3A	5962-8983903RA	PALCE16V8H-15E4/BRA
5962-8767116LA	PAL20R8-10/BLA	5962-89840013A	PALCE20V8H-25E4/B3A
5962-87671163A	PAL20R8-10/B3A	5962-8984001LA	PALCE20V8H-25E4/BLA
5962-8767117LA	PAL20R6-10/BLA	5962-89840023A	PALCE20V8H-20E4/B3A
5962-87671173A	PAL20R6-10/B3A	5962-8984002LA	PALCE20V8H-20E4/BLA
5962-8767118LA	PAL20R4-10/BLA	5962-89840033A	PALCE20V8H-15E4/B3A
5962-87671183A	PAL20R4-10/B3A	5962-8984003LA	PALCE20V8H-15E4/BLA
5962-8851501RA	PAL16L8B-4MJ/883B	5962-89841013A	PALCE22V10H-30/B3A
5962-88515012A	PAL16L8B-4ML/883B	5962-8984101KA	PALCE22V10H-30/BKA
5962-8851501SA	PAL16L8B-4MW/883B	5962-8984101LA	PALCE22V10H-30/BLA
5962-8851502RA	PAL16R8-4MJ/883B	5962-89841023A	PALCE22V10H-20E4/B3A
5962-88515022A	PAL16R8B-4ML/883B	5962-8984102KA	PALCE22V10H-20E4/BKA
5962-8851502SA	PAL16R8B-4MW/883B	5962-8984102LA	PALCE22V10H-20E4/BLA
5962-8851503RA	PAL16R6B-4MJ/883B	5962-89841043A	PALCE22V10H-25/B3A
5962-88515032A	PAL16R6B-4ML/883B	5962-8984104KA	PALCE22V10H-25/BKA
5962-8851503SA	PAL16R6B-4MW/883B	5962-8984104LA	PALCE22V10H-25/BLA
5962-8851504RA	PAL16R4B-4MJ/883B	5962-89841053A	PALCE22V10H-15E4/B3A
5962-88515042A	PAL16R4B-4ML/883B	5962-8984105KA	PALCE22V10H-15E4/BKA
5962-8851504SA	PAL16R4B-4MW/883B	5962-8984105LA	PALCE22V10H-15E4/BLA
5962-89839012A	PALCE16V8H-25E4/B2A	5962-9169501M3A	PALCE610H-20/B3A
5962-8983901RA	PALCE16V8H-25E4/BRA	5962-9169501MLA	PALCE610H-20/BLA
5962-89839022A	PALCE16V8H-20E4/B2A		

Military ProPAL™ Devices

The Advantages

An important service that AMD's Programmable Logic Division offers is ProPAL devices, the programming of a customer's PAL devices during the manufacturing cycle, saving aerospace customers significant time and money. We offer full 883, SMD, programmed products. Not only were we the first to offer this service, we by far have the most expertise in managing your programmed business.

The pre-programming of PAL devices for the customer offers a number of advantages, most of which increase the parts' reliability. Unlike a blank generic device, a ProPAL device undergoes a more thorough testing process. Listed below are just a few of the many advantages.

Enhanced Reliability

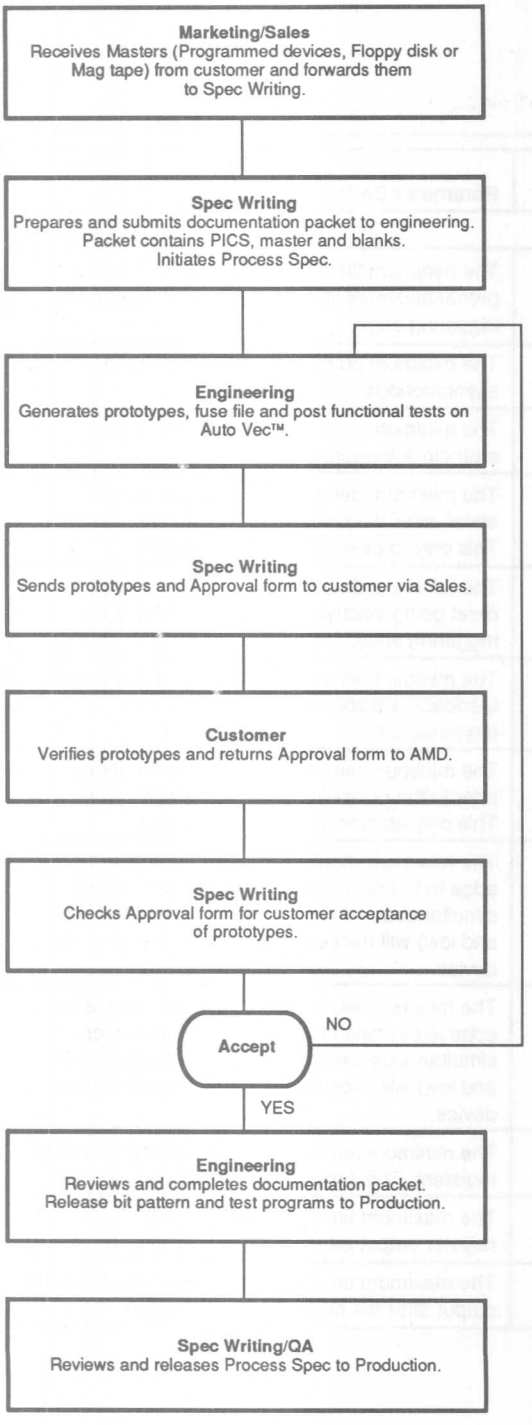
- In the design environment, the pattern undergoes fault simulation with > 90% coverage, providing a high testability. (Some patterns do not allow 90% fault coverage. In those cases the customer will be notified.)
- The parts are programmed prior to burn-in; weak parts are likely to fail to accept a program and be rejected on the spot.
- Programmed devices then must pass 25°C DC, functional and AC electrical tests prior to burn-in and DC, functional and AC electrical tests after burn-in, at temperature extremes, per M5004.

Although the price of the ProPAL device is higher than that of its unprogrammed counterpart, the added value provided to the user more than offsets the cost. In this era of cost-cutting and the need to get the most from each dollar spent, ProPAL devices make it possible for the customer to save money over the life of the project. Below are just a few examples of where cost savings can be recognized.

Cost Reduction Areas:

- The more thorough testing significantly increases the long term reliability of the device. System failures and resulting rework costs, owing to a defective PAL device, can easily be 50 times the purchase price of the component.
- The customer does not have to purchase and maintain costly programming and test facilities. He can concentrate on what he does best. . .design systems to aid in defense of our nation and allow AMD to do what we do best. . .produce and test Programmable Logic Devices.
- As volumes go up, the customer's production line won't be constrained by his programming and labeling capacities or throughput time.
- Inventories can be reduced. The customer no longer needs to store extra product for programming fall-out or human error.
- Improve lead time of manufacturing. The customer will no longer need to plan on internal time to program or label devices.

ProPAL Device Flow for Products with Existing Mil Shell Programs



Military Programming Process Summary

(per current Revisions of Mil–Std-883 and Mil-M-38510)

Assembly

Initial Electrical Test (25°C)	– 100% program to customer bit pattern
	– 100% DC/Functional/AC at 25°C, M5004
Burn-In	– Method 1015, Condition C or D
Electrical Test (25°C)	– 100% DC/Functional/AC at 25°C per M5004
	– Group A DC/Functional/ AC at 25°C per M5005
PDA	– 5% (DC only)
Solder Dip	
Mark	
Lot B Test	– Resistance to solvents, solderability, bond pull
	– M5005
Electrical Test (+125°C &–55°C)	– 100% DC/Functional/ AC, M5004
	– Group A DC/Functional/ AC, M5005
Hermiticity	– 100% Fine/Gross Leak per Method 1014
External Visual	– Method 2009
Data Review/Pack/Ship	

AMD is the proven technology leader in PAL devices and has numerous years of experience in programming customer patterns. Currently several major customers are using ProPAL devices and several major programs are being converted to ProPAL devices. Factory programming of your PAL device products is another service of the Military Programmable Logic's long-term partnership with and commitment to the worldwide Military and Aerospace market. For more information on Military ProPAL devices contact your local AMD sales office.

Parameter Symbol	Parameter Name	Parameter Definition
Timing		
t_{APR}	Asynchronous Preset Recovery Time	The minimum time after the asynchronous preset becomes inactive to the next input clock triggering edge.
t_{APW}	Asynchronous Preset Width	The minimum pulse width required for the asynchronous preset signal.
t_H	Hold Time	The minimum time a valid data level is held after clock triggering edge.
t_{HP}	Hold Time for Preload	The minimum delay time for data to remain stable after the preload signal becomes inactive. This only applies to TTL-level preload.
t_{SRR}	Synchronous Reset Recovery Time	The minimum time between the synchronous reset going inactive and the next input clock triggering edge.
t_S	Setup Time, Input or Feedback to Clock	The minimum time a valid data level of input or feedback is stable before the next clock triggering edge.
t_{SP}	Data Setup Time for Preload	The minimum time for input data to be stable prior to the preload signal becoming inactive. This only applies to TTL-level preload.
t_{WH}	Clock Width High	The minimum width of the clock high from rising edge to the next falling edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WL}	Clock Width Low	The minimum width of the clock low from falling edge to the next rising edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WP}	Preload Pulse Width	The minimum pulse width required to preload the registers. This only applies to TTL-level preload.
t_{AP}	Asynchronous Preset to Output	The maximum time required to preset the register output after the preset signal is asserted.
t_{AR}	Asynchronous Reset to Output	The maximum time required to reset the register output after the reset signal is asserted.

Parameter Symbol	Parameter Name	Parameter Definition
Timing		
t_{CO}	Clock to Register Output	The maximum time it takes to obtain a valid data level on the output pin after an input clock triggering edge is applied.
t_{CR}	Input or Feedback to Registered Output from Combinatorial Configuration; Output Mux Select 1 to 0	The minimum time from input or feedback to registered output as output mux selection changes from combinatorial to registered output 1 to 0).
t_{EA}	Output Enable Time, Clock to Output	The minimum delay between when an input is asserted and the output switches from a high-impedance state to HIGH or LOW logic state.
t_{ER}	Output Disable Time, Input to Output	The minimum delay between when an input is asserted and the output switches from a HIGH or LOW logic state to a high-impedance state.
t_F	Fall Time	The minimum time for a signal to fall from 80% to 20% of its stabilized high value.
t_{PD}	Propagation Delay, Input or Feedback to Combinatorial Output	The time for a signal to propagate from input or feedback to output.
t_{PR}	Power-up Reset Time	The minimum time for a registered output signal to be reset after the power is applied.
t_{PXZ}	Output Disable Time, OE to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a HIGH or LOW logic state to be a high-impedance state.
t_{PZX}	Output Enable Time, OE to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a high-impedance state to a HIGH or LOW logic state.
t_R	Rise Time	The minimum time for a signal to rise from 20% to 80% of its stabilized high value.
t_{RC}	Input or Feedback to Combinatorial Output from Registered Configuration; Output Mux Select 0 to 1	The minimum time from input or feedback to combinatorial output mux selection changes from registered to combinatorial output (0 to 1).
Voltage		
V_{CC}	Supply Voltage, Positive Potential	The voltage required across supply and ground terminals of a TTL or CMOS integrated circuit.
V_I	Input Clamp Voltage	The maximum input clamp voltage limit on every input pin.
V_{IH}	High-Level Input Voltage	The minimum high-level input voltage that is guaranteed to represent a high logic level.
V_{IL}	Low-Level Input Voltage	The maximum low-level input voltage that is guaranteed to represent a low logic level.
V_{OH}	High-Level Output Voltage	The minimum high logic level guaranteed for all outputs.
V_{OL}	Low-Level Output Voltage	The minimum low logic level guaranteed for all outputs.

Current		
I_{CC}	Supply Current, Corresponding to V_{CC}	The maximum current into the V_{CC} terminal of a TTL or CMOS integrated circuit.
I_I	Input Current with Maximum Input Voltage	The maximum current into an input pin when the input voltage is applied to the input pin.
I_{IH}	High-Level Input Current	The maximum current into an input pin when a logic-high level is applied to the input pin.
I_{IL}	Low-Level Input Current	The maximum current into an input pin when a logic-low level is applied to the input pin.
I_{OH}	High-Level Output Current	The maximum current into an output pin to guarantee an output logic-high level.
I_{OL}	Low-Level Output Current	The maximum current into an output pin to guarantee an output logic-low level.
I_{SC}	Output Short-Circuit Current	The current into an output when that output is short-circuited to ground (0.5 V).
I_{OZH}	High-Level Leakage Current	The maximum current into a high-impedance state output pin when a high logic level is applied to the output pin.
I_{OZL}	Low-Level Leakage Current	The maximum current into a high-impedance state output pin when a low logic level is applied to the output pin.
Miscellaneous		
C_{IN}	Input Capacitance	The input pin capacitance at a specified voltage and frequency.
C_{OUT}	Output Capacitance	The output or I/O pin capacitance at a specified voltage and frequency.
T_A	Operating Free Air Temperature	The ambient homogeneous temperature of the environment during operation.
T_C	Operating Case Temperature	The maximum chassis temperature during operation.
f_{MAX}	Maximum External Frequency	The $f_{MAX,\ External}$ is the maximum clocking frequency with external feedback. It is the reciprocal of the clock period ($t_S + t_{CO}$).
f_{MAX}	Maximum Internal Frequency	The $f_{MAX,\ Internal}$ is the maximum clocking frequency with internal feedback. An internal counter is used to determine "f_{CNT}."
f_{MAX}	Maximum Frequency without Feedback	The $f_{MAX,\ No\ Feedback}$ is the maximum clocking frequency with no feedback. It is the reciprocal of the sum of the data setup time (t_S) and the data hold time (t_H).

f_{MAX} Parameters

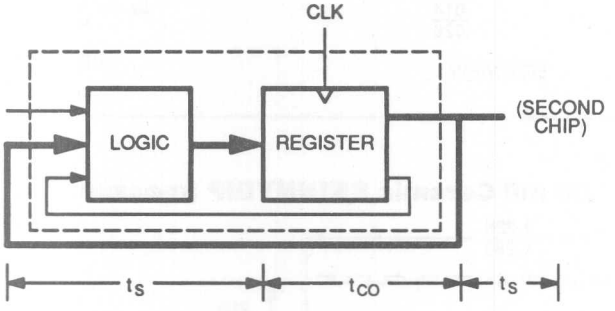
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

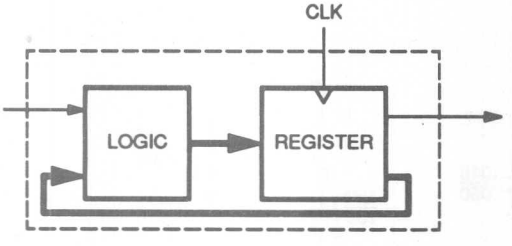
The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

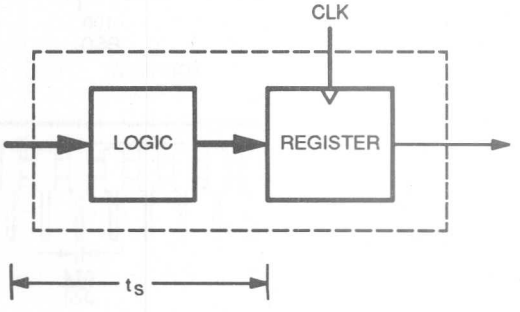
f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured.



f_{MAX} External; $1/(t_S + t_{CO})$



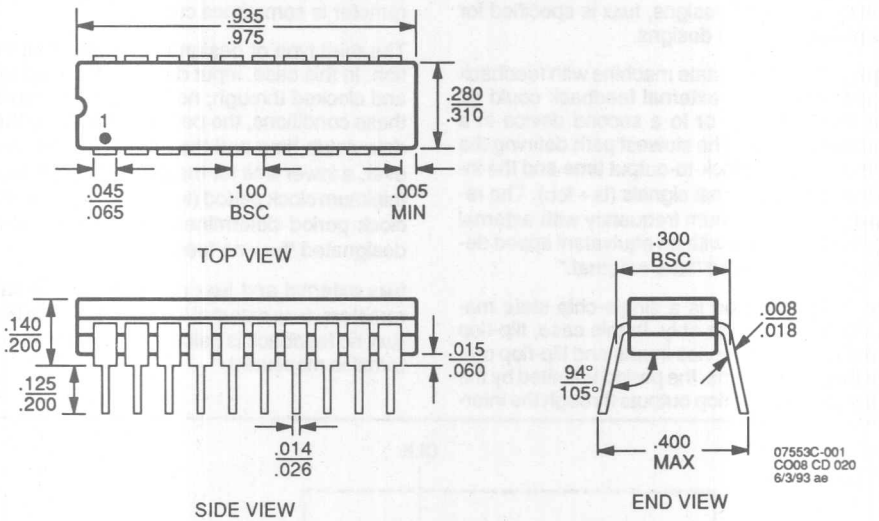
f_{MAX} Internal (f_{CNT})



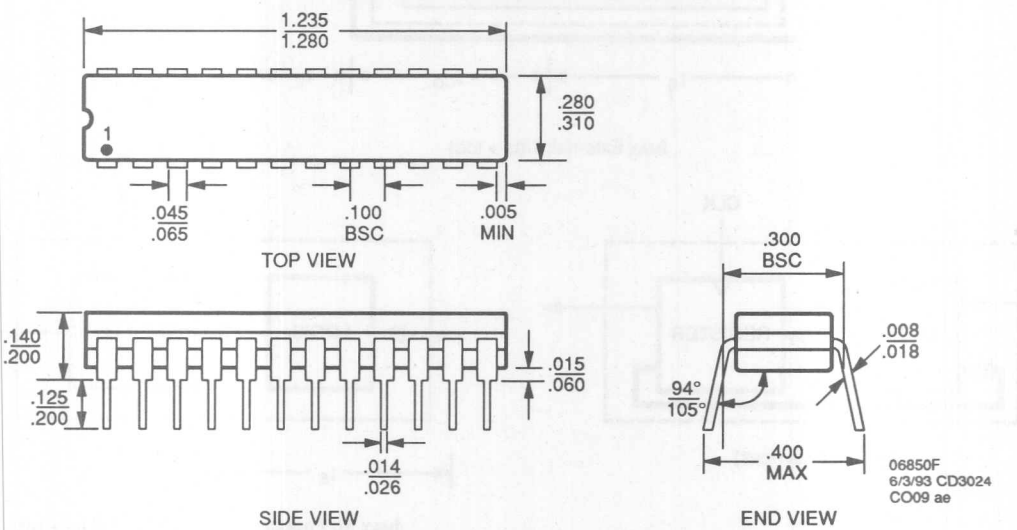
f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

PHYSICAL DIMENSIONS*

CD 020
20-Pin Ceramic DIP (measured in inches)

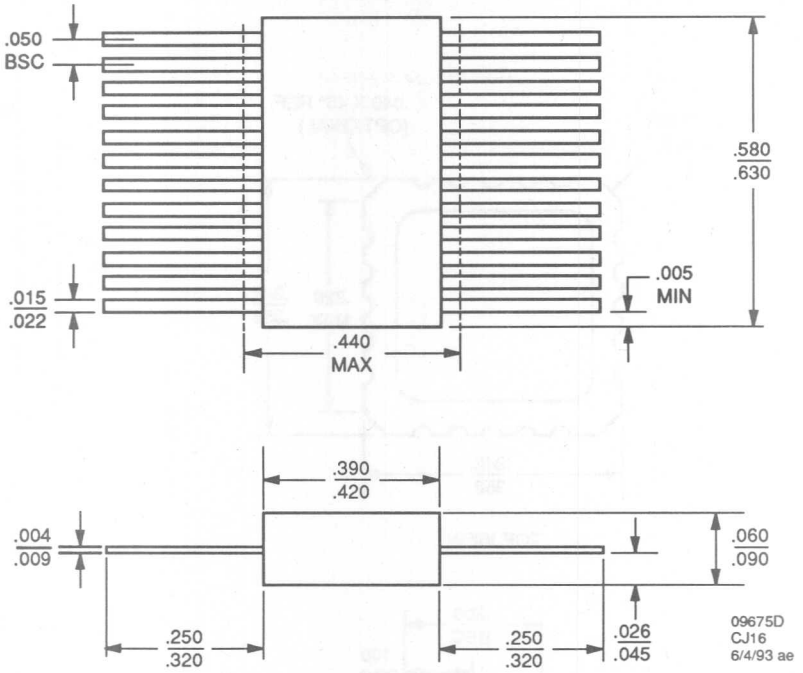


CD3024
24-Pin 300 mil Ceramic SKINNYDIP (measured in inches)

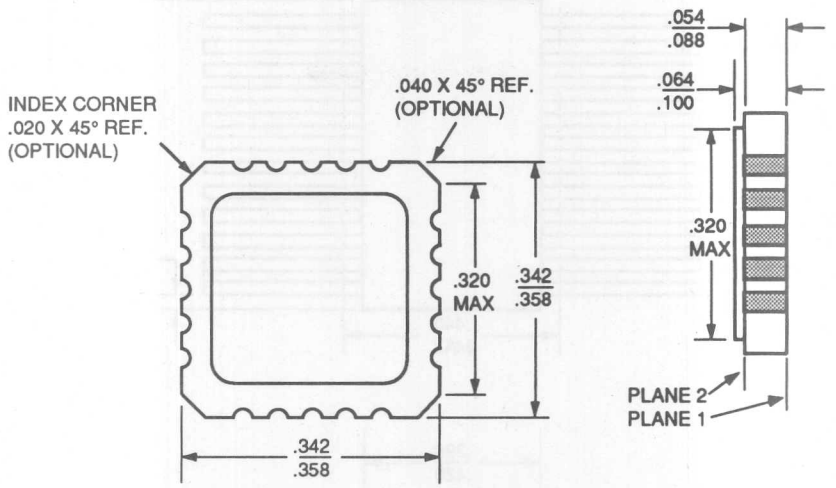


**For reference only. BSC is an ANSI standard for Basic Space Centering.*

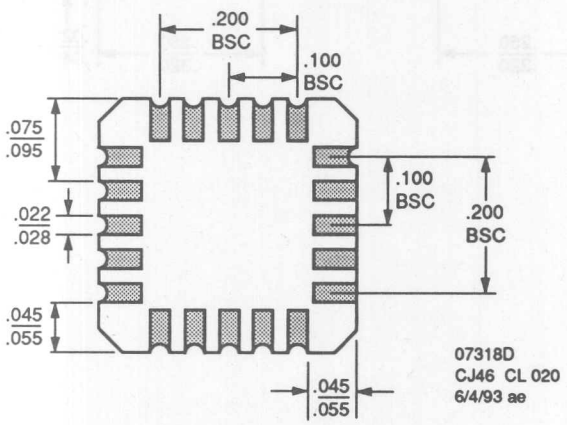
CFL024
24-Pin Ceramic Flatpack (measured in inches)



CL 020
20-Pin Ceramic Leadless Chip Carrier **(measured in inches)**

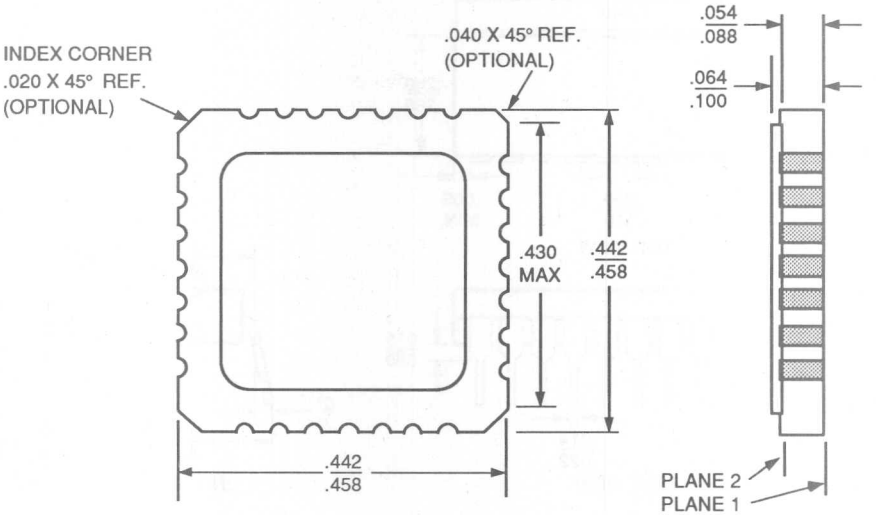


TOP VIEW

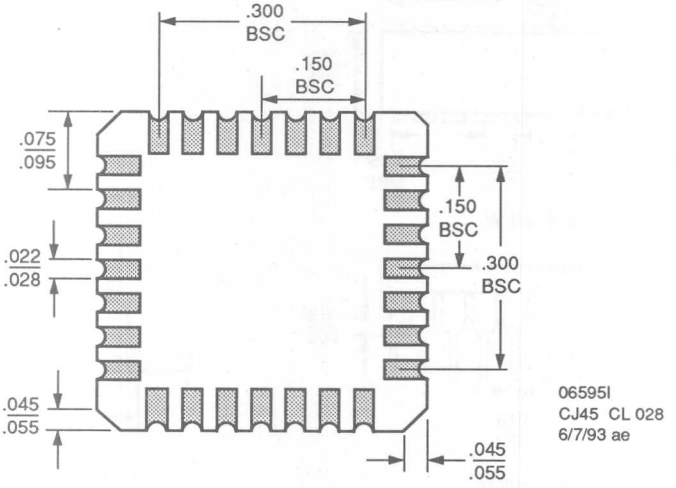


BOTTOM VIEW

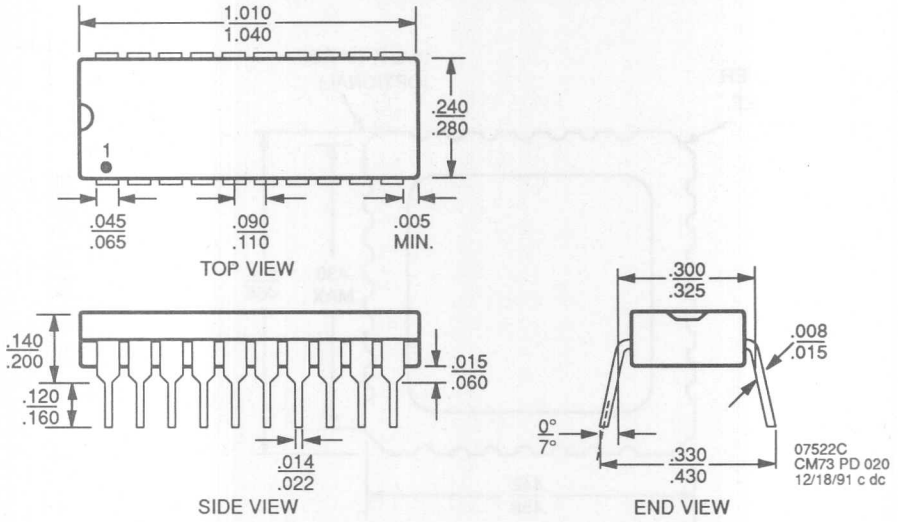
CL 028
28-Pin Ceramic Leadless Chip Carrier **(measured in inches)**



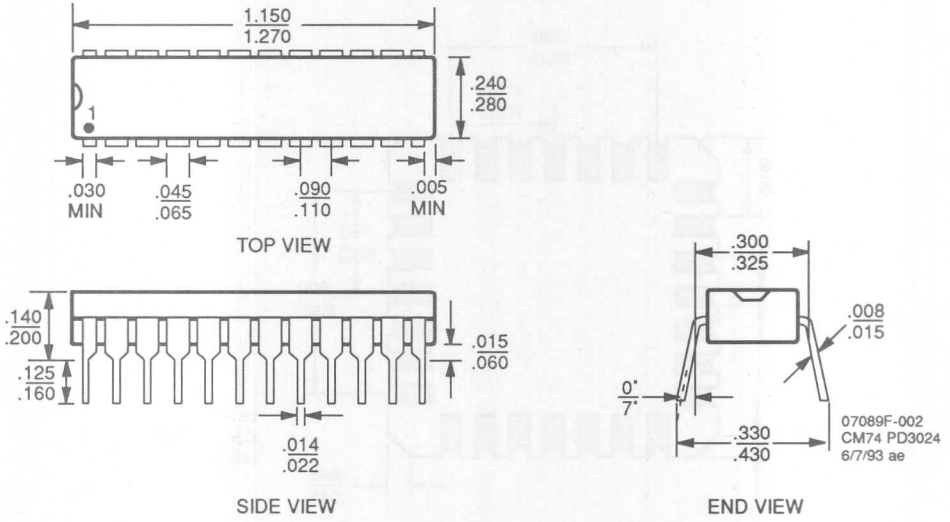
TOP VIEW



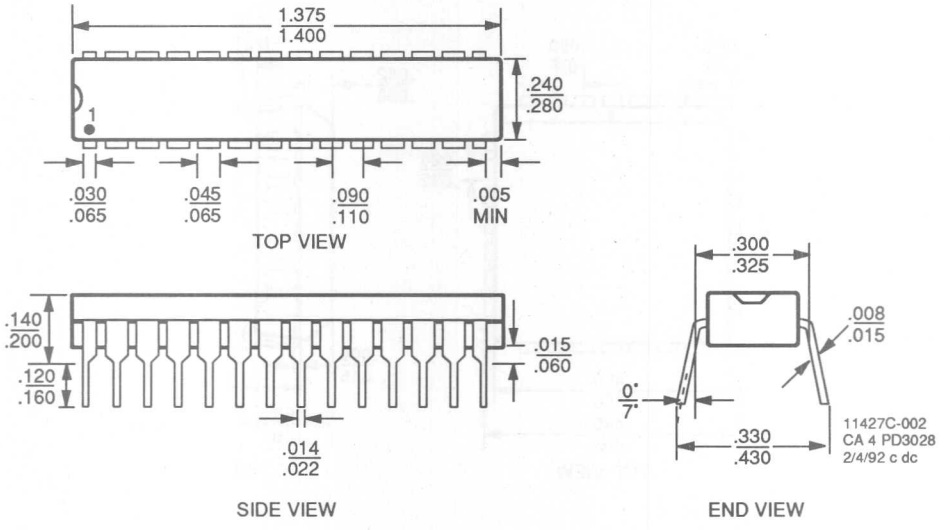
BOTTOM VIEW



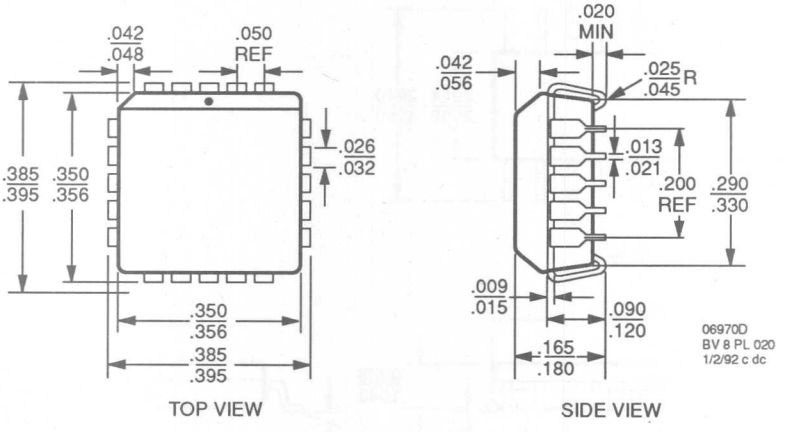
PD3024
24-Pin 300 mil Plastic SKINNYDIP (measured in inches)



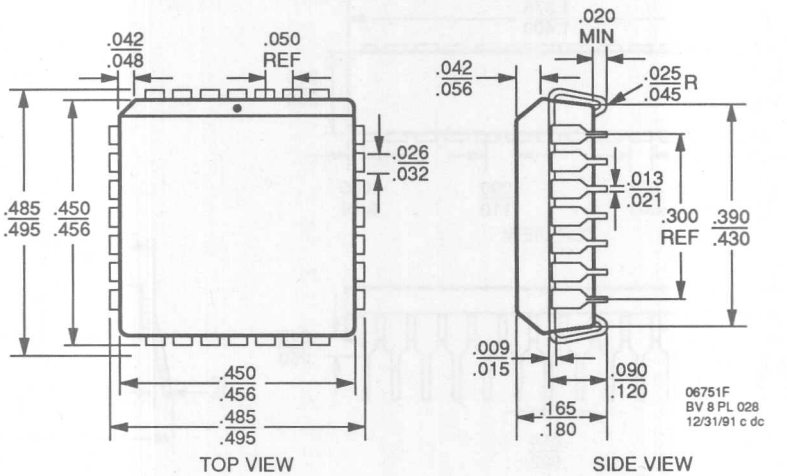
PD3028
28-Pin 300 mil Plastic SKINNYDIP (measured in inches)



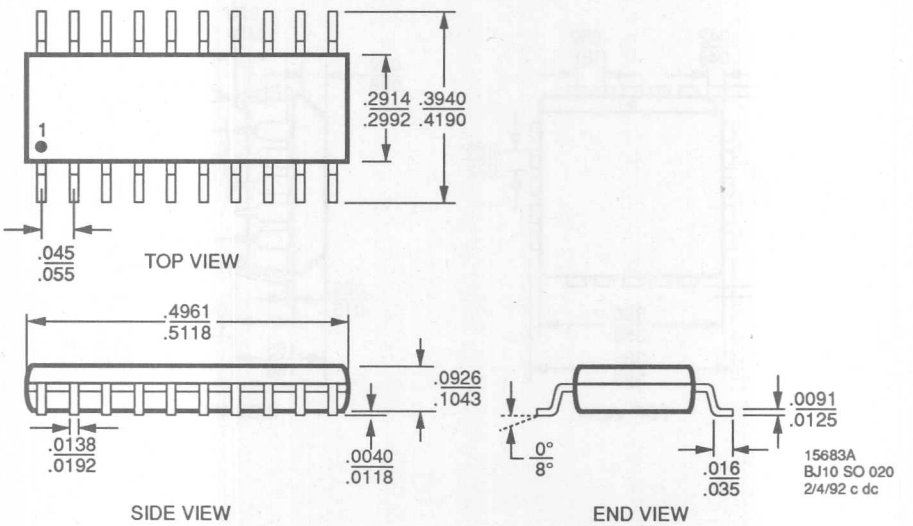
PL 020
20-Pin Plastic Leaded Chip Carrier (measured in inches)



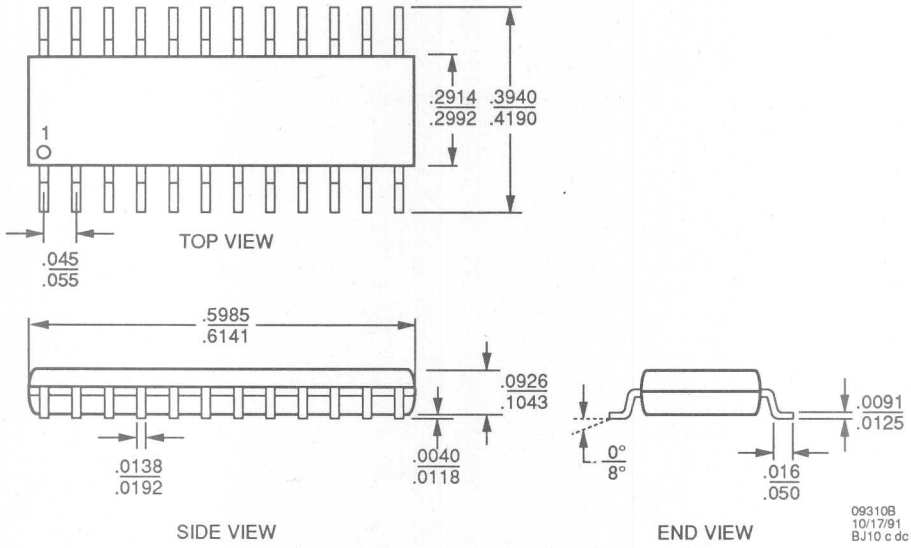
PL 028
28-Pin Plastic Leaded Chip Carrier (measured in inches)



SO 020
20-Pin Plastic Gull-Wing
Small Outline Package (measured in inches)



SO 024
24-Pin Plastic Gull-Wing
Small Outline Package (measured in inches)




IMPORTANT.
NOTES

CHAPTER

5 DESIGN AND TESTABILITY

Basic Design with PLDs 5-3
PLD Design Basics 5-8
PLD Design Methodology 5-16
Combinatorial Logic Design 5-27
Registered Logic Design 5-40
State Machine Design 5-60
Testability 5-73
Ground Bounce 5-92
Metastability 5-95
Latchup 5-97
Converting Bipolar to CMOS 5-100
High-Speed-Board Design Techniques 5-107
Minimizing Power Consumption with Zero-Power PLDs 5-135
Designing with the PALCE16V8HD 5-138


IMPORTANT
NOTES

Basic Design with PLDs

Advanced Micro Devices

INTRODUCTION

The Programmable Array Logic device, commonly known as the PAL device, was invented at Monolithic Memories in 1978. The concept for this revolutionary type of device sprang forth as a simple solution to the short comings of discrete TTL logic.

The successfully proven PROM technology which allowed the end user to "write on silicon" provided the technological basis which made this kind of device not only possible, but very popular as well.

The availability of design software made it much easier to design with programmable logic. As designers were freed from the drudgery of low-level implementation issues, new complex designs were easier to implement, and could be completed more quickly.

This chapter outlines some basic information essential to those who are unfamiliar with Programmable Logic devices (PLDs). The information may also be useful to those who are current users of programmable logic. The specific issues which need to be addressed are:

- What is a PLD?
- What other implementations are possible?
- What advantages do PLDs have over other implementations?

WHAT IS A PLD?

In general, a programmable logic device is a circuit which can be configured by the user to perform a logic function. Most "standard" PLDs consist of an AND array followed by an OR array, either (or both) of which is programmable. Inputs are fed into the AND array, which performs the desired AND functions and generates product terms. The product terms are then fed into the OR array. In the OR array, the outputs of the various product terms are combined to produce the desired outputs.

PAL Devices

The PAL device has a programmable AND array followed by a fixed OR array (Figure 1). The fact that the AND array is programmable makes it possible for the devices to have many inputs. The fact that the OR array is fixed makes the devices small (which means less expensive) and fast.

WHAT OTHER IMPLEMENTATIONS ARE POSSIBLE?

There are essentially four alternatives to programmable logic:

- Discrete Logic
- Gate Arrays
- Standard Cell Circuits
- Full Custom Circuits

Discrete Logic

Discrete logic, or conventional TTL logic, has the advantage of familiarity; hence its popularity. It is also quite inexpensive when only unit cost is considered. The drawback is that the implementation of even a simple portion of a system may require many units of discrete logic. There are "hidden" costs associated with each unit that goes into a system, which can render the overall system more expensive.

Designing with discrete chips can also be very tedious. Each design decision directly affects the layout of the board. Changes are difficult to make. The design is also more difficult to document, making it harder to debug and maintain later. These items all contribute to a long design cycle when discrete chips are used extensively.

Gate Arrays

Gate arrays have been increasing in popularity. The attractiveness of this solution lies in the device's flexibility. By packing the functions into the device, a great majority of the available silicon is actually used. Since such a device is customized for an application, it would seem to be the optimum device for that application.

However, one also pays substantial development costs, especially in the case of a design which needs changes after silicon has already been processed. Even though the unit costs are generally quite low for gate arrays, the volumes required to make their use worthwhile excludes them as a solution for many designers. This fact, added to the long design cycle and high risk involved, make this solution practical for only a limited number of designers.

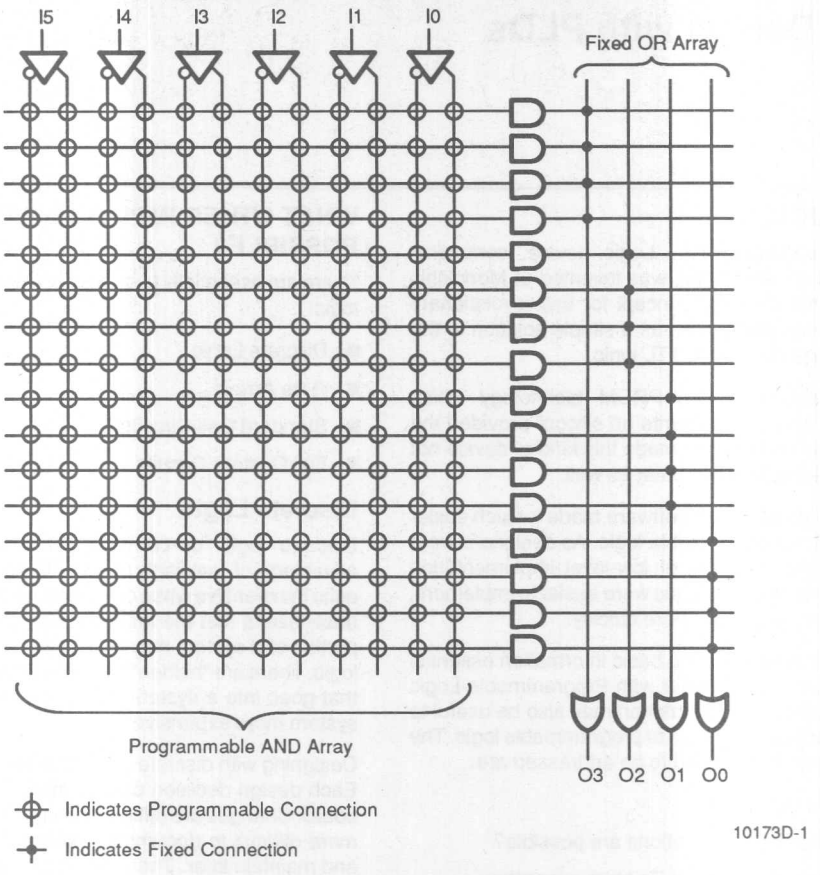


Figure 1. PAL Device Array Structure

Standard Cell Circuits

Standard cell circuits are quite similar to gate arrays, their main advantage being that they consist of a collection of different parts of circuits which have already been debugged. These circuits are then assembled and collected to perform the desired functions. This can ideally lead to reduced turn around from conception to implementation, and a much more efficient circuit.

The drawback is that even though the individual components of the circuit have been laid out, a complete layout must still be performed to arrange the cells. Instead of just customizing the metal interconnections, as is done in a gate array, the circuit must be developed from the bottom up. Development costs can be even higher than for gate arrays, and despite the standard cell concept, turn around time often tends to be longer than planned. Again, the volume must be sufficiently high to warrant the development costs.

Full Custom Circuits

Full custom designs require that a specific chip be designed from scratch to perform the needed functions. The intent is to provide a solution which gives the designer exactly what is needed for the application in question; no more and no less. Ideally, not a square micron of silicon is wasted. This normally results in the smallest piece of silicon possible to fit the needs of the design, which in turn reduces the system cost. Understandably, though, development costs and risks for such a design are extremely high, and volumes must be commensurately high in order for such a solution to be of value.

WHAT ADVANTAGES DO PLDS HAVE OVER OTHER IMPLEMENTATIONS?

As user-programmable semicustom circuits, PLDs provide a valuable compromise which combines many of the benefits of discrete logic with many of the benefits of other semicustom circuits. The overall advantages can be found in several areas:

- Ease of design
- Performance
- Reliability
- Cost savings

Ease of Design

The support tools available for use in designing with PLDs greatly simplify the design process by making the lower-level implementation details transparent. In a matter of one or two hours, a first time PLD user can learn to design with a PAL device, program it, and implement the design in a system.

The design support tools consist of design software and a programmer. The design software is used in generating the design; the programmer is used to configure the device. The software provides the link between the higher-level design and the low-level programming details.

All of the available design software packages perform essentially the same tasks. The design is specified with relatively high-level constructs; the software takes the design and converts it into a form which the programmer uses to configure the PLD. Most software packages provide logic simulation, which allows one to debug the design before actually programming a device. The high-level design file also serves as documentation of the design. This documentation can be even easier to understand than traditional schematics.

Many PLD users do not find it necessary to purchase a programmer; it is often quite cost effective and convenient to have either the manufacturer or an outside distributor do the programming for them. For design and prototyping, though, it is very helpful to have a programmer; this allows one to implement designs immediately.

The convenience of programmable logic lies in the ability to customize a standard, off-the-shelf product. PLDs can be found in stock to suit a wide range of speed and power requirements. The variety of architectures available also allows a choice of the proper functionality for the application at hand. Thus, a design can be implemented using a standard device, with the end result essentially being a custom device. If a design change is needed, it is a simple matter to edit the original design and then program a new device, or, in the case of reprogrammable CMOS devices, erase and reprogram the old device.

Board layout is vastly simplified with the use of programmable logic. PLDs offer great flexibility in the location of inputs and outputs on the device. Since larger functions are implemented inside the PLD, board layout can begin once the inputs and outputs are known. The details of what will actually be inside the PLD can be worked out independently of the layout. In any cases, any needed design changes can be taken care of entirely within the PLD, and will not affect the PC board.

Performance

Speed is one of the main reasons that designers use PAL devices. The PAL devices can provide equal or better performance than the fastest discrete logic available. Today's fastest PAL devices are being developed on the newest technologies to gain every extra nanosecond of performance.

Performance cannot come strictly at the expense of power consumption. Since PLDs can be used to replace several discrete circuits, the power consumption of a PLD may well be less than that of the combined discrete devices. As more PLDs are developed in CMOS technology, the option for even lower power becomes available, including zero standby power devices for systems which can tolerate only minute standby power consumption.

Reliability

Reliability is an area of increasing concern. As systems get larger and more complex, the increase in the amount of circuitry tends to reduce the reliability of the system; there are "more things to go wrong." Thus, a solution which inherently reduces the number of chips in the system will contribute to higher reliability. A programmable logic approach can provide a more reliable solution due to the smaller number of devices required.

With the reduction in units and board space, PC boards can be laid out less densely, which greatly improves the reliability of the board itself. This also reduces crosstalk and other potential sources of noise, making the operation of the system cleaner and more reliable.

Cost

For any design approach to be practical, it must be cost effective. Cost is almost always a factor in considering a new design or a design change. But, the calculation of total system cost can be misleading if not all aspects are considered. Many of the costs can be elusive or difficult to measure. For example, it is difficult to quantify the cost of market share lost due to late product introduction.

The greatest savings over discrete design are derived from the fact that a single PLD can replace several discrete chips. Board space requirements can drop 25% or more when PLDs are used. The relationship between the various alternatives is summarized in Figure 2.

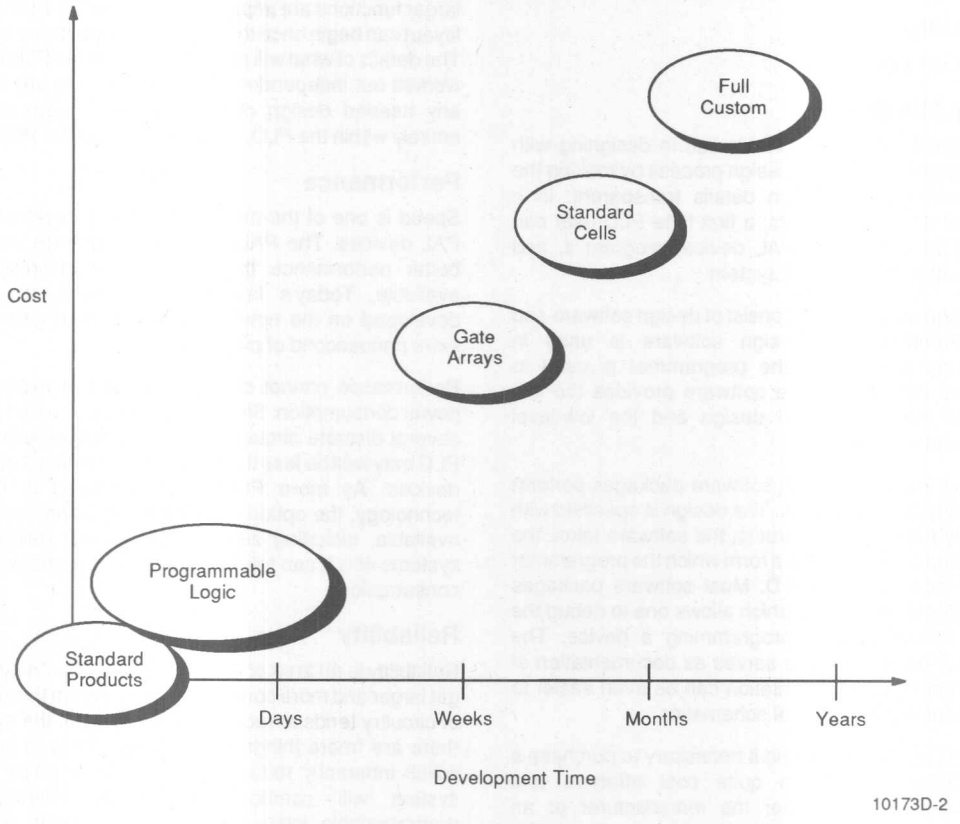


Figure 2. Development Cost vs. Time for Alternative Logic Implementations

Another economic benefit of the use of PLDs is that when one PAL device is used in several different designs, as is often the case, the user has not committed that device to any one of the particular designs until the device has been programmed. This means that inventory can be stocked for several different designs in the form of one device. As requirements change, the parts can be programmed to fit the need. And in the case of reprogrammable CMOS devices, one is not committed even after programming.

One final subtle cost issue is derived from the ease with which a competitor can copy a design. PLDs have a unique feature called a security bit, whose purpose is to protect a design from being copied. By using secured PLDs extensively in a system, one can safely avoid having one's system easily deciphered. The added design security provided by this feature can buy extra market time, forcing competitors to do their own original design work rather that copying the designs of others.

Summary

Programmable logic provides the means of creating semi-custom designs with readily available standard components. There is a wide variety of PLDs; PAL devices are most widely used, and perform well for basic logic and some sequencing functions.

By assuming some of the attributes of gate arrays, programmable logic provides the cost savings of any other semicustom device, without the extra engineering costs, risks, and design delays. Reliability is also enhanced as quality increases and board complexity decreases.

The design tasks are greatly simplified due to the design tools which are now available. Design software and device programmers allow top-down high-level designs with a minimum of time spent on actual implementation issues. Simulation allows some design debug before a device is programmed.

For all of these reasons, programmable logic has become, and will continue to be, the design methodology of choice among digital systems designers.

INTRODUCTION

This section is intended as a beginner's introduction to PLD design, although experienced users may find it a good review. We will take a step-by-step approach through two very simple designs to demonstrate the basic PLD design implementation process. Through this effort, you will be introduced to the concept of device programming.

By "beginner," we mean a logic designer who is just beginning to use programmable logic. You may have a lot of experience with discrete digital logic, or you may have just graduated from college. We assume a basic understanding of digital logic. Some computer experience is helpful, but not essential.

We will take no significant shortcuts for these examples, even though there may be times when we could. In this way, you can gain a better understanding of exactly what is happening as you implement your design.

We will talk about device programming, describing all of the steps that are necessary to program a PLD. However, due to the wide variety of programmers available, we will not get down to the level of detail that tells you exactly which buttons to push. Although we will get as close as we can, we must defer the details to your programmer manual.

Constructing a Combinatorial Design—Basic Gates

The first example we will try is a very simple combinatorial circuit consisting of all of the basic logic gates, as shown in Figure 1. This will be helpful for those designs where you are integrating random logic into a PAL device to save space and money.

As can be seen from the figure, there will be six separate functions involving a total of twelve inputs. It is important to bear in mind that programmable logic provides a convenient means of *implementing* designs. With a real design, some work would be required before this point to conceptualize the design, but due to the simplicity of these circuits, we are already in a position to start the implementation.

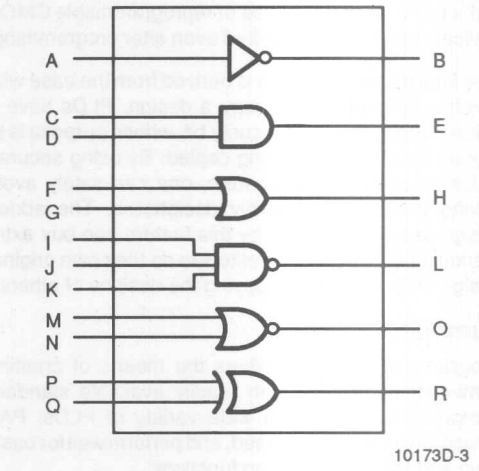


Figure 1. The Basic Logic Gates

Building the Equations

We will start by generating Boolean equations. The first function to be generated is an inverter. This is specified according to Figure 1 as:

```
B = /A
```

Here the "equal" sign (=) is used to assign a function to output B. The slash (/) is used to indicate negation. Thus, this equation may be read:

```
B is TRUE if NOT A is TRUE
```

The next function is a simple AND gate. As shown in Figure 1, we can write:

```
E = C*D
```

Here we use the "equal" sign again, but this time we have introduced the asterisk (*) to indicate the AND operation. This equation may be read:

```
E is TRUE if C AND D are TRUE
```

The third function is an OR gate, which may be written:

```
H = F + G
```

The "plus" sign (+) is used to specify the OR operation here. Because of the sum-of-products nature of logic as implemented in PLDs, it is often easy to place product terms on separate lines, which improves the readability. We may rewrite this equation as:

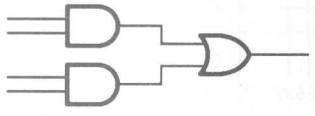
```
H = F
  + G
```

This equation may be read:

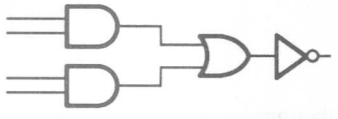
```
H is TRUE if F OR G is TRUE
```

For the moment, we will assume that we have active-HIGH outputs on our device. The functions we have generated so far have essentially been active-HIGH functions. At times we wish to generate active-LOW functions; the next two functions are active-LOW functions that we wish to implement in an active-HIGH device.

When we talk in terms of an active-HIGH or an active-LOW device, the real question is whether there is an extra inverter at the output. An active-HIGH device has an AND-OR structure; an active-LOW device has an AND-OR-INVERT structure which inverts the function at the output (see Figure 2).



a. AND-OR Structure



b. AND-OR-INVERT Structure

10173D-4

Figure 2. Active HIGH vs. Active LOW

NAND and NOR gates could be generated very simply in an active-LOW device, because we would just have to generate AND and OR functions, and let the output inverter generate their complements. However, given that we wish to implement these functions in an active-HIGH device, we must invoke DeMorgan's theorem, as follows:

```
/(X * Y) = /X + /Y
/(X + Y) = /X * /Y
```

We may generate our NAND function by writing:

```
L = / (I * J * K)
```

or, if preferred,

```
L = /I
  + /J
  + /K
```

Likewise the NOR function may be specified as:

```
O = /(M
  +  N)
```

or

```
O = /M * /N
```

Finally, an exclusive-OR (XOR) gate may be specified either as:

```
R = P :+: Q
```

where :+: represents the XOR operation, or more explicitly as:

```
R = P * /Q
  + /P * Q
```

We have now specified all of the functions in terms of their Boolean equations. The equations are summarized in Figure 3.

```
B = /A          ; inverter

E = C * D       ; AND gate

H = F           ; OR gate
  + G

L = /I          ; NAND gate
  + /J
  + /K

O = /M * /N ; NOR gate

R = P * /Q  ; XOR gate
  + /P * Q
```

Figure 3. Basic Gates Equations

A portion of a logic diagram is shown in Figure 4.

The logic diagram shows all of the logic resources available in a particular device. In each device, inputs are provided in true and complement versions, as shown in Figure 4. These drive what are often called "input lines," which are the vertical lines in the logic diagram. These input lines can then be connected to product terms. The name "product term" is really just a fancy name for an AND gate. However, PLDs provide lines with a small AND gate symbol at one end to indicate the function being performed.

Although you really do not need to be concerned with the actual implementation of these functions inside the PAL device, you may be curious. Figure 5 shows how the inverter and the AND gate are implemented. An 'X' indicates a connection. A product term that is not used is indicated by an 'X' in the small AND gate.

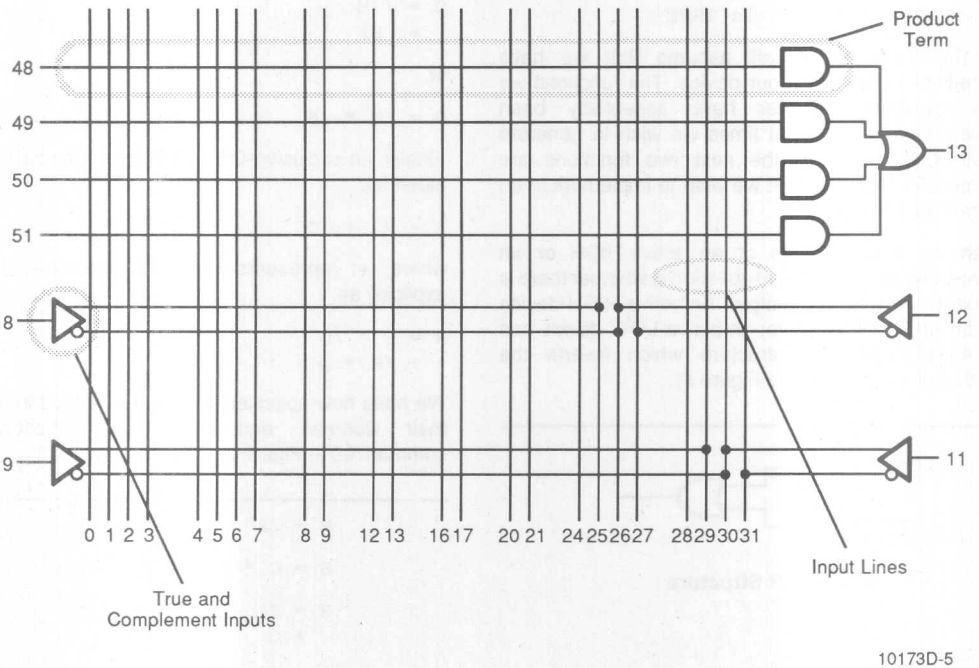
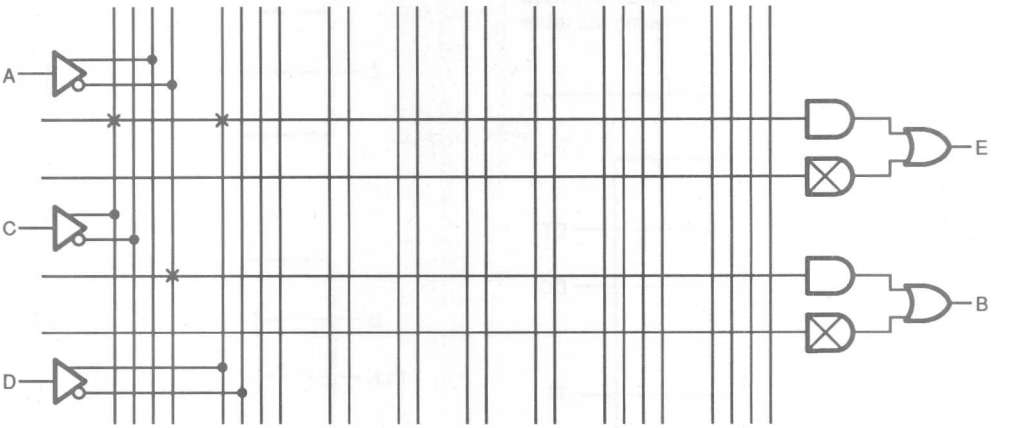


Figure 4. A Portion of a Logic Diagram



10173D-6

Figure 5. Implementation of NOT, AND Gates

Building the Design File

Once the design has been conceptualized, the design file must be generated.

We now know exactly what our functions are going to be. We have twelve inputs, six outputs, and the NAND function requires three product terms. Note that if we had specified:

```
L = / (I * J * K)
```

instead of:

```
L = /I
  + /J
  + /K
```

for the NAND gate, it would not be as obvious how many product terms would be needed.

We are now in a position to create the design file. The design entry varies with the software package used. You must consult the manuals supplied with the software for design entry format.

Generating a JEDEC File

Once the design file has been entered, you can assemble the design to get a JEDEC file. We have two purposes here: to make sure there are no basic mistakes in the file, and to generate a JEDEC file for programming. Again, how this is done is determined by the software.

Simulating the Gates

After you have verified that your design file is correct, it is time to verify that the design itself is correct. This is done by simulating the design. Simulation provides a way for you to see whether your design is working as you expect it to. You provide a series of commands, or events, which are then simulated by the software. If requested, the software can tell you if the simulation matches what you expect, and, if not, where the problems are.

The simulation section is the last part of the design file. It is not required, but is invariably helpful both in debugging the design, and in generating what can eventually be used as a portion of a test vector sequence.

The simulator also converts the simulation results into test vectors, and appends the vectors to the JEDEC file. This file can be used with programmers that provide functional tests.

Constructing a Registered Design—Basic Flip-Flops

Next we will do a very simple registered design: we will be designing all of the basic flip-flop types (Figure 6). We will conceptualize the design by reviewing briefly the behavior of the D-type flip-flop. We will then present the results for T, J-K, and S-R flip-flops.

The devices we will be using in the examples only have D-type flip-flops. Thus, we will be emulating the other flip-flops with D-type flip-flops.

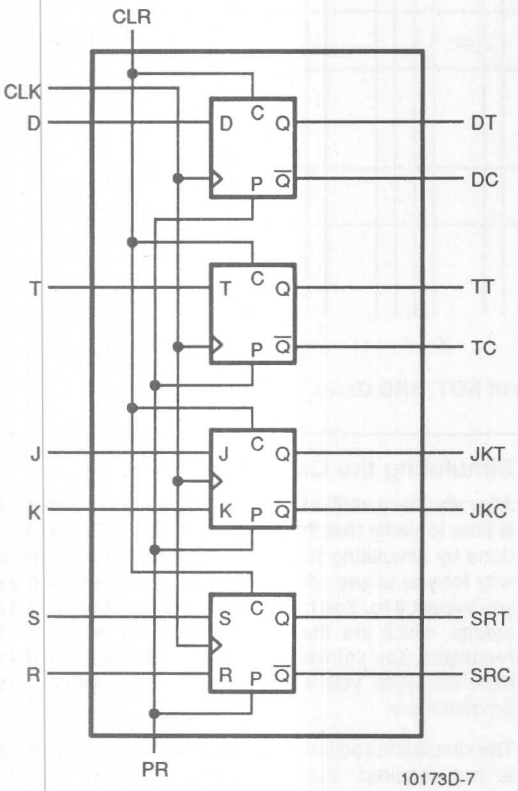


Figure 6. Basic Flip-Flops

Building the D-Type Flip-Flop Equations

A D-type flip-flop merely presents the input data at the output after being clocked. Its basic transfer function can be expressed as:

```
DT : = D
```

where we have used pins DT (D True) and D as shown in Figure 6.

Note the use of ':=' here instead of '='. This indicates that the output is registered for this equation. The difference is illustrated in Figure 7.

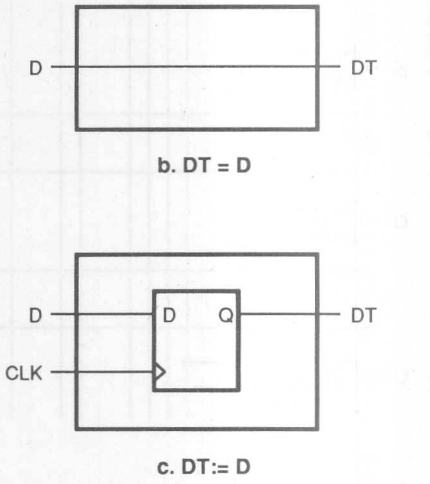


Figure 7. Registered vs. Combinatorial Equations

We can also generate the complement signal (named DC) with the statement:

```
DC : = /D
```

As shown in Figure 6, we want to add synchronous preset and clear functions to the flip-flops. This can be done with two input pins, called PR and CLR. To add these functions to the true flip-flop signal, we add /CLR to every product term and add one product term consisting only of PR. Likewise, for the complement functions, we add /PR to every product term, and add one product term consisting only of CLR. With these changes, the equations now looks like:

```
DT := D * /CLR
    + PR

DC := /D * /PR
    +  CLR
```

In this way, when clearing the flip-flops, the active-HIGH flip-flops have no product terms true, and go LOW; the active-LOW flip-flops have the last product term true, and will therefore go HIGH. The reverse will occur for the preset function.

There is still one hole in this design: what happens if we preset and clear at the same time? As it is right now, both outputs will go HIGH. This makes no sense since one signal is supposed to be the inverse of the other. To rectify this, we can give the clear function priority over the preset function. We can do this by placing /CLR on every product term for the true flip-flop signal. The results are shown as follows:

```
DT := D * /CLR
    + PR * /CLR

DC := /D * /PR
    + CLR
```

The same basic procedure can be applied to all of the other flip-flops. The equations are shown in Figure 8.

```
EQUATIONS

;emulating all flip-flops with D-type flip-flops

DT := D * /CLR              ;output is D if not clear
   + PR * /CLR              ;or 1 if preset and not clear at the same time

DC := /D * /PR              ;output is /D if not preset
   + CLR                    ;or 1 if clear

TT := T * /TT * /CLR        ;go HI if toggle and not clear
   + /T * TT * /CLR         ;stay HI if not toggle and not clear
   + PR * /CLR              ;go HI if preset and not clear at the same time

TC := T * /TC * /PR         ;go HI if toggle and not preset
   + /T * TC * /PR          ;stay HI if not toggle and not preset
   + CLR                    go HI if clearing

JKT:= J * /JKT * /CLR       ;go HI if J and not clear
   + /K * JKT * /CLR        ;stay HI if not K and not clear
   + PR * /CLR              ;go HI if preset and not clear at the same time

JKC:= /J * /JXC * /PR       ;go HI if not J and not preset
   + K * /JKC * /PR         ;stay HI if not K and not preset
   + CLR                    ;go HI if clear

SRT:= S * /CLR              ;go HI if set and not clear
   + /R * SRT * /CLR        ;stay HI if not reset and not clear
   + PR * /CLR              ;go HI if preset and not clear at the same time

SRC:= R * /PR               ;go HI if reset and not preset
   + /S * SRC * /PR         ;stay HI if not set and not preset
   + CLR                    ;go HI if clear
```

Figure 8. Flip-Flop Equation Section

Building the Remaining Equations and Completing the Design File

Notice that in some of the equations above, the output signal itself shows up in the equations. This is the way in which feedback from the flip-flop can be used to determine the next state of the flip-flop. An equivalent logic drawing of the TT equation is shown in Figure 9.

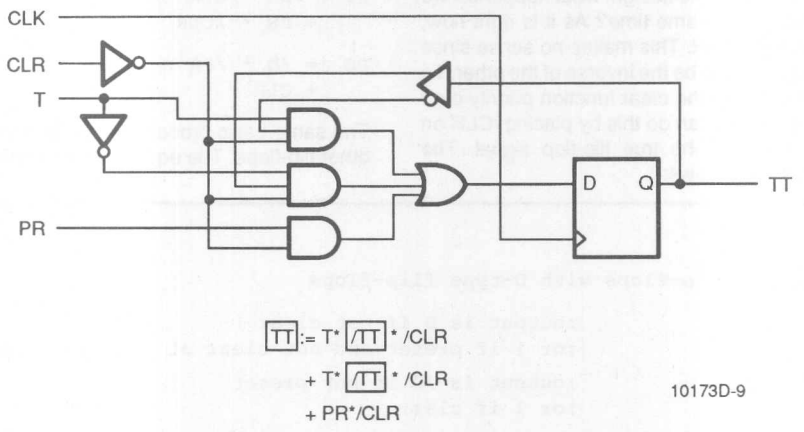


Figure 9. Feedback in the Equation for TT

We are now in a position to complete the design file. You must follow the instructions included with your software package to complete the file.

Simulating the Flip-Flops

After processing the design and correcting any mistakes, we can run the simulation.

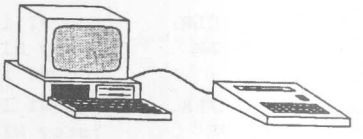
The file can now be simulated in the same manner as the basic gates design.

Programming a Device

After simulating the design, and verifying that it works, it is time to program a device. There are several steps to programming, but the exact operation of the programmer naturally depends on the type of programmer being used. We will be as explicit as we can here, but you will need to refer to your programmer manual for the specifics.

The first thing that must be done after turning the programmer on is to select the device type. This tells the programmer what kind of programming data to expect. The device type is usually selected either from a menu or by entering a device code. Your programmer manual will have the details.

Next a JEDEC file must be downloaded. To transfer the JEDEC file from the computer to your programmer, you will need to provide a connection, as shown in Figure 10.



10173D-10

Figure 10. A Connector Must Be Provided Between the Computer and the Programmer

If your programmer can perform functional tests, and you wish for those tests to be performed, you should download the JEDEC file containing the vectors; otherwise, you should download the JEDEC file without vectors.

To download data, the programmer must first be set up to receive data. The programmer manual will tell you how to do this.

Communication must be set up between the computer and the programmer. Whichever communication program is installed must be invoked. This is used to transmit the JEDEC file to the programmer. Follow the instructions for your program to accomplish the next steps.

Before actually sending the data, you must verify the correct communication protocol. Check to make sure you know what protocol the programmer is expecting; then set up the baud rate, data bits, stop bits, and parity, to match the protocol.

Once the protocol has been set up the JEDEC file must be downloaded.

Enter the name of the JEDEC file you wish to use. The computer will then announce that it is sending the data, and tell you when it is finished. Note that just because it says it has finished sending data does not mean that the data was received. Your programmer will indicate whether or not data was received correctly.

Once the data has been received, the programmer is ready to program a device. Place a device in the appropriate socket, and follow the instructions for your programmer to program the device. This procedure programs and verifies the connections in the device, and, if a JEDEC file containing vectors was used, will perform a functional test.

The programmer will announce when the programming procedure has been completed. You may then take the device and plug it into your application.

If you have actually programmed one of the examples that we created above, you naturally don't have a board into which you can plug the device. If you do have a lab setup, you may wish to play with the devices to verify for yourself that the devices perform just as you expected them to.

You will find much more detail on many issues that were not discussed in this section in the remaining sections of this handbook. This section should have provided you with the basic knowledge you need to understand the remaining design examples in this book, and to start your own designs.

PLD Design Methodology

Programmable logic devices (PLDs) are used in digital systems design for implementing a wide variety of logic functions. These logic functions range from simple random logic replacement to complex control sequencers. Programmable logic devices offer the multiple advantages of low cost, high integration, ease of use, and easier design debugging capability not available in other systems design options. In the following discussion we will detail the PLD design process.

Most PLDs have an AND-OR array structure with programmable connections in either or both of the arrays. A programmable array implies that the connections can be programmed by the user. The popular PAL (Programmable Array Logic) devices have a programmable AND array and a fixed OR array. PAL devices are used for a wide variety of combinatorial and registered logic functions. In this discussion we will also examine the various design constraints to be considered when selecting the correct architecture for a given application.

All digital logic can be efficiently reduced to two fundamental gates, AND and OR, provided both true and complement versions of all input signals are available. Such logic is generally built around what is known as the sum-of-products (AND-OR) form. Programmable logic devices are ideal for implementing such two-stage logic in the AND and OR arrays.

Various process technologies offer many design options for PLDs. The connections in the programmable arrays can be fuse-based, commonly used in both ECL and TTL bipolar technologies, E/EEPROM cell based in UV-EPROM and EEPROM CMOS technologies, and RAM cell-based in CMOS RAM technology. The selection of technology is mostly dependent upon the system speed and power constraints. Most design engineers are familiar with these constraints, which not only dictate the technology of PLDs but also all of the other logic used in a system.

Designing with PLDs involves the use of design software and a device programmer (Figure 1). The design software eliminates the need to identify every connection to be programmed for implementing the desired sum-of-products logic. The design process begins with the creation of a design file which specifies the desired function. The function is typically represented by its sum-of-products form and can be derived directly from the timing diagram and/or truth tables. Occasionally Karnaugh maps and state diagrams are also used. The design file is then assembled to produce the "JEDEC" file. The JEDEC file gets its name from the fact that it is an approved JEDEC standard for specifying the state of every connection on the device. Simulation can then be performed. If the design is correct, the JEDEC file is downloaded into a device programmer for programming the connections on the device. The device can then be plugged into the PC board where it will function. The entire procedure can often be performed with the designer never having to leave the desk. Most programmers interface to personal computers, so that the design file can be edited, assembled, simulated, and downloaded, and the device programmed, all in one place.

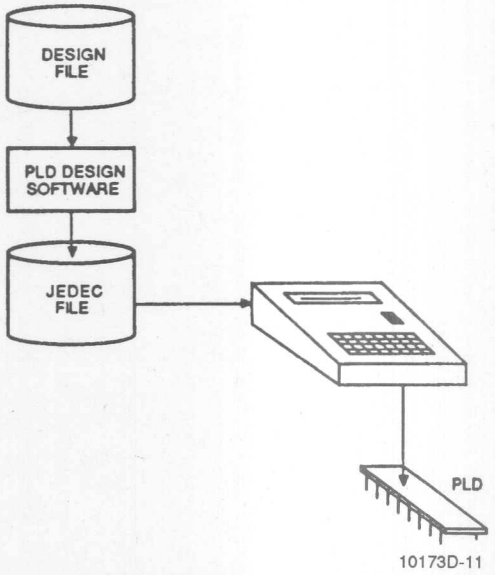
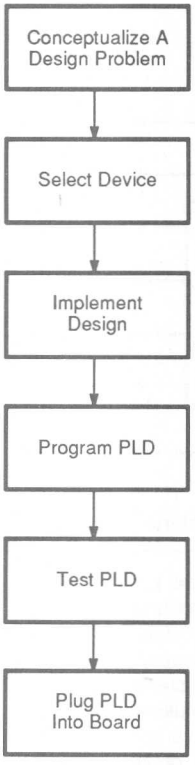


Figure 1. PLDs are Designed Using Software and a Device Programmer

The first stage in a PLD design process (Figure 2) is the conceptualization of a design problem; the second is the selection of the correct device; the third is the implementation of the design, which also includes simulating the design with test vectors; and finally, the

actual programming and testing on a system board. We will take a simple design example and go through the various stages of this design process.



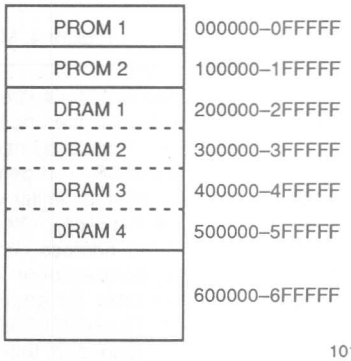
10173D-12

Figure 2. Programmable Logic Device Design Process

Conceptualizing a Design

The first step in the PLD design process is also required for any SSI/MSI design. An advantage of PLDs is that at this stage the designer needs to be concerned only with the required logic function. With SSI or MSI, various device logic limitations must be accounted for before the design can be started. Clearly a designer needs to develop a brief and complete functional description, based upon the system design requirements.

We will take the example of a simple address decoder circuit required for a 68000 microprocessor. The microprocessor has 24 address lines along with separate read and write signals. It requires some ROM to store the boot-up code as well as some RAM for storing and executing programs. The purpose of the address decoder circuitry is to select one of the memory addresses at a time. The RAMs and ROMs are assigned addresses on the 68000 microprocessor address space. The Address decoder circuit has to select one of the RAMs or ROMs for a specific range of addresses, called the address space. This selection is accomplished by asserting the specific chip-select signal for the RAM or ROM when the microprocessor accesses one of the addresses in the address space. There is additional circuitry in a typical microprocessor system for addressing I/O devices (such as disk controllers). These devices also require that chip-select signals be asserted when the microprocessor addresses them. Figure 3 shows an example address map for a 68000 microprocessor.



10173D-13

Figure 3. Memory Address Map

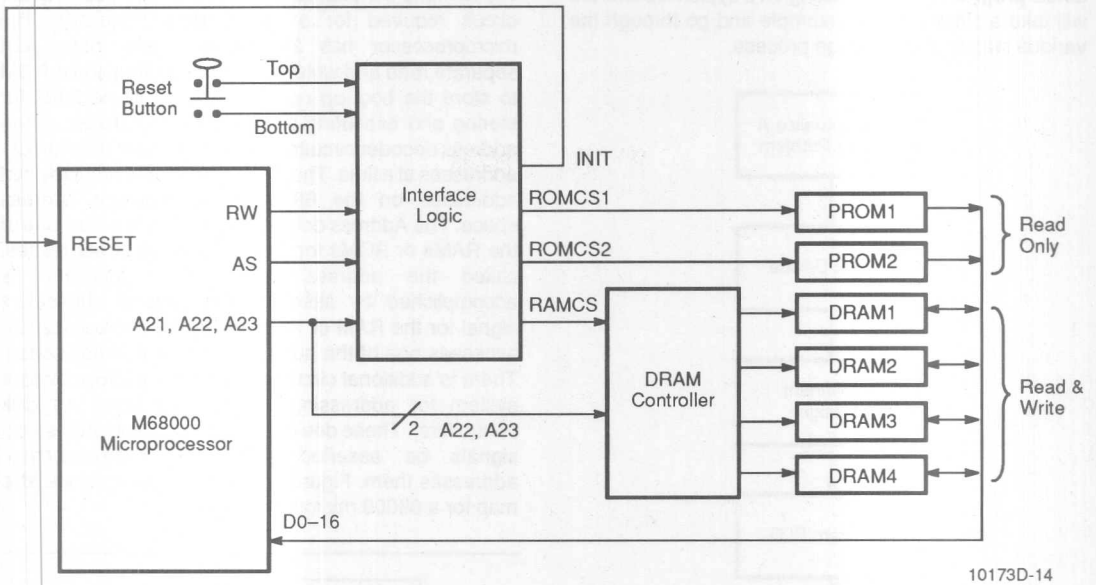


Figure 4. Microprocessor to Memory Interface

Figure 4 show the circuit diagram. The address signals from the 68000 microprocessor are inputs to the interface logic block. The outputs generated are ROMCS1, ROMCS2 and RAMCS. The generation of signals for selecting device I/Os is similar and is not shown here for the sake of simplicity. Other system inputs to the interface are the address strobe signal generated by the 68000 microprocessor as well as the read/write signal. The truth table for generating the outputs is shown in Table 1. This truth table is derived from the memory address map and the functional description of the design.

Table 1. Truth Table for Chip-Select Signals

Addresses Hex	Size	A23	A22	A21	Signal
000000–0FFFFF	1 MB	0	0	0	$\overline{\text{ROMCS1}}$
100000–1FFFFF	1 MB	0	0	1	$\overline{\text{ROMCS2}}$
200000–2FFFFF	1 MB	0	1	0	$\overline{\text{RAMCS}}$
300000–3FFFFF	1 MB	0	1	1	$\overline{\text{RAMCS}}$
400000–4FFFFF	1 MB	1	0	0	$\overline{\text{RAMCS}}$
500000–5FFFFF	1 MB	1	0	1	$\overline{\text{RAMCS}}$

Device Selection Considerations

The first task for the designer is to identify the design problem and classify it as a combinatorial function or a registered function, depending upon whether or not registers are required. In most cases, this decision depends upon the functional nature of the problem. Sometimes timing and logic considerations can also dictate the use of registers; this will be discussed later. Registers are usually not required for such simple combinatorial functions such as encoders, decoders, multiplexers, demultiplexers, adders, and comparators. However, registers are required for functions such as counters, timers, control signal generation, and state machines. No registers are required for this simple address decoding example.

The best choice for our combinatorial design would be a PAL device. The task now is to select a PAL device for implementing the desired function. General device selection considerations are listed below. These items are applicable to most designs.

- Number of input pins
- Number of output pins
- Number of I/O pins
- Device speed
- Device power requirements
- Number of registers (if any)
- Number of product terms
- Output polarity control

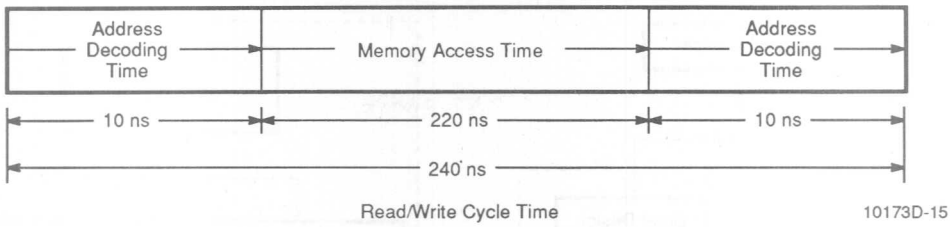


Figure 5. System Timing Requirements

The first resource that must be provided in a PLD is the number of pins needed for the basic logic function. This consists of the number of input and output pins. Many PLDs have internal feedback, which allows the generated output signal to be reused as an input. The same feedback also allows the pin to be used as a dedicated input, if required. This is especially useful for fitting various designs with different input/output requirements on the same device. The I/O pin capability of certain PLDs can also be very useful for certain bus applications.

The task is as simple as counting the number of input, output and I/O pins required by the design and picking a PLD which has the requisite number of pins.

The next selection issue is the device speed. The most important timing consideration for combinatorial PLDs is the propagation delay (t_{PD}) of signals from the input to the output of the device. For registered PLDs, the important timing consideration is the device clocking frequency. This clocking frequency is in turn determined by sum of the register setup time (t_S), and clock-to-output propagation delay (t_{CO}). Most systems impose some timing restrictions on the internal logic functions. These restrictions will determine the necessary t_{PD} (for combinatorial devices) or f_{MAX} (for registered devices).

In our design example, the PLD will primarily perform address decoding. The critical system timing constraint is determined by the read/write cycle time of the microprocessor and the memory access time available (Figure 5). Most microprocessors allow anywhere from 10 to 35 ns for address decoding. That is, 10 ns – 35 ns after the address is available, the correct memory chip-select signal should be asserted. In our design example, the available cycle time of 240 ns and memory access time of 220 ns leaves barely 10 ns for address decode time. We can check the propagation delay and select the appropriate speed device for our design, which is t_{PD} = 10 ns.

We have already briefly discussed the types of applications where registers are needed. Sometimes the consideration of system timing can affect whether or not registers are needed. Devices with registers can hold a signal stable for the long durations required by the addressed peripheral or memory. However, this slows the initial response or access time of the device since the chip select must wait for the setup time before the rising edge of the clock cycle. Devices without registers provide fast access time but hold the signal valid only as long as the input conditions are valid. In most address decoders, the address signals are kept asserted by the microprocessor until the read/write cycle is completed. In this case, the registers are not required for holding the signals asserted.

The remaining two general design considerations are the number of product terms and output polarity. We will discuss these two as we implement the design in the next section.

Implementing a Design

Implementing a design (Figure 6) requires the creation of a design file. The design file contains three types of information.

- Basic bookkeeping information
- Design syntax
- Simulation syntax

Once the design file is complete, it is then assembled and simulated. Once it passes assembly and simulation, the resultant JEDEC file is downloaded to a device programmer for configuring the device.

Design Syntax

In this example, as shown in Figure 6, there are two options available to the designer for expressing the design. The first is through traditional Boolean logic equations; the second is through a state machine syntax. The Boolean logic equations are the only option for combinatorial designs and can also be efficient for some registered designs. The Boolean equations can be derived from a combination of the functional description, the truth table and/or the timing diagrams (Figure 7). The state machine approach is ideal for large registered control designs, and can be derived from the functional description, state table, state diagram and/or the timing diagram (Figure 8).

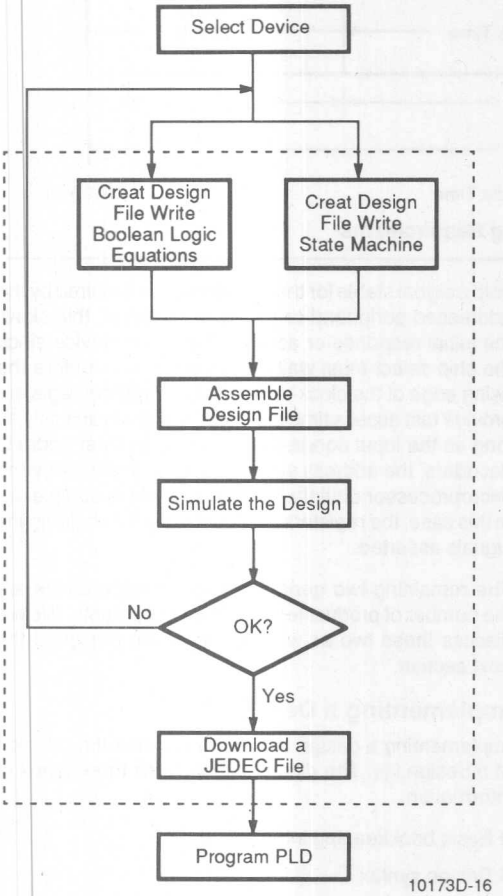


Figure 6. Implementing a Design

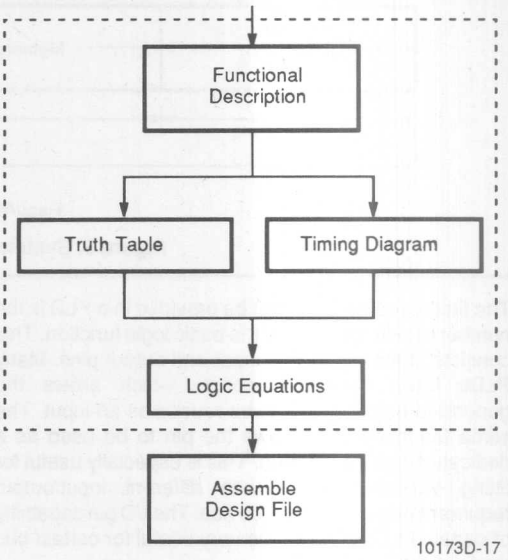


Figure 7. Writing Boolean Logic Equations

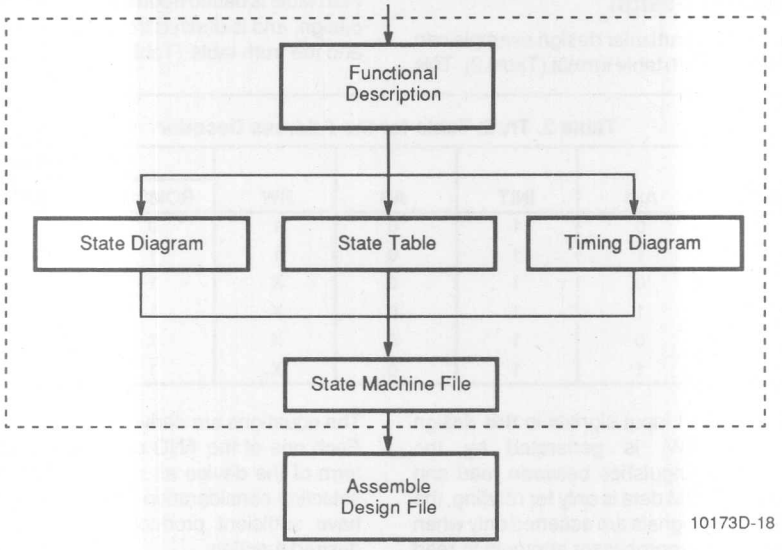


Figure 8. State Machine Description

Boolean Logic Equations

Boolean equations are used to represent the sum-of-products logic form. The Boolean equations are ideally suited for representing the two-level AND-OR logic available in most PLDs.

A conventional approach to the design is to convert the design problem to its discrete logic implementation. Such random SSI and MSI logic can be easily implemented in PLDs. This usually involves converting to sum-of-products Boolean logic form. This approach can be a chore, and much effort can be saved by implementing a design with PLDs in a sum-of-products form right from the start. This essentially means that the designer does not have to design around the limitations of fixed SSI and MSI functions. A direct implementation of a design in sum-of-products form in a PLD can also yield a faster circuit.

Boolean equations can be directly derived from the truth table or timing diagram (Figure 7). The truth table is used more often in simple combinatorial designs. The timing diagram method is used more often in registered control designs. We will first discuss the truth table method and then discuss the details of the timing diagram method.

In addition to specifying the logic function, the Boolean equations in the design file help document the design. There is no need to draw out an equivalent schematic. This allows design modularity; the schematic can just show a block for a particular PLD. Separate supporting documentation (the design file) provides the details without cluttering the drawing.

Truth-Table-Based Design

The requirements for our particular design example can be easily converted to a truth table format (Table 2). This truth table is based upon the functional description of the design, and is derived from the address map (Figure 3) and the truth table (Table 1).

Table 2. Truth Table for the Address Decoder

						Output Generated		
A23	A22	A21	INIT	AS	RW	ROMCS1	ROMCS2	RAMCS
0	0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	X	1	1	0
0	1	1	1	0	X	1	1	0
1	0	0	1	0	X	1	1	0
1	0	1	1	0	X	1	1	0

There are three additional input signals in this design example. The first, RW, is generated by the microprocessor, and distinguishes between read and write cycles. Since the ROM data is only for reading, the ROMCS1 and ROMCS2 signals are asserted only when RW is high (when the microprocessor attempts to read the ROM) and are not asserted for the write cycle. On the other hand, RAMCS is generated for both read and write cycles and the state of signal RW is "don't care."

The second additional signal, AS, is the address strobe signal generated by the microprocessor, and is asserted only when the address lines carry a valid address. All of the chip select signals need to be gated with the AS signal to ensure that they are only generated for valid addresses, and no spurious chip selects are generated.

The last signal is the INIT signal, which is a system initialization signal. This signal is used to initialize the microprocessor for a "warm boot," and none of the chip selects is allowed when this INIT signal is asserted.

Writing Boolean equations from the above logic is very straight forward. The output signal names, along with their polarity, are assigned to sum-of-product equations, which are based upon inputs and their polarities.

```
/ROMCS1 = /A23 * /A22 * /A21 * INIT * /AS * RW
/ROMCS2 = /A23 * /A22 *  A21 * INIT * /AS * RW
/RAMCS  = /A23 *  A22 * /A21 * INIT * /AS
        + /A23 *  A22 *  A21 * INIT * /AS
        +  A23 * /A22 * /A21 * INIT * /AS
        +  A23 * /A22 *  A21 * INIT * /AS
```

Figure 9. The Implementation In Boolean Equations

The equations are derived directly from the truth tables. Each one of the AND equations uses up one product term of the device as shown in Figure 9. One device selection consideration is to ensure that all the outputs have sufficient product terms to accommodate the desired function.

This brings us to the issue of output polarity. Suppose we had to generate active-HIGH outputs. In that case the output equations for the ROMCS1 signal would be:

```
ROMCS1 = /A23 + /A22 * /A21 * INIT */AS * RW
```

If the device has active-LOW outputs only, this equation's output polarity needs to be inverted to be able to fit the device. Using DeMorgan's theorem for Boolean logic we get:

```
/RCMCS1 = A23 + A22 + A21 + /INIT + AS + /RW
```

This equation requires a large number of product terms (six). Some signals are efficient and use fewer product terms in their true form, while others are more efficient in their inverted form. The device selection issues of product terms and output polarity also apply to registered designs.

Timing-Diagram-Based Design

Until now, we have discussed a PLD design using truth tables as the primary design vehicle. In this section we will attempt a design using a timing diagram as a design vehicle.

Earlier in the address decoder design we mentioned the INIT signal. This INIT signal essentially an initialization signal for the entire system. The INIT signal is used internally (via feedback) for disabling the chip selects during initialization. Externally it can be used to initialize

other system signals. This INIT signal is generated from a RESET switch connected to the inputs of the device as shown in Figure 10.

Most experienced designers understand the tradeoffs for device selection. They implicitly go through the steps of design conceptualization and device selection, explained earlier. They typically draw a block around the logic being designed, with the previous knowledge that it would fit a PLD which has sufficient inputs, outputs, IOs and product terms.

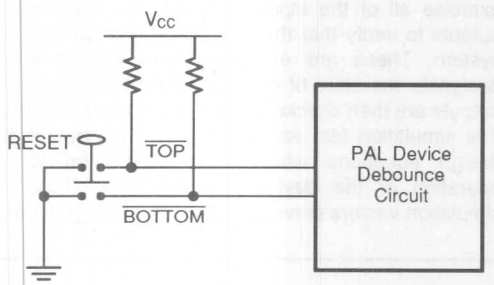


Figure 10. RESET Switch for System Initialization

To avoid unwanted initialization, the RESET switch must be debounced. That is, we want the INIT signal to remain HIGH until the switch actually contacts the bottom side. Once the bottom side is hit, INIT should be asserted active LOW. Once asserted, it should stay LOW and not change until the top side is hit again. The timing requirements of the debounce circuitry are shown in Figure 11. Signals TOP and BOTTOM are inputs to the programmable logic device. These signals are activated when the RESET switch touches the top and the bottom contacts, respectively.

We can formulate the equations by looking at the timing requirements of the debounce circuitry shown in Figure 11. The idea is to identify the key elements of this timing diagram. The arrows in Figure 11 show the critical events. The first arrow shows the normal state of all the pins when the RESET switch is not asserted. Subsequent arrows show each event in the timing of the INIT signal, depending upon the movement of the switch.

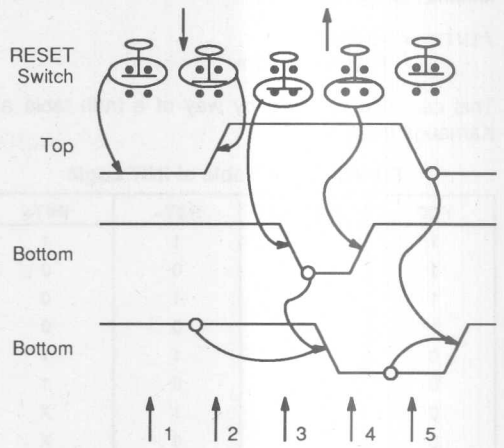


Figure 11. Timing Diagram for the Debounce Switch

The logic level of the signals at each critical event carries useful logic information for deriving Boolean equations. This logic information for each event is converted into direct Boolean equations as shown in below. For example, at instant 1 the INIT signal remains HIGH as long as the TOP signal remains LOW; this is converted to INIT = /TOP * BOTTOM.

1. Normal state — `INIT = /TOP`
2. Switch travels from TOP to BOTTOM — `INIT = TOP * BOTTOM * INIT`
3. Switch contacts BOTTOM — `/INIT = /BOTTOM`
4. Switch travels from BOTTOM to TOP — `/INIT = /INIT * BOTTOM * TOP`
5. Normal State Again

We can combine the two active-LOW events into one equation:

```
/INIT = /BOTTOM
      + /INIT * BOTTOM * TOP
```

Minimizing, this becomes:

```
/INIT = /BOTTOM
      + / INIT * TOP
```

This can also be done by way of a truth table and Karnaugh map.

Table 3. Truth Table of INIT Logic

TOP	BOTTOM	INIT–	INIT+
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	1
0	1	0	1
0	0	1	X
0	0	0	X

Here TOP or BOTTOM will be LOW if contacted. Note that both TOP and BOTTOM can not be contacted at the same time. The truth table of Table 3 yields the Karnaugh map shown in Figure 12. Grouping the zeros (because we are using active-LOW outputs) yields the Boolean equation identical to the one derived from the timing diagram.

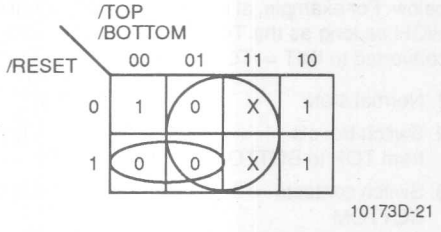


Figure 12. Karnaugh Map of INIT Signal Logic

There is essentially no difference between the truth table and timing diagram techniques for writing Boolean logic. Also, a careful analysis will indicate that we implicitly assumed a truth table in the timing diagram example. Some designers prefer to make a separate truth table (at least in the first few PLD designs), while others prefer to design directly from timing diagrams. While the truth table method allows a more optimal utilization of product terms, the timing diagram method is easier to visualize as it retains the design perspective. In both cases the logic should be minimized by the design software to ensure that the design is testable.

Most experienced designers understand the tradeoffs for device selection. They implicitly go through the steps of design conceptualization and device selection, explained earlier. They typically draw a block around the logic being designed, with the previous knowledge that it would fit a PLD which has sufficient inputs, outputs, IOs and product terms.

Simulation

Design simulation is an integral part of the design process, as shown in Figure 13. The purpose is to exercise all of the inputs and test the response of outputs to verify that they will work as desired in the system. These are essentially test vectors which designate the state of every input on the device; the outputs are then checked for an appropriate response. The simulation test vectors identify any flaws in the design equations which could affect the logical operation of the devices programmed. Thus, the simulation vectors serve as a design debugging tool.

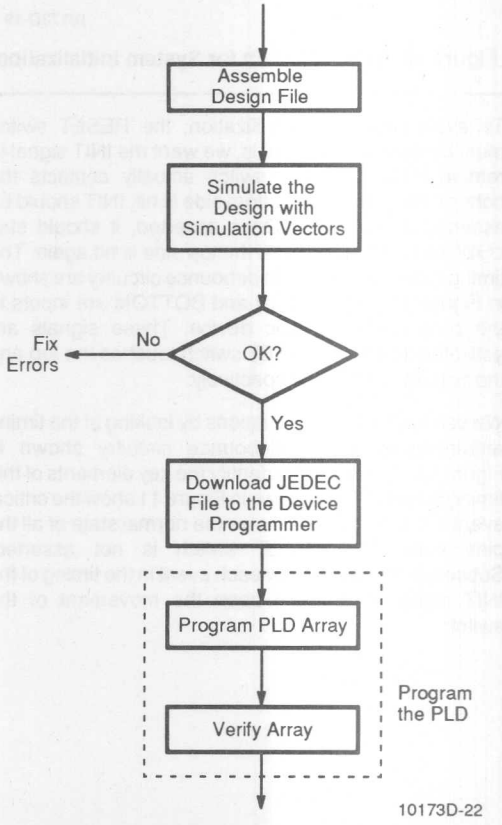


Figure 13. Device Simulation and Programming

Simulation test vectors will eventually make up part of a larger set of test vectors called "functional test vectors". These functional test vectors are used to exercise a real device after programming to identify any individual devices which are defective. Other means of identifying defective devices, such as signature analysis, are also available. In this section we will strictly focus on simulation vectors.

Simulation is included in the design file along with the logic equations. There is little standardization in these simulation expressions among various PLD design software packages, although most of them rely on test vectors to exercise the logic.

The simulation vectors or events can be directly derived from the truth table and the timing diagram of the design. The logic level and functions of all signals can be expanded and rewritten in a test vector form by the software. For example, the truth table for the address decoder example discussed earlier can be easily rewritten as shown in Table 4.

Table 4. Truth Table Used to Derive Simulation Vectors

A23	A22	A21	TOP	BOTTOM	AS	RW	ROMCS1	ROMCS2	RAMCS	INIT
0	0	0	0	1	1	1	H	H	H	H
0	0	0	0	1	0	1	L	H	H	H
0	0	1	0	1	1	1	H	H	H	H
0	0	1	0	1	0	1	H	L	H	H
0	1	0	0	1	1	X	H	H	H	H
0	1	0	0	1	0	X	H	H	L	H
0	1	1	0	1	1	X	H	H	H	H
0	1	1	0	1	0	X	H	H	L	H
1	0	0	0	1	1	X	H	H	H	H
1	0	0	0	1	0	X	H	H	L	H
1	0	1	0	1	1	X	H	H	H	H
1	0	1	0	1	0	X	H	H	L	H
1	0	1	0	1	X	X	H	H	H	H
1	0	1	1	1	X	X	H	H	H	H
1	0	1	1	0	1	X	H	H	H	L
1	0	1	1	1	1	X	H	H	H	L
1	0	1	0	1	1	X	H	H	H	H

These are essentially the simulation vectors which will allow us to define the inputs to the device and check the outputs of the device.

The simulator then interprets the design file and generates the output logic levels and/or waveforms, which can be checked by the designer.

Once the simulation is complete, the design file can be assembled to generate the JEDEC file. In the proceeding discussions we have assumed prior knowledge of the design file assembly. The procedure for assembly varies with different software packages.

Device Programming and Testing

Once the design simulation is completed, the final step is device programming and testing (Figure 14). Programmers are available from a variety of vendors. It is important to note that Advanced Micro Devices, Inc., qualifies programmers upon verifying that the algorithms used by the programmers are correct and that other basic criteria are met. When purchasing a programmer, check that the programmer is qualified for the devices you intend to use.

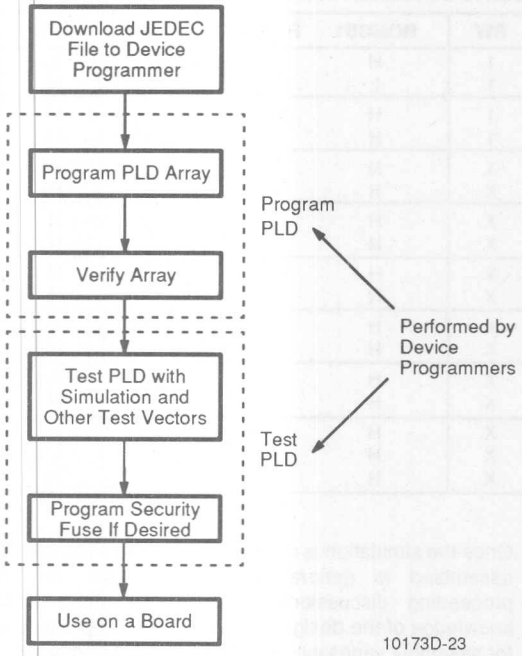


Figure 14. Device Programming and Testing

There are two types of programmers available: menu-driven or device code based. The menu-driven programmer directly indicates the part type being programmed, whereas the latter type requires the user to enter the device code before programming.

Once the JEDEC fuse file has been downloaded, the programmer can program the device; the PLD is then ready for use. The programmer also verifies the connections after the programming cycle. Programmers also provide the capability of reading a previously programmed device and creating duplicates of that device.

Testing PLDs

The testing of PLDs can be performed by the device programmer or by other test equipment. For a manufacturing environment, where high yields are required, device testing is critical. After testing is complete, the device security bit may be programmed, if desired, to secure the design from copying.

INTRODUCTION

In this section we will take a detailed look at several aspects of combinatorial logic design. Most combinatorial design applications can be easily segmented into five major fields.

- Encoders and Decoders
- Multiplexers
- Comparators
- Adders and Arithmetic Logic
- Latches

We will not only focus on the design methodology for these functions, but will also explore further function-specific PLD selection requirements. Generalized designs will be developed, which can be customized later to suit specific system applications. Ways of optimizing the design will also be discussed.

Encoders and Decoders

Two of the most important functions required in digital design are encoding and decoding. The encoding and decoding of data are used extensively in digital communications as well as in peripherals. Both these areas use various complex encoding and decoding techniques. Most of these techniques are extensions of the simple encoding and decoding techniques often used in other digital designs. In this discussion we will focus on simple encoding and decoding techniques. More complex techniques will be discussed later.

Encoders

A binary code of n bits can be used to represent 2n distinct pieces of coded data. A simple combinatorial encoder is a circuit which generates n bits of output information based upon one of the 2n unique pieces of input data information. This encoding of information is controlled by other independent control signals in a typical digital circuit.

An illustration of a typical encoder is shown in Figure 1. The design methodology typically followed is based on truth tables (Table 1), from which the Boolean equations are directly derived for the design. The same generic device selection considerations discussed in the section on PAL device design methodology apply for encoder and decoder designs.

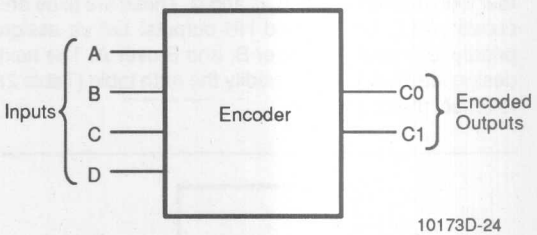


Figure 1. A Block Diagram of an Encoder

Table 1. Truth Table of a Typical Encoder

Inputs				Outputs	
A	B	C	D	C0	C1
1	0	0	0	L	L
0	1	0	0	L	H
0	0	1	0	H	L
0	0	0	1	H	H

The Boolean equations can then be optimized using Karnaugh maps or the software minimizer.

The resulting Boolean equations are:

```
C1  =  /A  *  B  *  /C  *  /D
    +  /A  *  /B  *  /C  *  D

C0  =  /A  *  /B  *  C  *  /D
    +  /A  *  /B  *  /C  *  D
```

A Priority Encoder

Let us take another look at the encoder example of Table 1. In this example it is assumed that only one of the inputs A, B, C or D is asserted HIGH at any one time. If two of the inputs are asserted HIGH simultaneously, a conflict would be created. To resolve this, a priority needs to be assigned to each of the inputs. Such a priority assignment is used to select a particular element when several inputs are asserted simultaneously. Each input is assigned a priority with respect to the other inputs. The output code generated is the code assigned to the highest priority input asserted.

Thus, a priority encoder is a combinatorial circuit block similar to a general encoder, except that the inputs are assigned a priority. Such priority encoders are used often in state machine applications, where they detect

the occurrence of the highest priority event. They are also used for microprocessor interrupt controllers, where they detect the highest priority interrupt. Another use for priority encoders is in bus control, where they are used in arbitration schemes for allowing selective access to the bus.

The model of a priority encoder is shown in Figure 2. The four input signals are A, B, C and D. These are to be encoded as LL, LH, HL and HH outputs. Let us assign priority to D over C, C over B, and B over A. The next design step would be to modify the truth table (Table 2) to reflect these priorities.

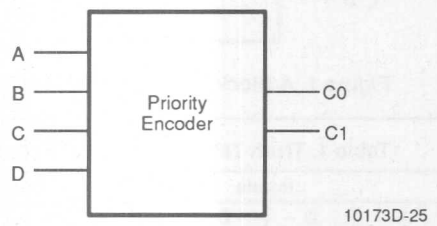


Figure 2. A Four-Input Priority Encoder Block Diagram

Table 2. Priority Encoder Truth Table

Inputs				Outputs		
A	B	C	D	C0	C1	
1	0	0	0	L	L	
0	1	0	0	L	H	
0	0	1	0	H	L	
0	0	0	1	H	H	
X	1	0	0	L	H	Priority Assignments
X	X	1	0	H	L	
X	X	X	1	H	H	

The Boolean equations, directly derived from the truth table, are:

```
C1  =  /A  *   B   *  /C   *   /D
    +  /A  *  /B   *  /C   *    D
    +          B   *  /C   *   /D
    +                         D

C0  =  /A  *  /B   *   C   *   /D
    +  /A  *  /B   *  /C   *    D
    +                 C   *   /D
    +                         D
```

These equations can be further optimized by the design software to the following:

```
C1  =   D  +  /C  *   B
C1  =   D  +   C
```

Although a priority encoder is a purely combinatorial function, output registers are frequently used to hold the output signal stable for longer durations.

Decoders

A decoder performs the reverse function of an encoder. It converts an n-bit code to one of its 2^n unique items. It is a combinatorial circuit designed such that at most one of its several outputs will be asserted based upon the unique input codes.

A decoder may have as many outputs as there are possible binary input selection combinations. As shown in the truth table (Table 3), only one output may be asserted at any time. When a new combination is applied, another output is asserted and the original output is returned to its non-asserted state.

Table 3. The Truth Table of an Active-LOW 4-to-16 Decoder

Input Select Lines				Output Lines															
A	B	C	D	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

The Boolean logic equations can be directly derived from the truth table shown in Figure 5. The procedure is the same as explained in the previous section on PLD design methodology. The Boolean equations derived are shown in Figure 3.

```
/Q0  =  /D  *  /C  *  /B  *   /A
/Q1  =  /D  *  /C  *  /B  *    A
/Q2  =  /D  *  /C  *   B  *   /A
/Q3  =  /D  *  /C  *   B  *    A
/Q4  =  /D  *   C  *  /B  *   /A
/Q5  =  /D  *   C  *  /B  *    A
/Q6  =  /D  *   C  *   B  *   /A
/Q7  =  /D  *   C  *   B  *    A
/Q8  =   D  *  /C  *  /B  *   /A
/Q9  =   D  *  /C  *  /B  *    A
/Q10 =   D  *  /C  *   B  *   /A
/Q11 =   D  *  /C  *   B  *    A
/Q12 =   D  *   C  *  /B  *   /A
/Q13 =   D  *   C  *  /B  *    A
/Q14 =   D  *   C  *   B  *   /A
/Q15 =   D  *   C  *   B  *    A
```

Figure 3. Decoder Boolean Logic Equations

Probably the most commonly used decoders are the address decoders required by most microprocessors and bus interfaces. These also constitute the most common application of PLDs in digital designs. The design considerations for address decoders have been covered earlier in the PLD Design Methodology section. Later we will develop a general Boolean equation for an address decoder circuit when we discuss range decoders.

Encoder/Decoder Device Selection Considerations

The general device selection considerations are listed below. Based upon the number of inputs and outputs required, a device can be selected.

- Number of Input Pins
- Number of Output Pins
- Number of I/O Pins
- Device Speed
- Device Power Requirements
- Number of Registers
- Number of Product Terms
- Output Polarity Control

Encoders typically require a large number of inputs and fewer outputs, whereas decoders typically require a large number of outputs and fewer inputs.

Notice from the truth table that there is no combination of inputs that will send all the outputs to their non-asserted state. Many designs actually need to be able to make all outputs inactive. This can be done simply by putting enable lines in all of the output AND gates. Many such design modifications can be easily added once the basic Boolean equations have been derived, instead of redoing the truth table.

Another important device selection consideration for encoders and decoders is the number of product terms required for a design. A careful selection of code values

(and priority assignments in priority encoders) can often reduce the required number of product terms. This can sometimes determine whether or not a design fits a device successfully. Figure 4 shows the truth tables of two simple partial 3-to-2 encoders. The product terms required for the two designs are different due to the different assignment of encoded bits.

Inputs			Outputs	
A	B	C	X1	X0
1	0	0	0	0
0	1	0	0	1
0	0	1	1	0

```
X1 =  /A * /B * C

X0 =  /A * /B * /C
```

Inputs			Outputs	
A	B	C	X1	X0
1	0	0	0	1
0	1	0	1	0
0	0	1	1	1

```
X1 = /A * B * /C
   + /A */B *  C

X0 =  A * /B * /C
   + /A * /B *  C
```

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Figure 4. Two Encoders with Different Product Term Requirements

Another way of looking at a decoder is as a logic function which, depending upon the select code applied, connects one data input to the selected outputs. Also known as a demultiplexer, a decoder essentially connects an input to one of 2^n outputs based upon n select code bits. The reverse logic function, which combines data from multiple sources to an output signal, is called a multiplexer and is discussed next.

Multiplexers

A multiplexer (sometimes referred to as a data selector) is a special combinatorial circuit, widely used in digital design. It is designed to gate one of several inputs to a single output. The input selected for connection to the output is controlled by a separate set of select inputs.

The traditional use of a multiplexer is for "time division multiplexing" in data communication, when gating several data lines to a single data transmission line for short intervals of time. The data received is then demultiplexed by using a demultiplexer.

The design methodology employed for multiplexer design is the truth-table approach. As an example, we can look at a three in put-to-one-output (3:1) multiplexer, which uses two select signals A and B. Based on these two select bits, the data on one of the three inputs is sent to the output. The truth table is shown in Table 4.

Table 4. Truth Table for a Three-to-One Multiplexer

Select		Inputs			Output
B	A	I1C0	I1C1	I1C2	O1Y
0	0	0	X	X	0
0	0	1	X	X	1
0	1	X	0	X	0
0	1	X	1	X	1
1	0	X	X	0	0
1	0	X	X	1	1

Deriving the Boolean equation from this truth table is a straight forward task. In this case no further minimization is possible. The Boolean equation is:

```
/01Y  =  /B  *  /A  *  /I1C0
      +  /B  *   A  *  /I1C1
      +   B  *  /A  *  /I1C2
```

The equations derived in the above example can be easily generalized for other multiplexers. The symbol for a general 2^n-inputs-to-one-output multiplexer is shown in Figure 5 where n select lines are used.

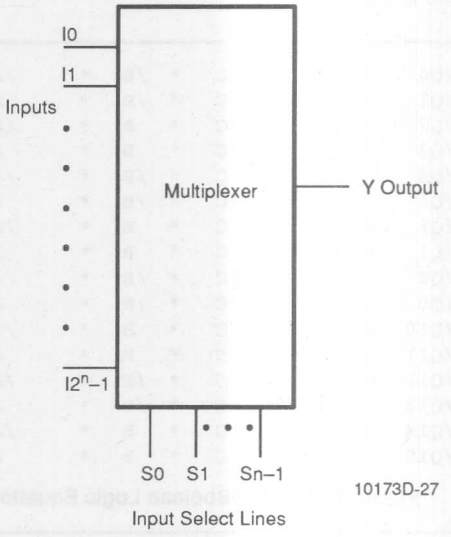


Figure 5. General Model of a 2^n-to-1 Multiplexer

The Boolean equations are:

n=2

```
Y  = /S1  * /S0  *  (I0)
   + /S1  *  S0  *  (I1)
   +  S1  * /S0  *  (I2)
   +  S1  *  S0  *  (I3)
```

n=3

```
Y  = /S2  *  /S1  * /S0  *  (I0)
   + /S2  *  /S1  *  S0  *  (I1)
   + /S2  *   S1  * /S0  *  (I2)
   + /S2  *   S1  *  S0  *  (I3)
   +  S2  *  /S1  * /S0  *  (I4)
   +  S2  *  /S1  *  S0  *  (I5)
   +  S2  *   S1  * /S0  *  (I6)
   +  S2  *   S1  *  S0  *  (I7)
```

Multiplexer Device Selection Considerations

Multiplexers typically require more inputs than outputs, so the devices with a large number of inputs and I/Os are usually more useful. Careful consideration must also be given to the number of product terms available on each output.

Several multiplexers are often used simultaneously to route multiple address and data bits, under the control of the same select lines. In such cases, multiple devices can be cascaded when the number of inputs and outputs exceeds device limits. Cascading is also possible for large multiplexers that do not fit in a single device. In such cases, the select bits should also be judiciously selected for each PLD, to minimize the number of product terms.

Another common trick for designing a multiplexer is to connect a number of outputs together and control the output enables using the select bits to multiplex data. Timing considerations for such designs include the output enable and disable times, which should be carefully selected to avoid output contentions.

Comparators

A comparator is a combinatorial circuit designed primarily to compare the relative magnitude of two binary numbers. Table 5 shows the truth table for a two-bit comparator.

Table 5. Truth Table for a Comparator

Inputs				Outputs		
A		B		EQL	LES	GTR
A2	A1	B2	B1	A=B	A<B	A>B
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0

A basic comparator compares two numbers only for equality, and generates the EQL signal (indicating A=B). An extension, called a magnitude comparator, also generates the LES signal (indicating A<B) and GTR signal (indicating A>B). Based on this truth table, the equations for the three output signals EQL, LES and GTR can be easily derived. These equations can then be optimized by using Boolean algebra, Karnaugh maps, or the minimization routine available with the software.

The final Boolean equations are:

```
EQL   = /A2* /A1   * /B2   * /B1
      + /A2   *  A1* /B2   *  B1
      +  A2* /A1       * B2   *    /B1
      +  A2   *  A1    * B2   *     B1

LES   = /A2   * /A1   * /B2   *     B1
      + /A2   * /A1   *  B2   *    /B1
      + /A2   * /A1   *  B2   *     B1
      + /A2   *   A   *  B2   *    /B1
      +/A2    *  A1   *  B2   *     B1
      + A2 */A1   *  B2   * B1

      = /A1   * /B2   *  B1
      + /A2   * /A1   *  B1
      + /A2   *  B2

GTR   = /A2   *  A1   * /B2   *    /B1
      +  A2   * /A1   * /B2   *    /B1
      +  A2   *  A1   * /B2   *    /B1
      +  A2   * /A1   * /B2   *     B1
      +  A2   *  A1   * /B2   *     B1
      +  A2   *  A1   *  B2   *    /B1

      = /A1   * /B2   * /B1
      + /A2   *  A1   * /B1
      + /A2   * /B2
```

Comparator Device Selection Considerations

The number of product terms needed is directly related to the number of bits compared. For LES (less than) and GTR (greater than) functions, the number of product terms required depends upon the number of bits in the two operands compared, as well as their value. The LES and GTR equations can be written as follows:

```
LES   =  B2   * /A2
      + (B2 :+:/A2)   *  B1*/A1

GTR   =  A2   * /B2
      + (A2 :+:/B2)   *  A1*/B1
```

These equations can then be extended for a general comparison of n-bit comparands as follows:

```
LES   =  Bn   * /An
      + (Bn :+:/An)   *Bn-1  *  /An-1
      + (Bn :+:/An)   *(Bn-1:+:/An-1)
        *Bn-2 */An-2

      + ...
      + ...
      + ...

      + (Bn :+:/An)   *(Bn-1:+:/An-1)...
        (B2 :+:/A2)   *  B1  *    /A1

GTR   =  An   * /Bn
      + (An :+:/Bn)   *An-1  *  /Bn-1
      + (An :+:/Bn)   *(An-1:+:/Bn-1) *
        An-2 */Bn-2

      + ...
      + ...
      + ...

      + (An :+:/Bn)   *(An-1:+:/Bn-1)...
        (A2 :+:/B2)   *  A1* /B1
```

The total number of product terms required for an n-bit comparison is 2^n-1. Comparators required a large number of product terms so, devices that offer many product terms can be used very effectively.

As is obvious from these equations, comparators require exclusive-OR functions. They can be efficiently implemented in devices that offers exclusive-OR functions but, can still be implemented in those devices that do not.

The values of the comparands themselves affect the number of product terms used. When the comparison is made with comparands which are power-of-two numbers, the number of product terms required can be reduced drastically. This essentially relies on the fact that when the lower bits of a comparand are all zeros only the highest bit needs to be compared, requiring only one product term. For example, in a two-bit comparator, if A1 is zero and A2 is one, the equation for the greater-than function becomes very simple and requires only one product term:

```
GTR = /B2
```

The general equation for the GTR signal can also be simplified when comparing a number B to a fixed power-of-two comparand A with p least significant zeros.

```
A  =  000010000 ...  00
      n    p         1

GTR = /Bn */Bn-1...*/Bp+1 */Bp
```

This general GTR equation can also be considered as an equation for comparing a number to a range of numbers extending from zero to number A. In fact, this trick is used very often by many system designers for address decoder functions. In the PLD design methodology section the ROMCS1 signal is one such signal that is generated for the address range from (000000) hex to (0FFFFF) hex. For this design n=23, the comparand A=(0FFFFF + 1)=100000, and p=21. Substituting in the general equation we get the same address decoder Boolean logic equation.

```
ROMCS1 = /A23 * /A22* /A21
```

As such designs require few product terms and no XOR gates, they are efficiently implemented on standard combinatorial PLDs. A general form of range comparators with two boundary comparands will be discussed later.

The third output signal is the EQL signal. The EQL Boolean equation tells us whether the two numbers are identical. Such information is useful not only in address decoders, but also in digital signal processing designs. This equation requires a large number of product terms. A closer examination reveals that it is essentially an exclusive-OR function.

```
EQL = /A2 * /B2 * (/A1 * /B1 + A1 * B1)
    + A2 *  B2 * (/A1 * /B1 + A1 * B1)

EQL = (A1:*:B1)* (A2:*:B2);Exclusive-NOR
                           ;function
```

Inverting this:

```
/EQL = (A1:+:B1) + (A2:+:B2); Exclusive-OR
                            ; function
```

This equation can be extended to give a general equation for equal-to comparison for two n-bit comparands.

```
/EQL  = (An :+: Bn)
      + (An-1 :+: Bn-1)
      + (An-2 :+: Bn-2)
      + (An-3 :+: Bn-3)
      + ...
      + ...
      + (A1 :+: B1)
```

This inverted equation is implementable in the sum-of-products form of the exclusive-OR functions, and can be easily expanded to the following:

```
/EQL  = A1 * /B1 + /A1 * B1
      + A2 * /B2 + /A2 * B2
      + A3 * /B3 + /A3 * B3
      + ...
      + ...
      + An * /Bn + /An * Bn
```

This gives us a general sum-of-products form of a comparator equation which is easily implemented in PAL devices. A n-bit comparator requires 2n product terms.

Note that the EQL equation, as well as GTR and LES equations, rely upon the XOR function. Often the logic represented by the equations is implemented in two or more devices.

Let us analyze these equations further. The LES and GTR outputs indicate whether one number is greater than or less that another. In fact, these equations can also be judiciously combined to get a comparison of a range of numbers such as A>X>B. Such range comparisons are very useful for address decoder circuits.

Range Decoders

Range decoders implemented as address decoders are one of the most commonly used applications of PLDs in digital systems. A good example is the address decoder illustrated earlier. Range decoders compare a number (address) to a given range of comparands (addresses). One way to arrive at the range decoder Boolean equations is to use the traditional truth table approach. Another way is to use the Boolean equations generated earlier in the comparator section for greater-than and less-than functions. To decode a range of three-bit numbers from B to A, we must compare another number X such that A>X>B. The Boolean equations for the GTR (A>X) and LES (B<X) functions are illustrated below:

```
GTR   =  A3 */X3
      + (A3 :+: /X3)   *  A2* /X2
      + (A3 :+: /X3)   * (A2:+: /X2 *A1 *
        /X1

LES   =  X3   * /B3
      + (X3 :+: /B3)   * X2 * /B2
      + (X3 :+: /B3)   * (X2:+: /B2)* X1
        */B1
```

Combining these two equations can give us a range signal which will be asserted only when A is greater than X and X is greater than B. The combined Boolean equation follows:

```
RANG  = (A3   * /X3
      + (A3 :+: /X3)   *  A2 * /X2
      + (A3 :+: /X3)   * (A2 :+: /X2)* A1 *
        /X1) * (X3*/B3
      + (X3 :+: /B3)   *  X2 * /B2
      + (X3 :+:  /B3   * (X2 :+:/B2) * X1
        */B1)
```

Using Boolean algebra we get the following equation:

```
RANG  =
        (A3  :+:/X3)  *  (X3  :+: /B3)  *  (A2  :+: /X2)*  A1   *  /X1 *  X2  * /B2
      + (A3  :+:/X3)  *  (X3  :+: /B3)  *  (X2  :+: /B2)*  A2   *  /X2 *  X1  * /B1
      + (A3  :+:/X3)  *  (A2  :+: /X2)  *  A1    *  /X1 *  X3   *  /B3
      + (X3  :+:/B3)  *  (X2  :+: /B2)  *  A3    *  /X3 *  X1   *  /B1
      + (A3  :+:/X3)  *  A2    *   /X2  *  X3    *  /B3
      + (X3  :+:/B3)  *  A3    *   /X3  *  X2    *  /B2
```

The general equation for n-bit comparands can also be obtained by extending these equations.

```
RANG  =  (An   *  /Xn
      +  (An  :+:/Xn)  *  An-1   * /Xn-1
      +  (An  :+:/Xn)  *  (An-1:+:/Xn-1) *  An-2  *  /Xn-2
      +  ...
      +  ...
      +  (An  :+:/Xn)  *  (An-1:+:/Xn-1)... (A2  :+: /X2)*  A1   *  /X1)
      *
         (Xn   *  /Bn
      +  (Xn  :+:/Bn)  *  Xn-1   * /Bn-1
      +  (Xn  :+:/Bn)  *  (Xn-1:+:/Bn-1) *  Xn-2  *  /Bn-2
      +  ...
      +  ...
      +  ...
      +  (Xn  :+:/Bn)  *  (Xn-1:+:/Bn-1)... (X2  :+: /B2)*  X1   *  /B1)
```

The number of product terms required is clearly very large and can easily exceed one hundred for an eight-bit range comparator. Most microprocessors have addresses which exceed 16 bits. In order to fit the design on a PAL device, one commonly used technique is to select the address range defined by A and B such that the range extends from address B+1 to A–1, where A and B+1 are power-of-two numbers. Because the address space is aligned on the power-of-two boundaries, a number of bits of the address comparands will be zero. When implemented in Boolean equations, this substantially reduces the number of product terms required.

The maximum number of product terms required for a three-bit range decoder shown above, with any comparand values, is 28. If the address chosen is from 2 to 3, resulting in A=4 and B=1, then only one product term will be required.

```
RANG = /X3 * X2
```

Similarly, for a range from one to five, B =1 and A = 6 (a multiple-of-two), and the number of product terms required is only two.

```
RANG  = /X3 * X2
      + X3 * /X2
```

Thus, a careful selection of range boundaries allows such logic functions to be implemented easily in PLDs. Such reduction in logic obviously also holds true for discrete implementations. Most address decoders are designed with address ranges with boundaries that are power-of-two numbers, and require few product terms for implementation.

For a power-of-two address range, the comparand A would be a power-of-two; 2, 4 or 8. These are numbers whose least significant bits are all zeros. Similarly, comparand B will be a power-of-two number (minus one); 1, 3, and 7. These are numbers whose least significant bits are all ones. Substituting these in the general equation for range comparators we arrive at:

```
A  =  0000100000000000
      n   p       1

B  =  0000000000011111
      n   q       1

RANG  =    /Xn * /Xn-1 *...* /Xp *
           (Xp-1 + Xp-2 + ... +Xq)
```

This is a general equation for a power-of-two range comparison. In the address decoder example, the ROMCS2 signal addresses the range from 100000 to 1FFFFF, in which case B=0FFFFF and A=2FFFFF. Here n=23, p=22, and q=21. The address decode equation for the ROMCS2 signal can be arrived at by substituting:

```
ROMCS2 = /A23 * /A22 * A21
```

This is the same equation that was found from the truth table.

Such designs are very common for address decoder applications. These do not require any XOR gates, and can be implemented in standard combinatorial PLDs with only sum-of-products logic.

Adders/Arithmetic Circuits

Digital systems are designed to carry out a variety of arithmetic instructions on binary numerical data. A good example is the ALU (Arithmetic Logic Unit) used in digital computers. The basic function of an ALU is that of an adder performing addition on two binary numbers. A binary adder takes two inputs, adds them, and generates the binary sum. A full adder is a one-bit adder with carry-in and carry-out; this is the basic building block of any adding circuit. The truth table of such an adder is shown in Table 6.

Table 6. Truth Table for a Full Adder

Inputs			Outputs	
A	B	C_{IN}	Y	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

This truth table is then used to form the Boolean equations in the manner described earlier.

```
Y     =   A   *  /B   */Cin
      +  /A   *  /B   * Cin
      +   A   *   B   * Cin
      +  /A   *   B   */Cin

Cout  =   A   * Cin
      +   A   * B
      +   B   * Cin
```

Larger binary adders can be made by cascading these full adders. Each carry-out is directed to carry-in for the next stage. Such adders are known as Ripple Adders.

Combinatorial PAL devices are ideal for this purpose, since they also provide internal feedback. Thus, one strong consideration in such designs is the internal feedback capability of the device, in addition to other general device selection considerations.

These ripple adders have the advantage that they can be cascaded to any length. However, since the carry-out from the least significant bit has to travel all the way to the highest significant bit, which can take a long time, such large adders are inefficient. Adders with built in carry-look-ahead circuitry can save time by simultaneously generating the carry-in signal for all of the bits.

Rewriting the equations for the full adder from above gives:

```
Y0 =  A0:+: B0:+:Cin
```

where the carry-out signal is:

```
C0 =  A0  *  B0    + (A0   +B0) * Cin
```

Extending these equations for an n-bit carry-look-ahead adder, we can directly get the following equations:

```
Y0 =  A0:+:  B0  :+: Cin

Y1 =  A1:+:  B1  :+:  C0
```

where

```
C0 =  A0  *  B0
   +  (A0 + B0)    * Cin

Y2 =  A2  :+: B2 :+:  C1
```

where

```
C1 =  A1  *  B1
   +  (A1 + B1)    * (A0   * B0)
   +  (A1 + B1)    * (A0   +B0) * Cin

Y3 +  A3:+:  B3  :+:  C2
```

where

```
C2 =  A2  *  B2
   +  (A2 + B2)    * (A1   * B1)
   +  (A2 + B2)    * (A1   +B1) * (A0 * B0)
   +  (A2 + B2)    * (A1   +B1) * (A0+ B0)
      * Cin
```

In general,

```
Yn =  An:+:  Bn  :+:Cn-1
and Cn-1  =An-1   *Bn-1
   +  (An-1   +Bn-1)  *(An-2 *  Bn-2)
   +  ...
   +  ...
   +  (An-1   +Bn-1)  * ...   *    (A0
   +  B0) * Cin
```

and finally the carry-out is:

```
Cn =  An  *  Bn
   +  (An + Bn)    *(An-1  *Bn-1)
   +  (An + Bn)    *(An-1  +Bn-1) *
      (An-2*  Bn-2)
   +  ...
   +  ...
   +  (An + Bn)    * ...    *(A0 + B0) * Cin
```

These equations are essentially a combination of the traditional generate and propagate logic for ALU design.

Adder Device Selection Considerations

The number of product terms required for implementing a carry-look-ahead adder is enormous. The carry-out function alone for a four-bit carry-look-ahead adder requires over 36 product terms in the sum-of-products form. For a single-level AND-OR implementation the number of product terms required for the most significant bit Y3 is 28.

A logic trick lies in the bit-pair decoding function. All of the bits of the first operand in the registers (A) and the second operand at the inputs (B) are bit-pair decoded. As illustrated in Figure 6, the results of this bit-pair decoding are A + B, A + /B, /A + B, and /A + /B. These outputs are then fed to the AND array as inputs.

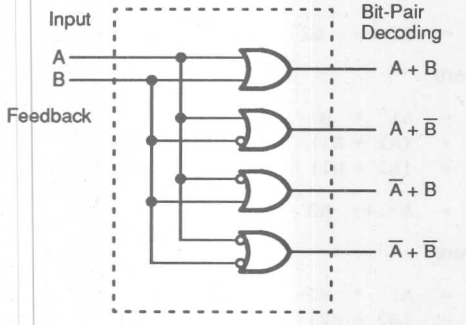


Figure 6. Bit-Pair-Decoding Function

Sixteen AND combinations of these four inputs can then be formed on every product term of the AND-OR array. These are shown in Figure 7, and include the standard true and complements of both the bits as well as XOR< XNOR and various other combinations. This bit pair decoding essentially provides an extra two-level AND-OR logic level before the AND-OR array. The cost as well as extra propagation delay of the extra logic level is minimal, since the array size does not increase.

The equations for the adder can obviously benefit from multi-level logic. The bit-pair decoding can be used to implement the first two levels of logic. The next level of logic can be implemented in the standard AND-OR array. Every product term of the AND-OR array can combine one of the sixteen possible functions of different inputs/feedbacks of the device.

The product terms are then combined together through an OR gate to implement the CARRY-OUT function, shown in Figure 8. For adder outputs Y0, Y1, Y2, and Y3, the product terms are combined through an XOR gate, as shown in Figure 9.

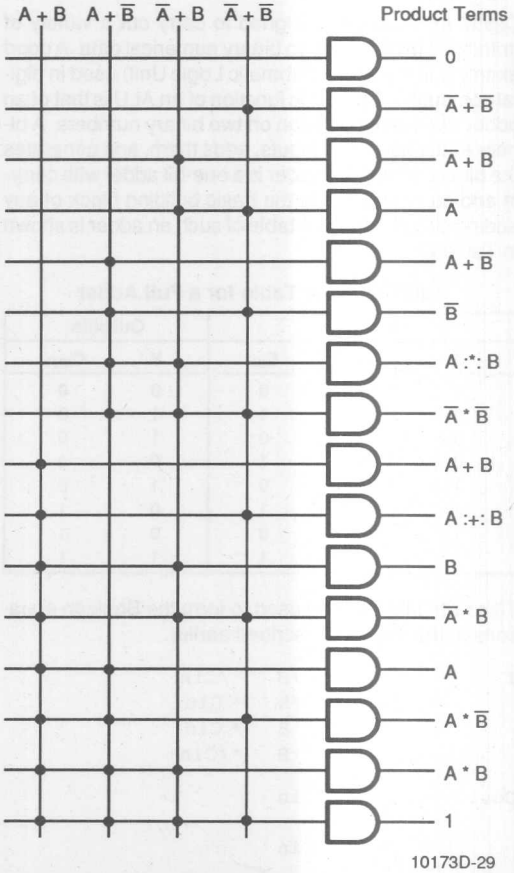
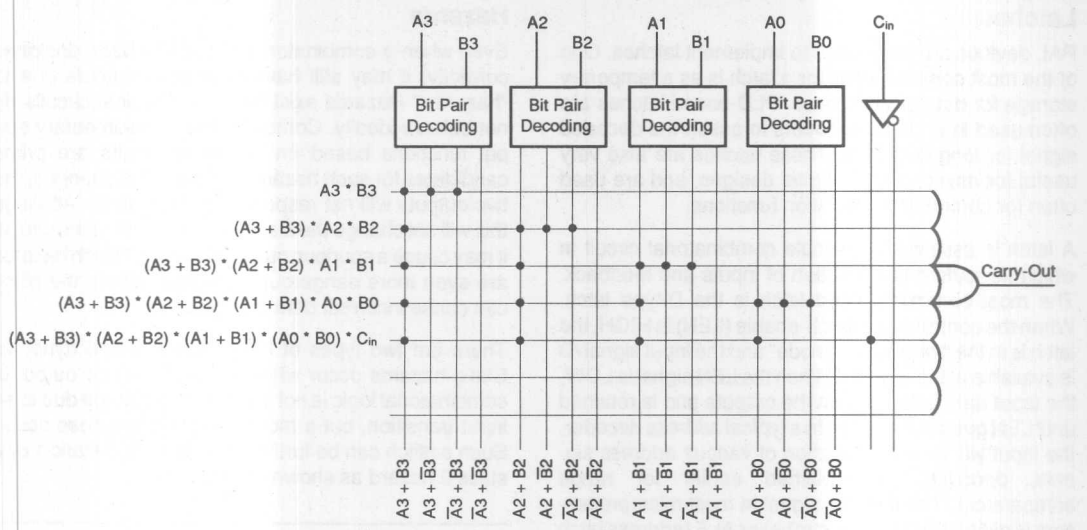


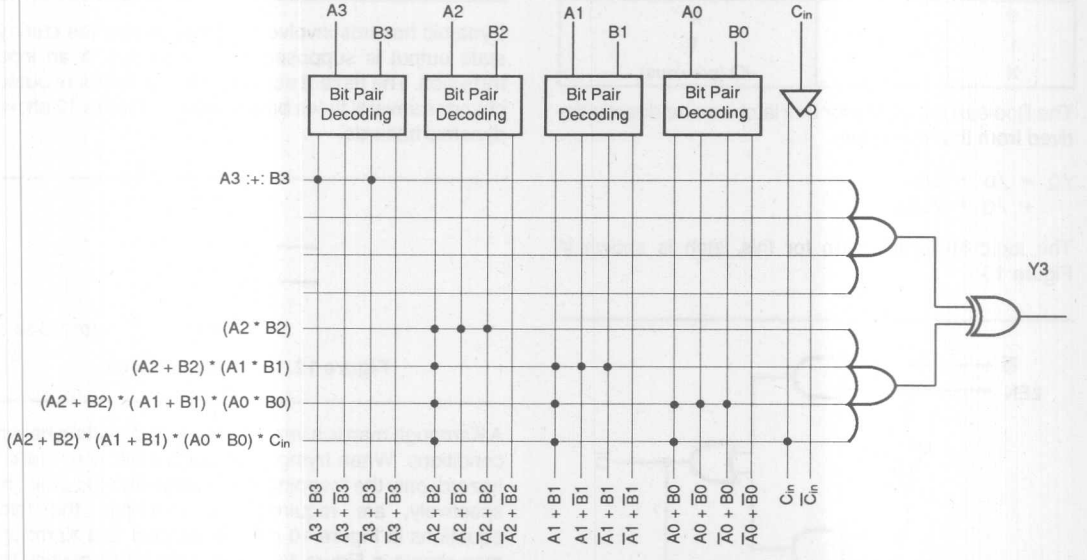
Figure 7. Sixteen Possible Input Logic Combinations



Carry-Out = A3 * B3
(A3 + B3) * A2 * B2
(A3 + B3) * (A2 + B2) * A1 * B1
(A3 + B3) * (A2 + B2) * (A1 + B1) * A0 * B0
(A3 + B3) * (A2 + B2) * (A1 + B1) * (A0 * B0) * C_{in}

10173D-30

Figure 8. Implementation of CARRY-OUT Function



Y3 = A3 :+: B3
:+: (A2 * B2)
+(A2 + B2) * (A1 * B1)
+(A2 + B2) * (A1 + B1) * (A0 * B0)
+(A2 + B2) * (A1 + B1) * (A0 * B0) * C_{in})

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Figure 9. Relationship Between Adder Boolean Equation and Device Logic

Latches

PAL devices are often used to implement latches. One of the most common uses for a latch is as a temporary storage for data or addresses. PLD-based latches are often used in address decoders to assert the decoded signal for long durations. These latches are also very useful for asynchronous digital designs, and are used often for control and arbitration functions.

A latch is essentially a simple combinatorial circuit in which the output is a function of inputs and feedback. The most commonly used latch is the D-type latch. When the control signal latch-enable (LEN) is HIGH, the latch is in the "transparent mode" and the input signal /D is available at the outputs. When the LEN signal is LOW, the input data is latched on the outputs and is retained until LEN goes back HIGH. In a typical address decoder, the input will be a combination of various address signals, decoded as explained earlier for range comparators. The latching signal in most microprocessors is called AS (address strobe) or ALE (address latch enable).

The truth table for a latch can be derived directly from this functional description, and is shown in Table 7.

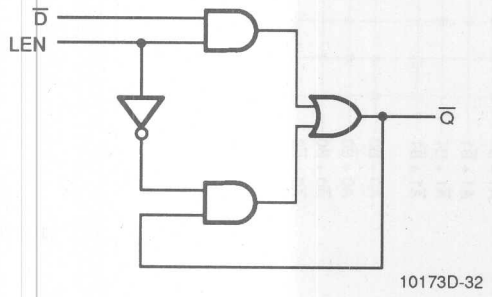
Table 7. Truth Table of a Simple Latch

Inputs		Outputs
/D	LEN	/Q
0	1	0
1	1	1
X	0	/Q (previous)

The Boolean equations for this latch can be directly derived from the truth table:

```
/Q = /D * LEN
   + /Q * /LEN
```

The logic implementation for this latch is shown in Figure 10.



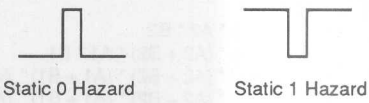
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Figure 10. A Transparent Latch

Hazards

Even when a combinatorial circuit has been designed correctly, it may still have erroneous outputs due to "hazards." Hazards exist because physical circuits do not behave ideally. Combinatorial complementary output functions based on the same inputs are prime candidates for such hazards. As the input changes, the two outputs will not respond simultaneously. Although this will not change the steady-state output of the circuit, it may cause a spurious pulse or a "glitch." Such hazards are even more dangerous in latches, where the glitch can cause incorrect data to be latched.

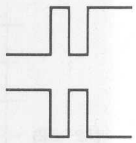
There are two types of hazards, static and dynamic. Static hazards occur when the steady-state output of combinatorial logic is not supposed to change due to an input transition, but a momentary change does occur. Such a glitch can be further classified as a static 1 or a static 0 hazard as shown in Figure 11.



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Figure 11. Static Hazards

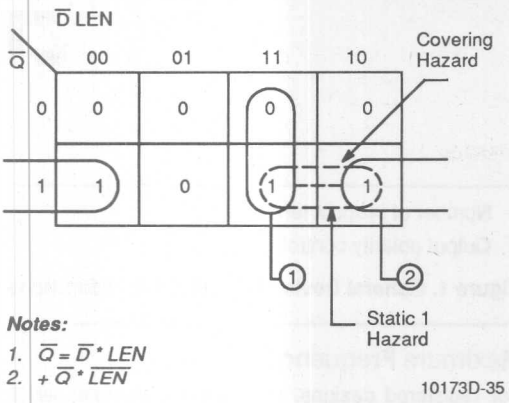
Dynamic hazards involve situations where the steady-state output is supposed to change due to an input transition. The hazard occurs when the transient output changes several times before settling. Figure 12 shows dynamic hazards.



10173D-34

Figure 12. Dynamic Hazards

A Karnaugh map is a very good way of detecting hazard conditions. When trying to detect a static 0 or static 1 hazard, only the mapping of the zeros and the ones, respectively, are required. For example, the latch equations in Figure 10 can be mapped to a Karnaugh map shown in Figure 13. The relationship between the Karnaugh mapping and the Boolean equation product terms is also illustrated.



Notes:
1. $\overline{Q} = \overline{D} * LEN$
2. $+ \overline{Q} * \overline{LEN}$

10173D-35

Figure 13. Karnaugh Map for Transparent Latch Design

The possibility of a hazard exists when the signal LEN changes. Initially, when D and LEN are HIGH, the output Q is also HIGH. When LEN switches to LOW, it is possible for the output to go LOW momentarily. This is because when LEN goes LOW the first product term is disabled, and to maintain the output HIGH the second product term should be enabled exactly at the same instant. Due to the uneven gate delays or routing conditions on board, these two events will not take place simultaneously. This is a static 1 hazard. It can also be identified directly in the Karnaugh map by the two adjacent but disjoint sets of ones, grouped together to form a product term each.

The hazard conditions can be easily avoided in the PLDs by providing an extra cover product term. This product term is shown with a dotted line in the Karnaugh map. This third product term will keep the output asserted during the transition of the LEN signal, when the control changes from the first product term to the second. The modified Boolean equation is shown below.

```
/Q = /D * LEN
   + /Q * /LEN
   + /D * /Q     (Cover product term)
```

Devices on which latches are implemented need to provide output feedback. All devices with I/O pins provide this necessary feedback. The only other consideration for selecting a device would be the provision of sufficient number of product terms for addressing the needs of glitch-free and testable design.

Registered Logic Design

INTRODUCTION

In the previous section we discussed combinatorial designs, circuits whose outputs are totally independent of any system clock. In this section we will discuss sequential circuits, where outputs store their previous values until a new clock is applied. The storage elements which retain the previous output values are called flip-flops. A bank of these flip-flops forms a register, although individual flip-flops are often called registers.

Before we discuss purely registered designs, let us take a look at designs which combine both registered and combinatorial portions. Registered and combinatorial outputs are often mixed on a single device. There can be two distinct designs, one registered and one combinatorial (often glue logic) combined on a single device for higher integration. There may also be a design requirement where registered outputs need to be decoded using combinatorial logic.

There are a number of devices which provide both registered and combinatorial outputs. Most devices provide programmable register bypass, which allows outputs to be programmed as registered or combinatorial.

In most design software packages, the output registers are signified by the ":=" assignment symbol, as opposed to the "=" sign for a combinatorial output. This helps to easily identify registers in each equation. In devices which provide outputs configurable as either registered or combinatorial, this sign is also used by the software to configure the outputs.

General Device Selection Considerations

The same set of general device selection considerations discussed in the PLD design methodology section apply to registered designs. The list of items which must be considered is repeated in Figure 1 for convenience. A device can be conveniently selected based upon the specific input and output requirements.

- Number of input pins
- Number of output pins
- Number of I/O pins
- Device speed
- Device power requirements
- Number of registers
- Number of product terms
- Output polarity control

Figure 1. General Device Selection Considerations

Maximum Frequency

For registered designs, speed is a parameter which needs careful consideration. Most combinatorial designs use the propagation delay (t_{PD}) for ensuring that enough time is allowed for the data from the inputs to appear at the outputs. In registered designs the effects of the clock must be taken into account. This is reflected in the maximum frequency (f_{MAX}) parameter. The flexibility inherent in PLD design provides a choice of configurations from which different f_{MAX} parameters can be calculated.

In the first type of design, the PLD is used for a standalone registered design. In order to decide the next logic level of the registers, the present logic level needs to be available at the inputs of the registers before they are clocked (Figure 2.) Under these conditions the clock period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flops inputs. This f_{MAX} is designated "f_{MAX} *internal.*" A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

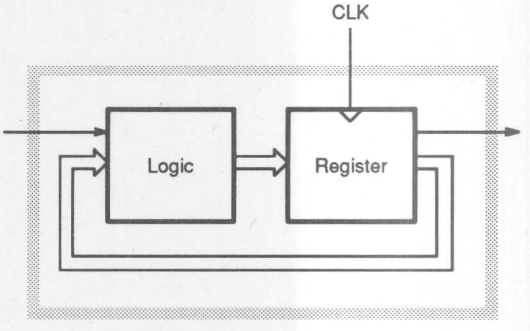


Figure 2. Internal f_{MAX}

The second type of system configuration is when a number of logic devices with registers, including PLDs, are clocked with a common clock. This is probably the most prevalent configuration. In this case, the registered outputs are sent off-chip back to the device inputs or to the inputs of a second device. The slowest path defining the period (Figure 3) is the sum of the clock-to-output time and the input setup time for the external signals (t_S+t_{CO}). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} *external*."

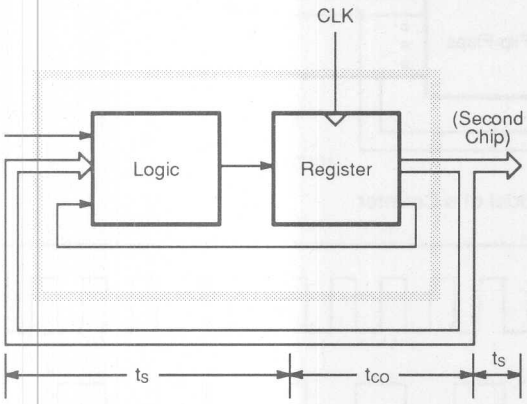


Figure 3. External f_{MAX}

The third type of design is a simple data path application. In this case, input data is presented, to the flip-flop and clocked; no feedback is employed (Figure 4). In this case, the period is limited by the sum of data setup time and data hold time (t_S+t_H). However, the minimum clock period ($t_{WH} + t_{WL}$) is usually a stricter limit. Thus, the third f_{MAX} designated "f_{MAX} *no feedback*" will be the lesser of $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$.

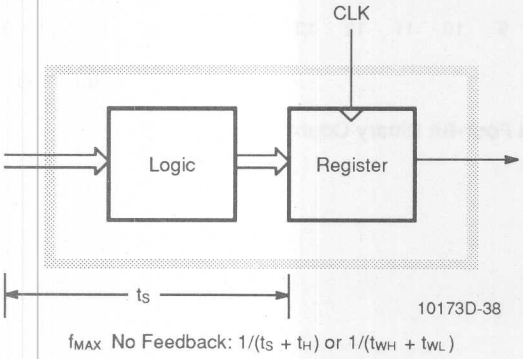


Figure 4. f_{MAX} with No Feedback

f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} internal is measured.

Flip-Flop Types

There are four basic types of flip-flops; S-R, J-K, T and the popular D-type.

In this section, we will assume that the reader is familiar with these flip-flops.

Almost all registered PLDs provide the basic D-type flip-flops. D-type flip-flops are the simplest to design with and will be used throughout this section. Some PLDs provide the capability of configuring output registers as either D, T, J-K or S-R. Configurable flip-flops in some cases can reduce the number of product terms required for certain designs. The effect of the configurable flip-flops will be discussed wherever relevant.

Synchronous vs. Asynchronous

Registered designs can be easily classified into two categories; synchronous and asynchronous. In synchronous designs the clock inputs of all the registers are tied together to a common clock. With asynchronous designs, the flip-flops' clock inputs may not be tied together, and the clocks may be gated or even driven by other flip-flops. We will first discuss synchronous registered designs and then asynchronous registered designs.

Synchronous Registered Designs

Synchronous registered designs are used for two major functions: data handling and control. Registered synchronous designs for data handling include counters and shift registers. There are various types of counters. Some are; binary counters, modulo counters, Johnson counters, and Gray-code counters. These counters are differentiated by the sequence of values through which the counter travels. A binary counter is the simplest form of a counter, and is used most often for data functions. Any system requiring a regular count uses a binary counter. Modulo, Gray-code, and Johnson counters are also used for control.

All counters are actually subsets of a larger class of digital designs called state machines. State machines are discussed in detail in the next chapter of this handbook.

Counters

Counters are the most commonly used sequential circuits. A set of registers, that cycles through a predetermined, unvarying sequence, is called a counter. A general model of a synchronous counter is illustrated in Figure 5. This shows a common clock to all the flip-flops, whose outputs are fed back to a combinatorial logic array called the next-state (count) decoder. The next count is generated by this logic based upon the present

count and control inputs. Most PLDs use the standard sum-of-products form of array for this logic.

The relationship between a four-bit counter and its signal timing diagram is illustrated in Figure 6. The counters can also be represented by state diagrams (Figure 7). The state diagrams are bubble-and-arrow diagrams. Each bubble represents a count value and each arrow a transition from one count to the next. More detail on state diagrams is given in the next chapter on state machine design. For counters, the state diagrams are a convenient representation tool and will be used in the discussion when necessary.

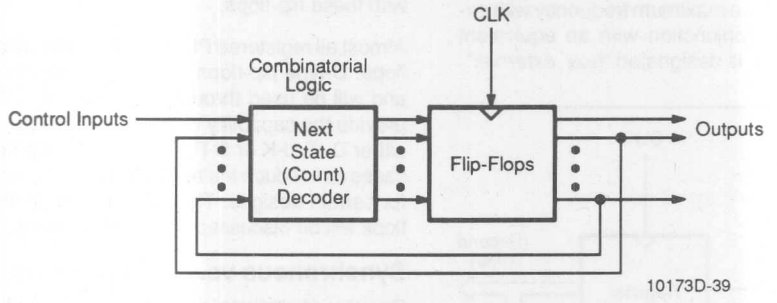


Figure 5. General Model of a Counter

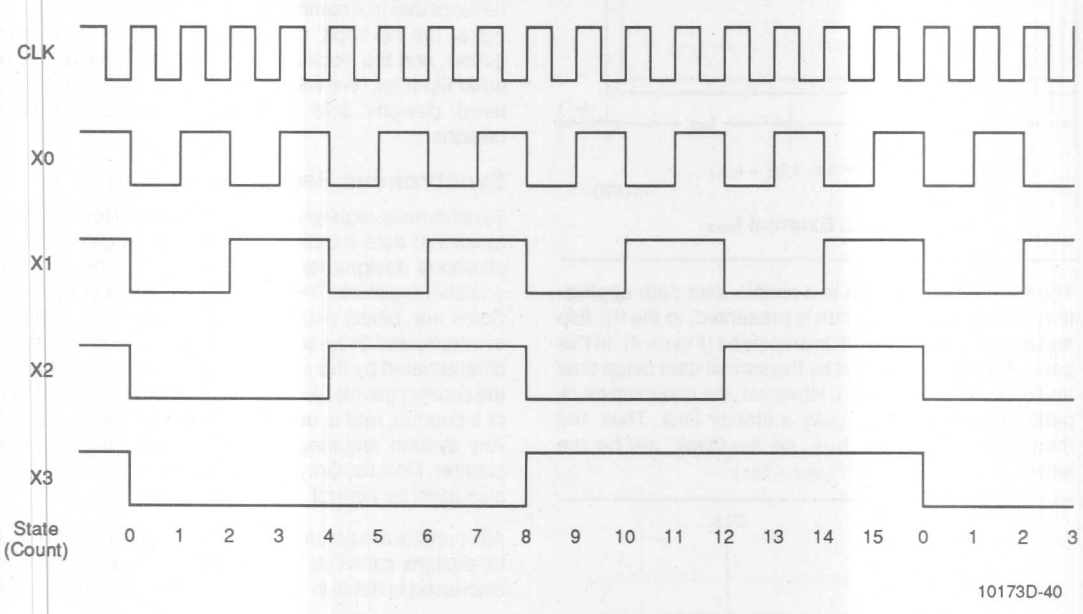


Figure 6. Timing Diagram of a Four-Bit Binary Counter

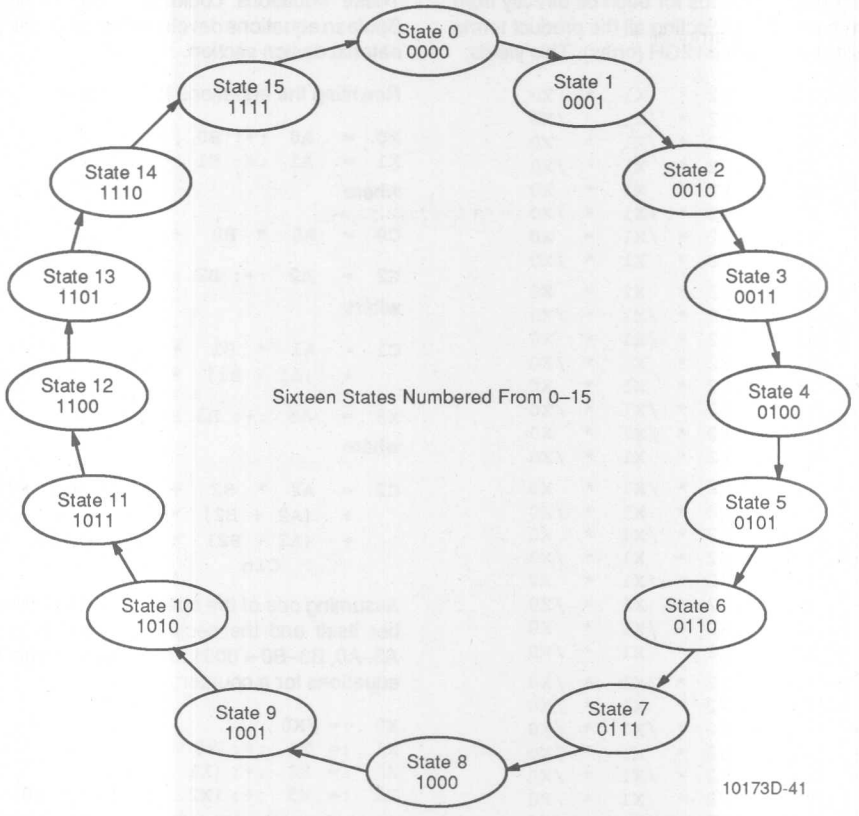


Figure 7. State Diagram of a Four-Bit Binary Counter

Binary Counters

Let us examine a four-bit binary counter. The truth table (also called the transition table) for such a counter is given in Table 1. The table lists the next state values of all the output registers based upon their present values.

Table 1. The Truth Table for a Four-Bit Binary Counter

Present State				Next State			
X3	X2	X1	X0	X3	X2	X1	X0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

We derive Boolean equations for each bit directly from the above truth table by collecting all the product terms where outputs are asserted HIGH (ones). This yields:

```
X3  :=     /X3 *  X2 *  X1 *  X0
       +    X3 * /X2 * /X1 * /X0
       +    X3 * /X2 * /X1 *  X0
       +    X3 * /X2 *  X1 * /X0
       +    X3 * /X2 *  X1 *  X0
       +    X3 *  X2 * /X1 * /X0
       +    X3 *  X2 * /X1 *  X0
       +    X3 *  X2 *  X1 * /X0

X2  :=     /X3 * /X2 *  X1 *  X0
       +   /X3 *  X2 * /X1 * /X0
       +   /X3 *  X2 * /X1 *  X0
       +   /X3 *  X2 *  X1 * /X0
       +    X3 * /X2 *  X1 *  X0
       +    X3 *  X2 * /X1 * /X0
       +    X3 *  X2 * /X1 *  X0
       +    X3 *  X2 *  X1 * /X0

X1  :=     /X3 * /X2 * /X1 *  X0
       +   /X3 * /X2 *  X1 * /X0
       +   /X3 *  X2 * /X1 *  X0
       +   /X3 *  X2 *  X1 * /X0
       +    X3 * /X2 * /X1 *  X0
       +    X3 * /X2 *  X1 * /X0
       +    X3 *  X2 * /X1 * /X0
       +    X3 *  X2 *  X1 * /X0

X0  :=     /X3 * /X2 * /X1 * /X0
       +   /X3 * /X2 *  X1 * /X0
       +   /X3 * /X2 * /X1 * /X0
       +   /X3 *  X2 *  X1 * /X0
       +    X3 * /X2 * /X1 * /X0
       +    X3 * /X2 *  X1 * /X0
       +    X3 *  X2 * /X1 * /X0
       +    X3 *  X2 *  X1 * /X0
```

These Boolean equations are for devices with active-HIGH outputs. These equations can be inverted for devices with active LOW outputs. The Boolean equations for active-LOW devices can also be directly derived from the truth table by collecting all the product terms where the active-LOW outputs (zeros) are asserted.

Manipulating the equations with Boolean algebra, we obtain the Boolean logic equations:

```
X0  := /X0
X1  := X1  :+: X0
X2  := X2  :+: (X1   * X0)
X3  := X3  :+: (X2   * X1    * X0)
```

Similarly, for active-LOW output devices (since /(A :+: B) = /A :+: B):

```
/X0 := X0
/X1 := /X1 :+: X0
/X2 := /X2 :+: (X1   * X0)
/X3 := /X3 :+: (X2   * X1    * X0)
```

These equations could also be obtained from the Boolean equations developed for an adder in the combinatorial design section.

Rewriting the equations for an adder:

```
X0  =  A0  :+: B0 :+: Cin
X1  =  A1  :+: B1 :+: C0
```

where

```
C0  =  A0  *  B0   +  (A0 + B0)   *  Cin
```

```
X2  =  A2  :+: B2 :+: C1
```

where

```
C1  =  A1  *  B1   +  (A1 + B1)  * (A0 * B0)
    +  (A1 + B1)   *  (A0 + B0)  *  Cin
```

```
X3  =  A3  :+: B3 :+: C2
```

where

```
C2  =  A2  *  B2   + (A2 + B2) *(A1 * B1)
    +  (A2 + B2)   *  (A1 + B1)  *(A0 * B0)
    +  (A2 + B2)   *  (A1 + B1)  *(A0 * B0)
       *  Cin
```

Assuming one of the operands in the adder is the number itself and the second operand is one (X3–X0 = A3–A0, B3–B0 = 0001 and Cin = 0) we get the following equations for a counter:

```
X0  := /X0
X1  := X1  :+: X0
X2  := X2  :+: (X1   *X0)
X3  := X3  :+: (X2   * X1    * X0)
```

These are, of course, the same equations as the ones derived directly from the truth table. The equations for a binary counter are very regular. The general equation for an n-bit binary counter can be directly expressed:

```
Xn := Xn :+: (Xn-1* Xn-2 ... X0)
```

For devices with active-LOW outputs, the general Boolean equations can be derived by inverting both sides of the equation:

```
/Xn := /Xn :+: (Xn-1* Xn-2 ... X0)
```

These equations represent a binary UP counter. Counting backwards for a DOWN counter, the Boolean equations can be similarly generated, either from the truth table or from the adder Boolean equations. The general equation for a DOWN counter is:

```
Xn := Xn :+: (/Xn-1* /Xn-2 ... /X0)
```

This equation is for active-HIGH outputs. For active-LOW output devices the Boolean equation for a DOWN counter is:

```
/Xn := /Xn :+: (/Xn-1* /Xn-2 ... /X0)
```

Further control functions can be added to these counter equations directly either at the truth-table stage or in the equations. For example, a load data function is required in most counters. This allows registers to be loaded with a count under the control of another input signal (LOAD). When the LOAD signal is HIGH the counter is loaded with the input data, and when the LOAD signal is LOW the counting is resumed.

Binary Counter Device Selection Considerations

One major device selection consideration is the logic requirement.

The binary counter Boolean equations make use of exclusive-OR functions in the output. In most of the registered PLDs, the XOR functions are implemented in their sum-of-products logic form. This usually requires a large number of product terms. Most standard PAL devices provide eight product terms per output. However, for larger counters, a greater number of product terms is required.

Some PLDs provide a dedicated XOR gate on the outputs. This allows an AND-OR-XOR implementation of the Boolean logic, and consequently requires fewer product terms.

Cascading Binary Counters

Situations are occasionally encountered in digital system designs where very long counters are required. Binary counters can be easily cascaded into two or more devices to construct such large counters. The design of long counters is very simple. These are designed as simple binary counters with a count enable control. The less significant counters generate an extra output signal at the penultimate count. These signals are ANDed together to form the count enable signal for the higher-order counter. For a down counter the reverse scheme is implemented.

Cascading counters is a lot easier than cascading adders because the carry-look-ahead circuitry is not required. The only thing to remember is that the more significant counter toggles only when the penultimate count of all of the less significant counters is reached.

Flip-Flop Selection

Until now, all the designs have been implemented in devices with D-type flip-flops. What happens if the counter design is implemented in a device that allows both J-K and T-type registers? The Boolean logic equations for such a design can be derived from the truth table. This requires advanced knowledge of the functionality of the J-K and T-type registers. For the J-K register the output is asserted when the J input goes HIGH and the output is unasserted when the K input goes HIGH. Toggle type registers require the T input to be asserted for every change in the output level.

Table 2. Truth Table for D, J-K and T-Type Flip-Flops

Present State				Next State															
				X3				X2				X1				X0			
X3	X2	X1	X0	D	J	K	T	D	J	K	T	D	J	K	T	D	J	K	T
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1
0	0	1	1	0	0	0	0	1	1	0	1	0	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1
0	1	0	1	0	0	0	0	1	0	0	0	1	1	0	1	0	0	1	1
0	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	1
0	1	1	1	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
1	0	0	1	1	0	0	0	0	0	0	0	1	1	0	1	0	0	1	1
1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	1	1	0	1	0	0	1	1	0	0	1	1
1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1
1	1	0	1	1	0	0	0	1	0	0	0	1	1	0	1	0	0	1	1
1	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	1
1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Table 2 shows the truth table for both a J-K and a T-type register implementation for a binary counter. Deriving and optimizing the equations from the table, we get the following results:

```
X3-J   :=  /X3  *   X2  *   X1  *   X0
X3-K   :=   X3  *   X2  *   X1  *   X0
X2-J   :=  /X2  *   X1 *X0
X2-K   :=   X2  *   X1 X0
X1-J   :=  /X1  *   X0
X1-K   :=   X1  *   X0
X0-J   :=  /X0
X0-K   :=   X0
X3-T   :=   X2  *   X1  *   X0
X2-T   :=   X1  *   X0
X1-T   :=   X0
X0-T   :=    1
```

As we can see from these equations, the number of product terms used for J-K and T-type implementations are smaller than the number of product terms required for a D-type implementation.

Which flip-flop is most efficient depends on the relative number of transitions or holds required. As a counter traverses from one count (state) to another, every output either makes a "transition" (changes logic level) or "holds" (stays at the same logic level). Small counters in general require more transitions and fewer holds. As the designs get larger, the higher-order bits require fewer transitions and more holds.

D-type flip-flops use up product terms only for active transitions from logic LOW level to HIGH level, and for logic HIGH level holds only. J-K and T-type flip-flops use up product terms for both LOW-to-HIGH and HIGH-to-LOW transitions, but eliminate hold terms. Generally, the requirements of transition and hold terms depends upon the count sequence selection. D-type flip-flops are more efficient for small designs. Conversely J-K and T-type flip-flops can be more efficient for large designs, which require more hold terms.

A comparison of product term requirements of 2-, 3-, 4- and 5-bit binary counters can be representative for other types of counters and state machines. Table 3 shows the transition terms and the hold terms required for these counters. For a J-K type flip-flop implementation, after optimizing, total product terms required are 4, 6, 8, and 10 respectively. The D-type implementation requires 3, 6, 10, and 15 respectively, and is relatively less efficient for large counters.

Table 3. Product Term Requirements for Configurable Flip-Flops

Binary Counter	Transitions	Holds	D Product Terms	J-K Product Terms	T Product Terms
2-Bit	6	2	3	4	1
3-Bit	14	10	6	6	1
4-Bit	30	34	10	8	1
5-Bit	62	98	15	10	1

Modulo Counters

The number of unique states a counter traverses is generally referred to as the modulus. A typical n-bit binary counter has a maximum modulus of 2n. It is often necessary to introduce signal delays into the logic design to meet timing requirements. This makes it possible to allow for bus-skew, access time, or differential propagation delays between devices along two different signal paths. A typical example of this is the introduction of wait states to allow for access times of different memory elements. Counters and delay lines are commonly used to introduce the delay. Counters in PLDs have the added advantage of programmability to select the required delay. Such applications where precise timing duration control is required usually use modulo counters with a non-power-of-two modulus. Other applications of modulo counters include waveform generators and arbiters.

Table 4. Truth Table for a BCD Counter

Present State					Next State			
Q3	Q2	Q1	Q0		Q3	Q2	Q1	Q0
0	0	0	0	0 -> 1	0	0	0	1
0	0	0	1	1 -> 2	0	0	1	0
0	0	1	0	2 -> 3	0	0	1	1
0	0	1	1	3 -> 4	0	1	0	0
0	1	0	0	4 -> 5	0	1	0	1
0	1	0	1	5 -> 6	0	1	1	0
0	1	1	0	6 -> 7	0	1	1	1
0	1	1	1	7 -> 8	1	0	0	0
1	0	0	0	8 -> 9	1	0	0	1
1	0	0	1	9 -> 0	0	0	0	0

A good example of a modulo counter is a BCD counter. Such a counter is useful in applications where the computer's outputs are generated using a decimal system. While a four-bit binary counter can count to sixteen, the BCD counter terminates the count at the modulus of 10.

Modulo counters can be designed in a variety of ways. One direct way is to use the truth table to implement a count to a modulus and directly derive the equations from it. The truth table for a BCD count (from zero to nine) is shown in Table 4.

Now let us consider what happens if the device accidentally powers up in one of the count values from ten to fifteen. These are illegal counts (states) and, for a good design, a mechanism must be built into the equations to allow it to recover back into a legal state. What we actually need is to consider the truth table in Table 5 in conjunction with the one in Table 4 for deriving the Boolean equations.

Table 5. Truth Table for Illegal State Recovery to Count Zero

Present State					Next State			
Q3	Q2	Q1	Q0		Q3	Q2	Q1	Q0
1	0	1	0	10 -> 0	0	0	0	0
1	0	1	1	11 -> 0	0	0	0	0
1	1	0	0	12 -> 0	0	0	0	0
1	1	0	1	13 -> 0	0	0	0	0
1	1	1	0	14 -> 0	0	0	0	0
1	1	1	1	15 -> 0	0	0	0	0

A state diagram for the BCD counter is shown in Figure 8. For active-LOW outputs, the Boolean equations can be derived directly from the truth table and optimized using Karnaugh maps or the software minimizer.

The Boolean equation for Q3 is:

```
/Q3 :=    /Q3 * /Q2 * /Q1 * /Q0
        + /Q3 * /Q2 * /Q1 *  Q0
        + /Q3 * /Q2 *  Q1 * /Q0
        + /Q3 * /Q2 *  Q1 *  Q0
        + /Q3 *  Q2 * /Q1 * /Q0
        + /Q3 *  Q2 * /Q1 *  Q0
        + /Q3 *  Q2 *  Q1 * /Q0
        +  Q3 * /Q2 * /Q1 *  Q0
        +  Q3 * /Q2 *  Q1 * /Q0
        +  Q3 * /Q2 *  Q1 *  Q0
        +  Q3 *  Q2 * /Q1 * /Q0
        +  Q3 *  Q2 * /Q1 *  Q0
        +  Q3 *  Q2 *  Q1 * /Q0
        +  Q3 *  Q2 *  Q1 *  Q0
```

The equation can be reduced to the following:

```
/Q3 :=    /Q3 * /Q2
        + /Q3 * /Q1
        + /Q2 *  Q0
        +  Q3 *  Q1
        +  Q3 *  Q2
```

Similar Boolean equations can be generated for Q2, Q12 and Q0.

Figure 9 shows the circuit diagram of a loadable dual BCD counter.

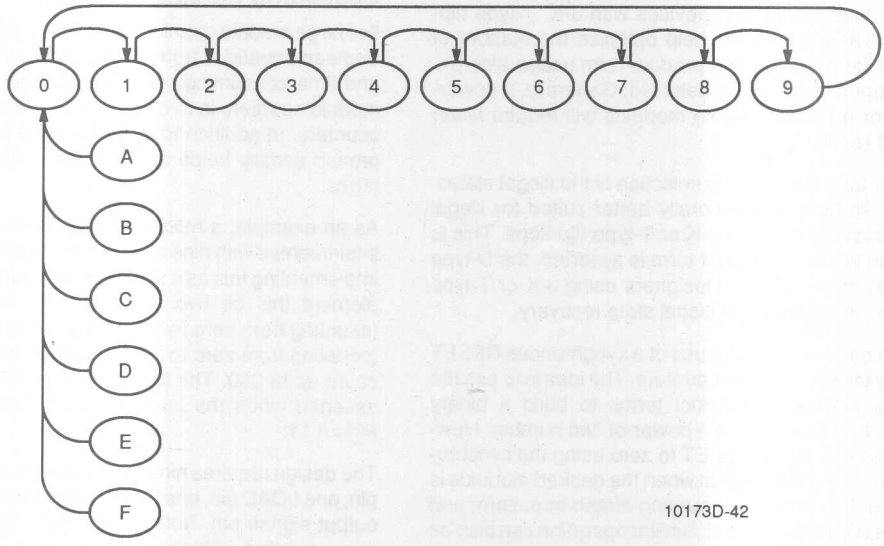


Figure 8. State Sequence of a BCD Counter Showing Illegal State Recovery

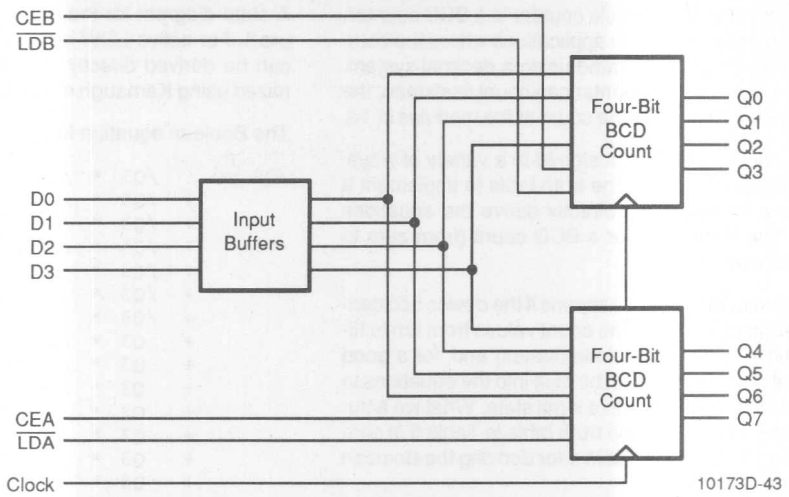


Figure 9. Circuit of a Dual BCD Counter

Modulo Counter Device Selection Considerations

We have illustrated a counter that counts from zero to a fixed modulus. The same technique can be applied for a counter which counts down from a maximum power-of-two number to a fixed modulus, or even a counter which counts from one modulus to another. The important considerations will be the number of product terms used.

The registered PLDs used for modulo counters are similar to the ones selected for other counters. Since the counts used are binary, devices with J-K, T-type flip-flops, or XOR gates will help optimize the number of product terms used. The product term usage also depends upon the modulus selected. Generally, a power-of two or a multiple-of-two modulus will require fewer product terms.

Another factor for flip-flop selection is the illegal states. D-type flip-flops are generally better suited for illegal state recovery than the J-K or T-type flip-flops. This is because when no product term is asserted, the D-type flip-flops reset to zero. Designers using J-K or T-type flip-flops must design-in illegal state recovery.

Certain devices allow the use of a synchronous RESET product term for modulo counters. The idea is to use the minimal number of product terms to build a binary counter that counts up to a power-of-two number. However, this counter is RESET to zero using the synchronous RESET product term when the desired modulus is reached. It then begins counting afresh from zero, and the procedure is repeated. Similar operation can also be achieved with a synchronous PRESET product term for a down counter.

Using synchronous RESET and PRESET product terms allows the counter to recover from illegal states. Notice that the logic product terms in the counter are designed for a complete binary count. If the counter powers up in any illegal state (as shown in Figure 10), it will continue the count until the terminal count and then, return to zero, where the correct modulo count will begin. This illegal state recovery will take an unpredictable number of clock cycles, and you may wish to design a more systematic recovery system.

Cascading Modulo Counters

For large modulo counters, the technique of generating Boolean equations from the truth tables is very tedious and time consuming. Another approach for designing modulo counters is to divide it into two smaller modulo counters. In addition to simplifying the design, this approach usually helps optimize the number of product terms.

As an example, a modulo-360 counter can be directly implemented with nine register bits. However, instead of implementing this as a straight 9-bit counter, we can implement this as two counters: one four-bit counter (counting from zero to 14) and another five-bit counter (counting from zero to 23). Together, the two counters count up to 360. The terminal count output, MOUT, is asserted when the count reaches 360, as shown in Figure 11.

The design requires nine inputs, nine outputs, one clock pin, one LOAD pin, one RESET and one MOUT (module output signal) pin. Note that no extra flip-flops or pins were needed. Obviously, the count values of this counter are not the same as a straight modulo-360 counter. Actually, this is what contributes to the optimization of the number of product terms used.

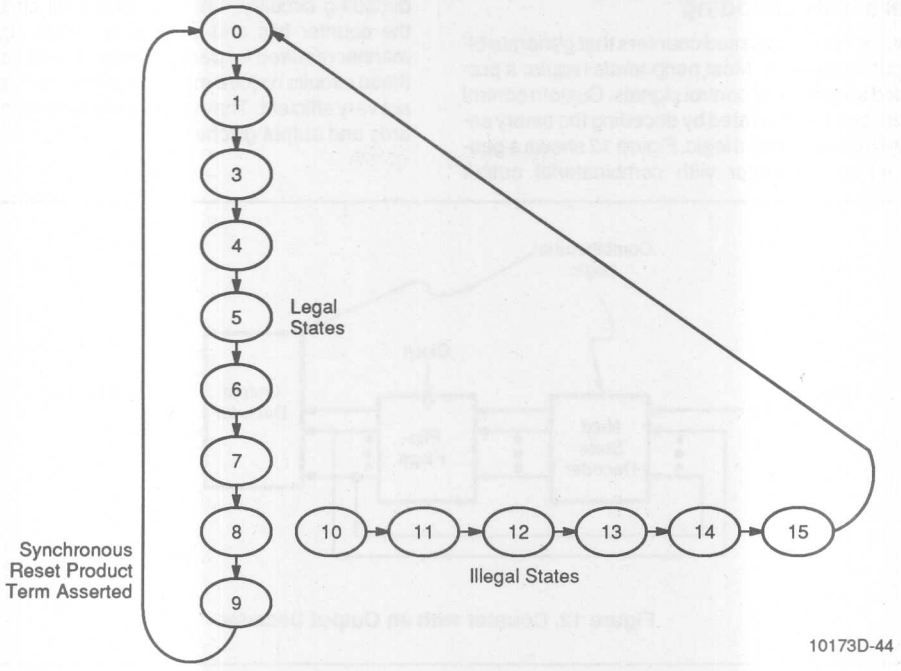


Figure 10. A BCD Counter Using Synchronous RESET Product Term

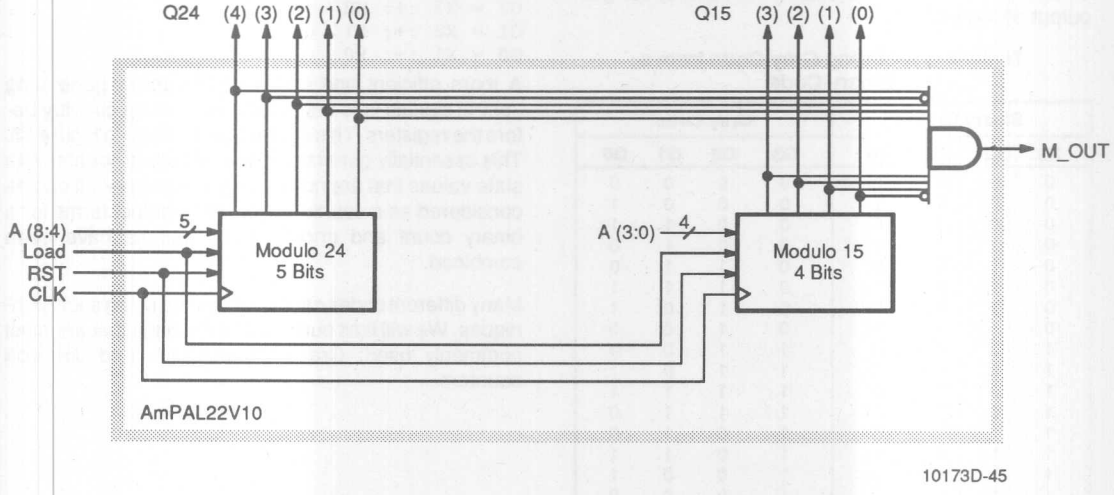


Figure 11. A Modulo-360 Counter

Counters with Encoding

Until now, we have discussed counters that generate binary output sequences. Most peripherals require a predetermined sequence of control signals. Custom control sequences can be generated by decoding the binary sequence with combinatorial logic. Figure 12 shows a general model of a counter with combinatorial output decoding circuitry. This combinatorial circuit modifies the counter bits and generates output signals in the manner required for peripheral timing and control. Since these circuits require extra combinatorial logic, they are not very efficient. They are also more susceptible to hazards and output glitches.

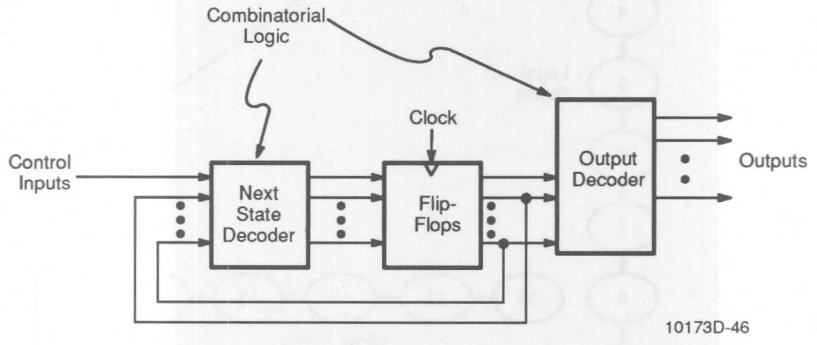


Figure 12. Counter with an Output Decoder

It is possible to have a different output coding for a four-bit counter, as shown in Table 6. This code, called Gray code, allows only one output bit to toggle for each new count value. This code can be easily derived from a four-bit binary counter code (also shown in Table 6) using an output decoder.

Table 6. Generating Gray Code from a Binary Code

Binary Code				Gray Code			
X3	X2	X1	X0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

We can derive the Boolean equations for the combinatorial output decoder from the truth table. The equations are:

```
G3 = X3
G2 = X3 :+: X2
G1 = X2 :+: X1
G0 = X1 :+: X0
```

A more efficient and easier technique for generating control signals is to implement the decode circuitry before the registers. This alternative is shown in Figure 13. This essentially generates a non-standard counter with state values that are not a binary progression. It can be considered as a counter where the product terms for a binary count and encoding the outputs have been combined.

Many different codes can be generated using such techniques. We will limit ourselves to the ones that are most commonly used: Gray-code counters and Johnson counters.

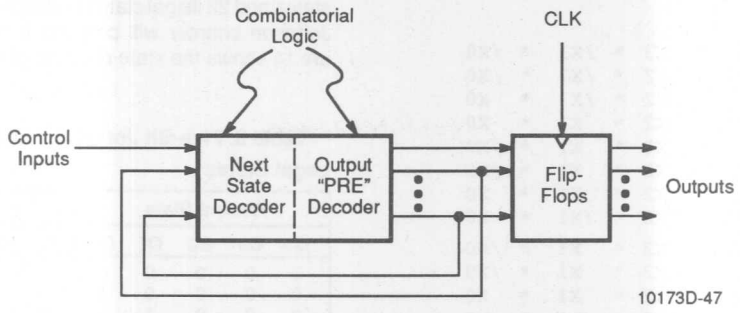


Figure 13. Counter with Combined Next State Generation and Output Encoding Circuit

Gray-Code Counters

Gray-code counters are often used in digital designs for control timing functions. The primary advantage of Gray-code counters stems from the characteristic that only one output bit changes value for every clock cycle. These output signals can be easily decoded using a combinatorial decoder without any risk of hazards. Gray-code counters are used extensively as system clocks, since the different output bits provide different clock pulses, without the risks of hazards. Gray-code is also used in high-speed data communication applications, where data is transmitted from one part of the system to another, and where the error susceptibility increases with the number of bit changes between adjacent numbers in a sequence. These are also used for such specialized applications as shaft encoders and real-time process control.

The implementation of a Gray-code counter is very simple. A truth table can be derived from the transition table as is done for a binary counter. The Boolean equations can then be directly derived from the truth table. The truth table for the Gray-code counter is shown in Table 7.

Table 7. Truth Table for a Four-Bit Gray-Code Counter

Present State				Next State			
X3	X2	X1	X0	X3	X2	X1	X0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	1	0	0	1	0
0	0	1	0	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	1
0	1	0	1	0	1	0	0
0	1	0	0	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	1
1	1	1	1	1	1	1	0
1	1	1	0	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	1
1	0	0	1	1	0	0	0
1	0	0	0	0	0	0	0

The Boolean logic equations for a Gray-code counter are:

```
X3  :=     /X3 *  X2 * /X1 * /X0
     +      X3 *  X2 * /X1 * /X0
     +      X3 *  X2 * /X1 *  X0
     +      X3 *  X2 *  X1 *  X0
     +      X3 *  X2 *  X1 * /X0
     +      X3 * /X2 *  X1 * /X0
     +      X3 * /X2 *  X1 *  X0
     +      X3 * /X2 * /X1 *  X0
X2  :=     /X3 * /X2 *  X1 * /X0
     +     /X3 *  X2 *  X1 * /X0
     +     /X3 *  X2 *  X1 *  X0
     +     /X3 *  X2 * /X1 *  X0
     +     /X3 *  X2 * /X1 * /X0
     +      X3 *  X2 * /X1 * /X0
     +      X3 *  X2 * /X1 *  X0
     +      X3 *  X2 *  X1 *  X0
X1  :=     /X3 * /X2 * /X1 *  X0
     +     /X3 * /X2 *  X1 *  X0
     +     /X3 * /X2 *  X1 * /X0
     +     /X3 *  X2 *  X1 * /X0
     +      X3 *  X2 * /X1 *  X0
     +      X3 *  X2 *  X1 *  X0
     +      X3 *  X2 *  X1 * /X0
     +      X3 * /X2 *  X1 * /X0
X0  :=     /X3 * /X2 * /X1 * /X0
     +     /X3 * /X2 * /X1 *  X0
     +     /X3 *  X2 *  X1 * /X0
     +     /X3 *  X2 *  X1 *  X0
     +      X3 *  X2 * /X1 * /X0
     +      X3 *  X2 * /X1 *  X0
     +      X3 * /X2 *  X1 * /X0
     +      X3 * /X2 *  X1 *  X0
```

Johnson Counters

A Johnson counter is part of a family of counters known as "ring counters." These counters are used for special applications where code symmetry is desired. Ring counters are also often used for timing purposes, since all the outputs are essentially a series of pulses. This code symmetry also allows use of the fewest possible product terms with a D-type register. Devices that provide a small amount of logic per cell, can implement Johnson counters very easily.

Johnson counters are also known as circular-shift counters. The sequence for a five-stage Johnson counter is shown in Table 8. As can be seen in the truth table, the counter first fills up with 1's from left to right and then it fills up with zeros again. Note from the output sequence that only one of the Johnson counter bits changes for every clock period, like the Gray-code counter. One major advantage of the Johnson counter is that it can be readily decoded with small two-input NAND gates and hence is suitable for high-speed applications.

Note that the five-stage sequence has a table of 10 legal states and 22 illegal states (Table 9). In general, an n-bit Johnson counter will produce a modulus of 2n. Figure 14 shows the state diagram of the five-bit counter.

Table 8. Five-Bit Johnson Counter Truth Table

Legal States

Present State					Next State				
Q4	Q3	Q2	Q1	Q0	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	0	0	0
0	0	0	1	1	0	0	0	0	1
0	0	1	1	1	0	0	0	1	1
0	1	1	1	1	0	0	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	0	0	1	1	1	1	0
1	1	0	0	0	1	1	1	0	0
1	0	0	0	0	1	1	0	0	0

The implementation of a Johnson counter is relatively straight-forward, and is the same regardless of the number of stages. When D-type flip-flops are used, the Q output of each flip-flop is connected to the D input of the following stage. The single exception is the Q output of the last stage, which is complemented and connected to the D input of the first stage.

Table 9. Illegal States for a Five-Bit Johnson Counter

Illegal States

Present State					Next State				
Q4	Q3	Q2	Q1	Q0	Q4	Q3	Q2	Q1	Q0
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0
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1	1	1	0	1	0	0	0	0	0

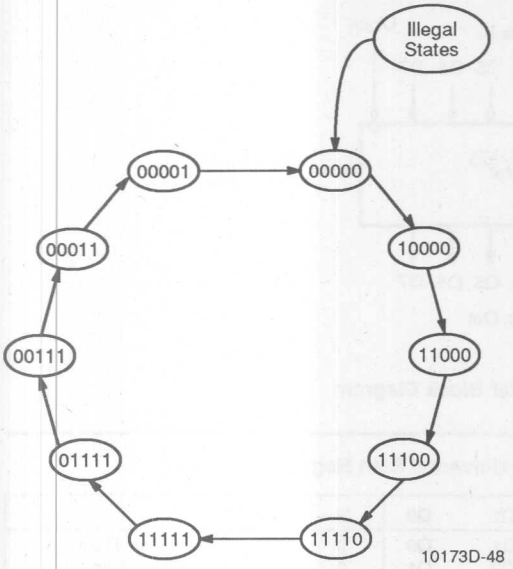


Figure 14. State Diagram of a Five-Bit Johnson Counter

One disadvantage of the counter is the number of invalid (or illegal) states. The invalid states increase exponentially with the length of the counter. The bigger the counter becomes, the greater are its chances of entering an illegal state. Johnson counters are very susceptible to illegal states, and can "hang up" very easily. Noise or improper use can cause this counter to end up in an illegal state. Therefore, a design with illegal state recovery circuitry is always recommended.

Figure 15 shows a nine-bit Johnson counter that can be derived by directly extending the design of a five-bit Johnson counter.

Shift Registers

A Shift Register is a special digital circuit often used as a primary building block in digital computer systems. It is closely related to a ring counter. Its fundamental usage is for temporary data storage and bit-wise data manipulation for advanced arithmetic and multiplication operations. Shift registers are also frequently used in communications, for converting parallel byte-wide data from the microprocessor to a serial data bit-stream for transmission. Shift registers are also used in graphics systems for serializing parallel data for use by the display monitor. A number of examples of video shift registers are included in the graphics section.

The fundamental purpose of a shift register (Figure 16) is to shift data from one flip-flop to another. There are several types of shift registers. They are classified by the way in which incoming data is received (parallel or serial), and how outgoing data is transmitted (parallel or serial).

In the following example, we will discuss a simple universal shifter that provides both serial and parallel input and output functions. Depending upon the control signals I0 and I1, the data is shifted from one flip-flop to another in the left or the right direction. These inputs also control when the new parallel data is loaded onto the registers. When shifting left or right, serial data can be received and transmitted on serial pins LIRO and RILO. Since the flip-flop outputs appear on the output pins at all times, the parallel output data is always available. The truth table is shown in Table 10.

The Boolean logic equations can be directly derived from the truth table, and are shown Figure 17.

Shift registers can be modified to suit various system design requirements. This universal shift register can be used for serial in/serial out, parallel in/parallel out, serial in/parallel out and parallel in/serial out functions.

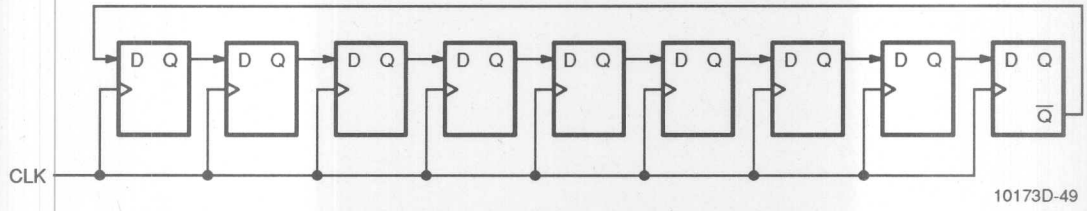


Figure 15. Block Diagram of a Nine-Bit Johnson Counter

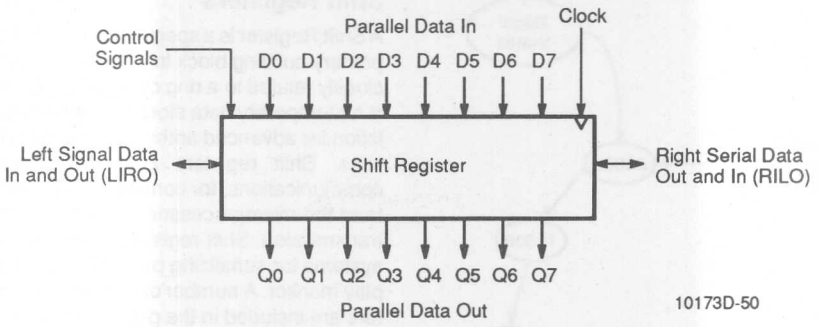


Figure 16. A Shift Register Block Diagram

Table 10. The Truth Table for a Universal Shift Register

Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	I1	I0	
Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	0	0	;Retain Data
RILO	Q7	Q6	Q5	Q4	Q3	Q2	Q1	0	1	;Shift Right
Q6	Q5	Q4	Q3	Q2	Q1	Q0	LIRO	1	0	;Shift Left
D7	D6	D5	D4	D3	D2	D1	D0	1	1	;Load Data

```
Equations
/Q0   :=     /I1*/I0*/Q0              ;HOLD Q0
      +      /I1*I0*Q1                ;SHIFT RIGHT
     :+:      I1*/I0*/LIRO            ;SHIFT LEFT
      +       I1*I0*/D0               ;LOAD D0
/Q1   :=     /I1*/I0*/Q1              ;HOLD Q1
      +      /I1*I0*/Q2               ;SHIFT RIGHT
     :+:      I1*/I0*/Q0              ;SHIFT LEFT
      +       I1*I0*/D1               ;LOAD D1
/Q2   :=     /I1*/I0*/Q2              ;HOLD Q2
      +      /I1*I0*/Q3               ;SHIFT RIGHT
     :+:      I1*/I0*/Q1              ;SHIFT LEFT
      +       I1*I0*/D2               ;LOAD D2
/Q3   :=     /I1*/I0*/Q3              ;HOLD Q3
      +      /I1*I0*/Q4               ;SHIFT RIGHT
     :+:      I1*/I0*/Q2              ;SHIFT LEFT
      +       I1*I0*/D3               ;LOAD D3
/Q4   :=     /I1*/I0*/Q4              ;HOLD Q4
      +      /I1*IO*/Q5               ;SHIFT RIGHT
     :+:      I1*/I0*/Q3              ;SHIFT LEFT
      +       I1*I0*/D4               ;LOAD D4
/Q5   :=     /I1*/I0*/Q5              ;HOLD Q5
      +      /I1* I0*/Q6              ;SHIFT RIGHT
     :+:      I1*/I0*/Q4              ;SHIFT LEFT
      +       I1* I0*/D5              ;LOAD D5
/Q6   :=     /I1*/I0*/Q6              ;HOLD Q6
      +      /I1*I0*/Q7               ;SHIFT RIGHT
     :+:     I1*/I0*/Q5               ;SHIFT LEFT
      +      I1*I0*/D6                ;LOAD D6
/Q7   :=     /I1*/I0*/Q7              ;HOLD Q7
      +      /I1*I0*/RILO             ;SHIFT RIGHT
     :+:     I1*/I0*/Q6               ;SHIFT LEFT
      +      I1*I0*/D7                ;LOAD D7
             /LIRO = /Q0              ;LEFT IN RIGHT OUT
             LIRO.TRST = /I1*I0
             /RILO = /Q7              ;RIGHT IN LEFT OUT
             RILO.TRST = I1*/I0
```

Figure 17. Boolean Logic Equations for an Octal Shift Register

Barrel Shifters

In most data processing systems, some form of data shifting or rotation is necessary. In typical computer systems, the shifter is located at the output of the ALU, and usually requires a single-cycle shift and add function (Figure 18). For such applications as floating-point arithmetic or string manipulation, ordinary shift registers are inefficient, since they require n clock cycles for an n-bit shift.

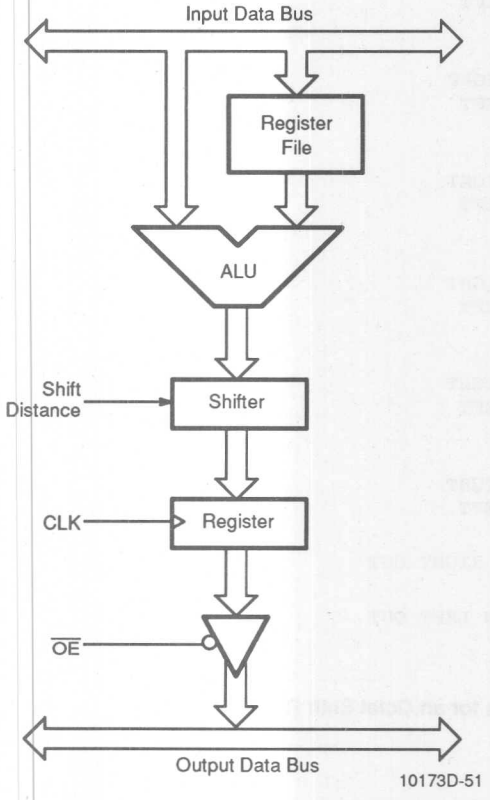


Figure 18. Typical ALU Architecture

A specialized shift register, called a "barrel shifter," is used to shift (or rotate) data by any number of bits in a single clock cycle. The name "barrel shifter" is used because of the circular nature of the shift operation. The storage registers on the output of the shifter are used in this architecture to pipeline the data operation, increasing throughput. The three-state buffer on the output registers is also useful for providing an interface to the data bus.

The design of a barrel shifter proceeds in the same manner as a regular shift register. The truth table is drawn, and the Boolean equations are then written based upon the truth tables. An eight-bit barrel shifter requires at least eight data inputs, eight registered data outputs, three control lines to specify the shift distance, a clock input and an output enable that controls the three-state buffer on the register output.

Figure 19 shows the block diagram for an eight-bit registered barrel shifter, while Table 11 shows the truth table. The registered barrel shifter requires a total of 14 inputs and 8 outputs.

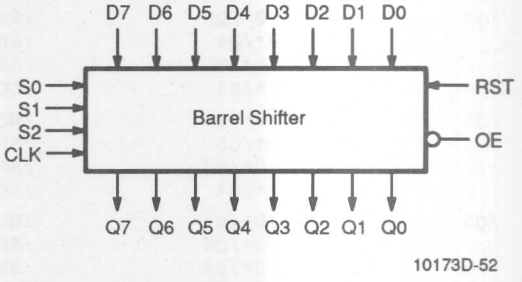


Figure 19. Block Diagram of an Eight-Bit Barrel Shifter

Table 11. Truth Table for an Eight-Bit Barrel Shifter

S2	S1	S0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	D6	D5	D4	D3	D2	D1	D0	D7
0	1	0	D5	D4	D3	D2	D1	D0	D7	D6
0	1	1	D4	D3	D2	D1	D0	D7	D6	D5
1	0	0	D3	D2	D1	D0	D7	D6	D5	D4
1	0	1	D2	D1	D0	D7	D6	D5	D4	D3
1	1	0	D1	D0	D7	D6	D5	D4	D3	D2
1	1	1	D0	D7	D6	D5	D4	D3	D2	D1

Gray-Code, Johnson Counter and Shift Register Device Selection Considerations

Gray-code counters, Johnson counters and shift registers are not very logic-intensive; the number of product terms required is minimal. The D-type flip-flops provide the most efficient implementations, allowing these designs to be easily implemented in most PAL devices.

Since Gray-code counters are often used as system clocks, very high speed PAL devices provide the highest resolution clocks.

Barrel shifters are very logic-intensive and require many product terms, since data from all the inputs needs to be accessible at any output. Registered PLDs with a large number of product terms are ideal for barrel shifters. Large barrel shifters can also be partitioned into a number of PLDs.

Asynchronous Registered Designs

Until now, we have discussed strictly synchronous registered designs, where a common system clock is used. In asynchronous registered designs, a common clock is not used. The register clock may be generated by the output of another register, or by a logical combination of various other signals. Such designs are usually slow for such applications as timing generation, because when the output of one register is used to clock another, multiple delays are encountered before all the register outputs stabilize. On the other hand, designs can be very fast for asynchronous applications such as bus arbitration and control, where a fast response to a bus signal can be provided without waiting for a common system clock.

Although asynchronous designs are easier to visualize, they present larger problems in implementation. Combinatorial hazard conditions can cause false clocking of registers, destroying the logic intended by the designer. The designer also needs to worry about race conditions when clocking a number of register simultaneously. Careful design analysis is strongly recommended before implementing any asynchronous design.

Ripple counters are probably the easiest examples of such asynchronous designs. Figure 31 shows the logic diagram of a five-bit binary ripple counter. These counters clearly have the advantage of design simplicity. The output from one stage is fed as the clock to the next stage. However, this results in a slower counting rate, since the clock signals need to propagate through all five registers before the next count is reached.

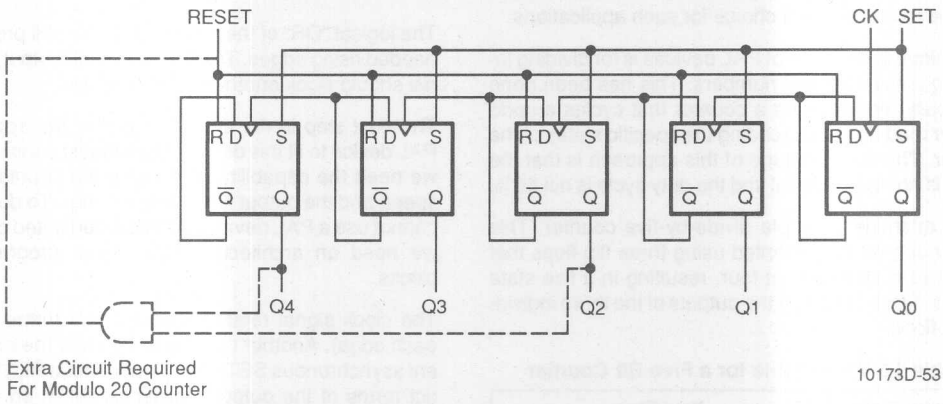


Figure 20. A Five-Bit Ripple Counter

Figure 20 shows the implementation of a modulo-20 counter that is RESET when output bits Q4 and Q2 are both HIGH. Since the RESET is implemented with a product term, the extra AND gate shown can be implemented directly within the PAL device.

Asynchronous Designs Device Selection Considerations

The device selection for asynchronous designs is easy. As the clock signals require logic, only PLDs that allow implementations of Boolean logic on the clock signals are useful.

OTHER APPLICATIONS OF REGISTERED PLDs

Registered PLDs are used for a number of miscellaneous applications that are not covered by the synchronous and asynchronous design applications discussed up to now. One such application is as a frequency divider.

- Frequency dividers
- Addressable Registers

Frequency Dividers

Standard synchronous counters provide the basic capability of dividing an input frequency. A single register of a PAL device will let us divide by two.

If we stack these registers, a binary counter provides symmetrical division by 2, 4, 8, 16, etc. This divider has been a standard for years, and the PAL device has always been on excellent choice for such applications.

One unique application of PAL devices is for dividing input frequencies by odd numbers. This has been done historically by designing a counter that cycles an odd number modulo, and decoding the specific states of the counter. The disadvantage of this approach is that the output is not symmetrical and the duty cycle is not 50%.

Let us examine a simple divide-by-five counter. This counter can be implemented using three flip-flops that start at zero and reset at four, resulting in a five-state counter. Table 12 shows the outputs of the three individual flip-flops.

Table 12. Truth Table for a Five-Bit Counter

Present State			Next State			
Q2	Q1	Q0	Q2	Q1	Q0	
0	0	0	0	0	1	State zero to one.
0	0	1	0	1	0	State one to two.
0	1	0	0	1	1	State two to three.
0	1	1	1	0	0	State three to four.
1	0	0	0	0	0	State four to zero.

The Boolean equations are:

```
Q2  := /Q2   * Q1   * Q0    ;MSB bit
Q1  := /Q1   * Q0   + Q1  * /Q0
Q0  := /Q2   */Q0           ;LSB bit
```

The waveforms for this divider are shown in Figure 21. Notice that the Q2 output goes HIGH for one state and that this output is one fifth of the input frequency, but it is a 20% duty cycle. Q1 is active for two states; it provides the same frequency, but with a 40% duty cycle. If we want a 50% duty cycle, we are going to have to divide a state in half.

To provide the 50% duty cycle, the two edges should be evenly spaced in the count sequence, one edge in the middle of state two and one at the beginning of state zero. The first edge can be formed by logically "ANDing" state_2 with the falling edge of the clock. The second edge can be formed by decoding state zero.

```
edge_1 =/clock */Q2 * Q1*/Q0
                     ;edge between
                     ;states two and
                     ;three
edge_2= /Q2 */Q1 */Q1 ;edge at state
                     ;zero
```

The logical "OR" of these two equations will provide the needed rising edges. To provide a clean output, this signal should clock another output register.

The next step in the design is to pick the appropriate PAL device to fit this design. Our biggest concern is that we need the capability of clocking the counter at one speed and the output flip-flop at another. To do this, we cannot use a PAL device that has a dedicated clock pin; we need an architecture that allows programmable clocks.

The clock signal requires two product terms (one for each edge). Another technique is to use the independent asynchronous SET and asynchronous RESET product terms of the output register. A HIGH on the SET product term asserts the register output, and a HIGH on the RESET product term unasserts the register output. Due to the asynchronous nature of the product terms some adjustment in timing is required. The SET product term is asserted when in state 0 (Q2=0, Q1=0 and Q0=0), and the RESET product term is asserted when between states two and three.

```
OUTPUT.SET = /clock * /Q2 * Q1 * /Q0
                              ;set between
                              ;states 2 & 3
OUTPUT.RESET = /Q2 */Q1 * /Q0
                              ;reset at
                              ;state zero
```

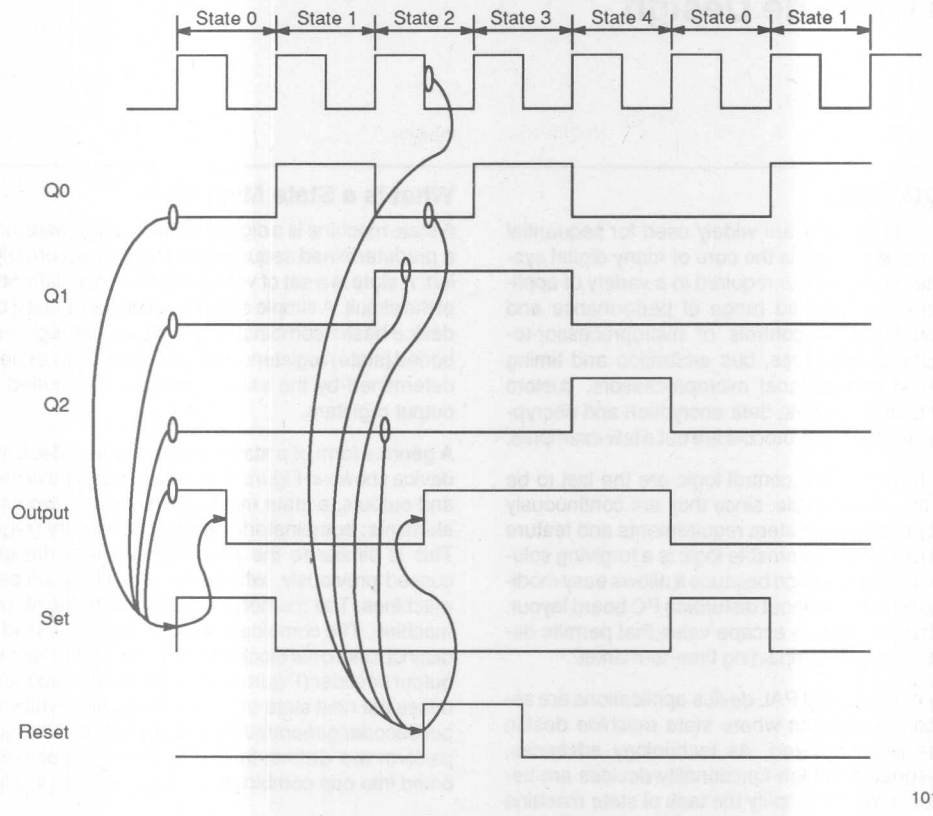


Figure 21. Waveform for a Frequency Divider

Addressable Registers

Addressable registers are commonly-used MSI functions, often implemented in PAL devices. Addressable registers are used as building blocks for digital computers. Depending upon the address input one of the many flip-flops in the register retain their previous values.

State Machine Design

INTRODUCTION

State machine designs are widely used for sequential control logic, which forms the core of many digital systems. State machines are required in a variety of applications covering a broad range of performance and complexity; low-level controls of microprocessor-to-VLSI-peripheral interfaces, bus arbitration and timing generation in conventional microprocessors, custom bit-slice microprocessors, data encryption and decryption, and transmission protocols are but a few examples.

Typically, the details of control logic are the last to be settled in the design cycle, since they are continuously affected by changing system requirements and feature enhancements. Programmable logic is a forgiving solution for control logic design because it allows easy modifications to be made without disturbing PC board layout. Its flexibility provides an escape valve that permits design changes without impacting time-to-market.

A majority of registered PAL device applications are sequential control designs where state machine design techniques are employed. As technology advances, new high-speed and high-functionality devices are being introduced which simplify the task of state machine design. A broad range of different functionality-and-performance solutions are available for state machine design. In this discussion we will examine the functions performed by state machines, their implementation on various devices, and their selection.

What Is a State Machine?

A state machine is a digital device that traverses through a predetermined sequence of states in an orderly fashion. A state is a set of values measured at different parts of the circuit. A simple state machine can consist of PAL-device based combinatorial logic, output registers, and buried (state) registers. The state in such a sequencer is determined by the values stored in the buried and/or output registers.

A general form of a state machine can be depicted as a device shown in Figure 1. In addition to the device inputs and outputs, a state machine consists of two essential elements: combinatorial logic and memory (registers). This is similar to the registered counter designs discussed previously, which are essentially simple state machines. The memory is used to store the state of the machine. The combinatorial logic can be viewed as two distinct functional blocks: the next state decoder and the output decoder (Figure 2). The next state decoder determines the next state of the state machine while the output decoder generates the actual outputs. Although they perform two distinct functions, these are usually combined into one combinatorial logic array as in Figure 1.

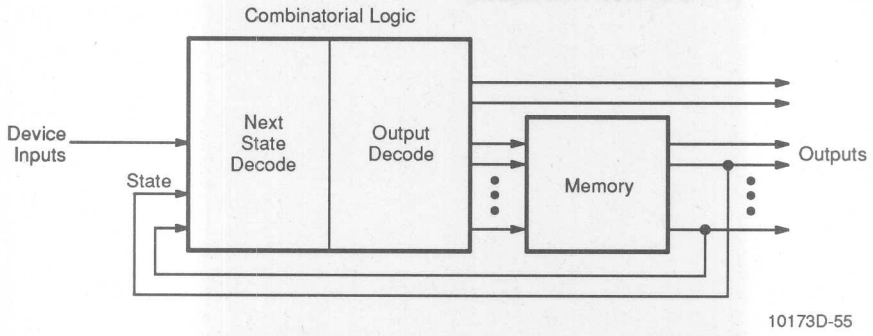


Figure 1. Block Diagram of a Simple State Machine

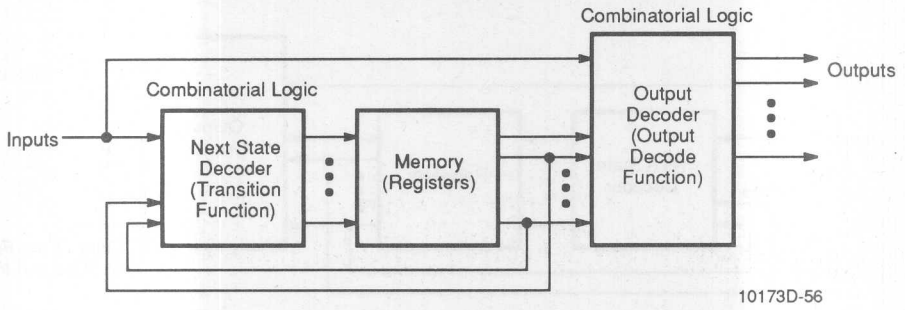


Figure 2. State Machine, with Separate Output and Next State Decoders

The basic operation of a state machine is twofold:

1. It traverses through a sequence of states, where the next state is determined by next state decoder, depending upon the present state and input conditions.
2. It provides sequences of output signals based upon state transitions. The outputs are generated by the output decoder based upon present state and input conditions.

Using input signals for deciding the next state is also known as branching. In addition to branching, complex sequencers provide the capability of repeating sequences (looping) and subroutines. The transitions from one state to another are called *control sequencing* and the logic required for deciding the next states is called the *transition function* (Figure 2).

The use of input signals in the decision-making process for *output generation* determines the type of a state machine. There are two widely known types of state machines: Mealy and Moore (Figure 3). Moore state machine outputs are a function of the present state only. In the more general Mealy-type state machines, the outputs are functions of both the state and the input signals. The logic required is known as the *output function*. For either type, the control sequencing depends upon both states and input signals.

Most practical state machines are synchronous sequential circuits that rely on clock signals to trigger the state transitions. A single clock is connected to all of the state and output edge-triggered flip-flops, which allows a state change to occur on the rising edge of the clock. Asynchronous state machines are also possible, which utilize the propagation delay in combinatorial logic for the memory function of the state machine. Such machines are highly susceptible to hazards, hard to design and are seldom used. In our discussion we will focus solely on sequential state machines.

State Machine Applications

State machines are used in a number of system control applications. A sampling of a few of the applications, and how state machines are applied, is described below.

As sequencers for digital signal processing (DSP) applications, state machines offer speed and sufficient functionality without the overkill of complex microprocessors. For simple algorithms, such as those involved in performing a Fast Fourier Transform (FFT), a state machine can control the set of vectors that are multiplied and added in the process. For complex DSP operations, a programmable DSP may be better. On the other hand, the programmable DSP solution is not likely to be as fast as the dedicated hardware approach.

Consider the case of a video controller. It generates addresses for scanning purposes, using counters with various sequences and lengths. Instead of implementing these as actual counters, the sequences involved can be "unlocked" and implemented, instead, as state machine transitions. There is an advantage beyond mere economy of parts. A count can be set or initiated, then left to take care of itself, freeing the microprocessor for other operations.

In peripheral control the simple state machine approach can be very efficient. Consider the case of run-length-limited (RLL) code. Both encoding and decoding can be translated into state machines, which examine the serial data stream as it is read, and generate the output data.

Industrial control and robotics offer further areas where simple control functions are required. Such tasks as mechanical positioning of a robot arm, simple decision making, and calculation of a trigonometric function, usually does not require the high-power solution of microprocessors with stacks and pointers. Rather, what is required is a device that is capable of storing a limited number of states and allows simple branching upon conditions.

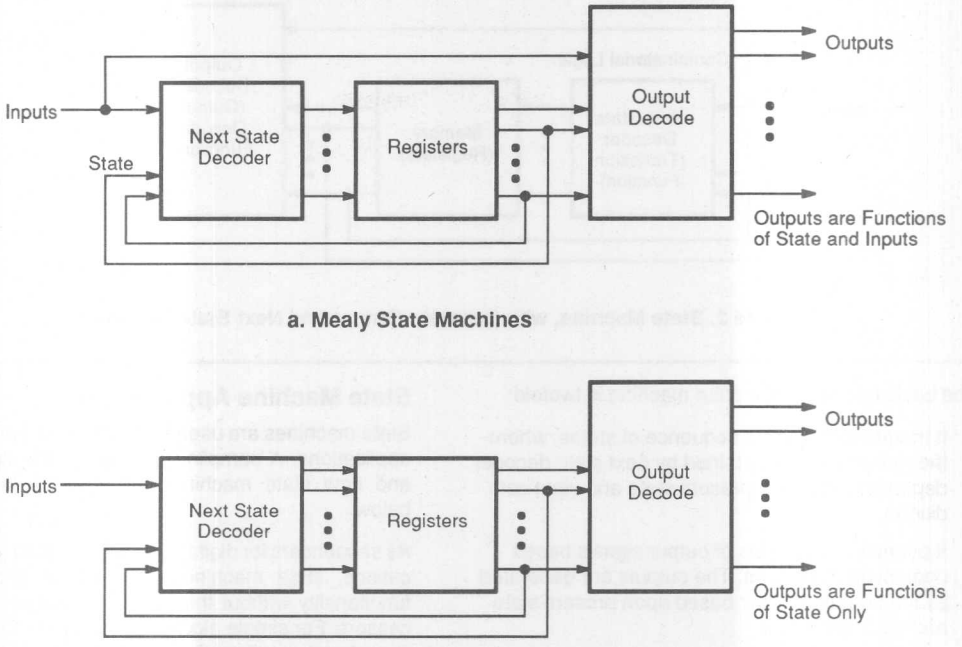


Figure 3. The Two Standard State Machine Models

Data encryption and decryption present similar problems to those encountered in encoding and decoding for mass media, only here it is desirable to make the scheme not so obvious. A programmable state machine device with a security Bit is ideal for this because memory is internally programmed and cannot be accessed by someone tampering with the system.

Functions Performed

All the system design functions performed by controllers can be categorized as one of the following state machine functions:

- Arbitration
- Event monitoring
- Multiple condition testing
- Timing delays
- Control signal generation

Later we will take a design example and illustrate how these functions can be used when designing a state machine.

State Machine Theory

Let us take a brief look at the underlying theory for all sequential logic systems, the *finite state machine* (FSM), or simply state machine.

Those parts of digital systems whose outputs depend on their past inputs as well as their current ones can be modeled as finite state machines. The "history" of the machine is summed up in the value of its internal state. When a new input is presented to the FSM, an output is generated which depends on this input and the present state of the FSM, and the machine is caused to move into new state, referred to as the next state. This new state also depends on both the input and present state. The structure of an FSM is shown pictorially in Figure 2. The internal state is stored in a block labeled "memory." As discussed earlier, two combinatorial functions are required: the transition function, which generates the value of the next state, and the output function, which generates the state machine output.

State Diagram Representation

The behavior of an FSM may be specified in graphical form as shown in Figure 4. This is called a state diagram, or state transition diagram. Each bubble represents a state, and each arrow represents a transition between states. Inputs that cause the transitions are shown next to each transition arrow.

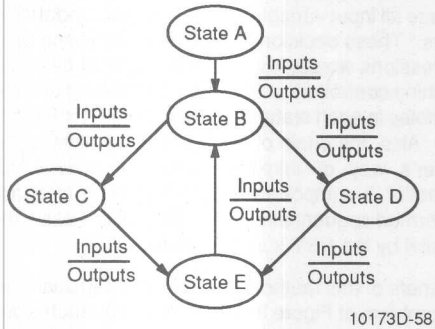


Figure 4. State Machine Representation

Control sequencing is represented in the state transition diagram as shown in Figure 5. Direct control sequencing requires an unconditional transition from state A to state B. Similarly conditional control sequencing shows a conditional transition from state C to either state D or state E, depending upon input signal I1.

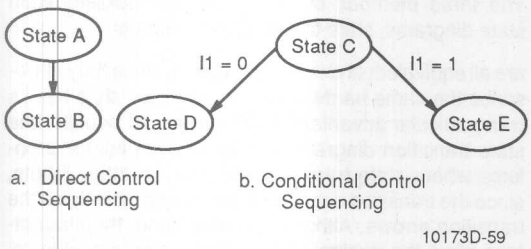


Figure 5. Control Sequencing

For Moore machines the output generation is represented by assigning outputs with states (bubbles) as shown in Figure 6. Similarly, for Mealy machines conditional output generation is represented by assigning outputs to transitions (arrows), as was shown in Figure 4. More detail on Mealy and Moore output generation is given later.

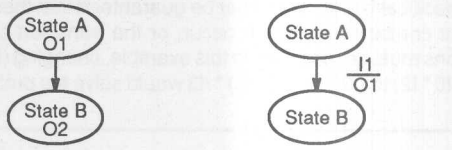


Figure 6. Output Generation

For this notation, there is a specification uncertainty as to which signals are outputs or inputs, as they both occur on the drawing next to the arrow in which they are active. This is usually resolved by separating the input and output signals names with a line (Figures 4 and 6). Sometimes an auxiliary pin list detailing the logic polarity and input or output designations is also used.

State transition diagrams can be made more compact by writing on the transitions not the input values that cause the transition, as in Figure 4, but a Boolean expression defining the input combination or combinations that cause this transition. For example, in Figure 7, some transitions have been shown for a machine with inputs START, X1, and X2. In the transition between states 1 and 2, the inputs X1 and X2 are ignored (that is, they are "don't cares") and thus do not appear on the diagram. This saves space and makes the function more obvious.

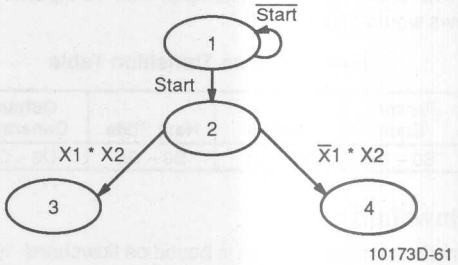


Figure 7. State Transition Diagram with Mnemonics

There can be a problem with this method if one is careless. The state transitions in figure 8 show what can happen. There are three input combinations, (I0, I1, I2, I3) = {1011}, {1101} and {1111}, which make both (/I0 * /I2 + I3) and (I0 * I1 + I0 * I2) true. Since a transition to two next states is impossible, this is an error in the

specification. It must either be guaranteed that these input combinations never occur, or the transition conditions must be modified. In this example, changing (I0 * I1 + I0 * I2) to (I0 * I1 + I0 * I2) * /I3 would solve the problem.

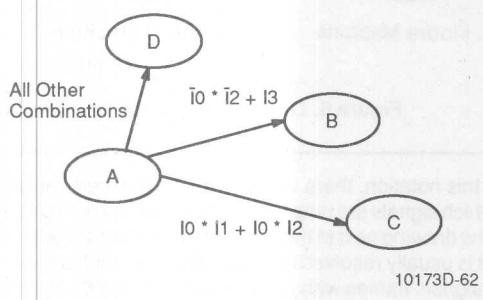


Figure 8. State Diagram with Conflicting Branch Conditions

State Transition Table Representation

A second method for state machine representation is the tabular form known as the state transition table, which has the format shown in Table 1. Listed along the top are all the possible input bit combinations and internal states. Each row gives the next state and the next output; thus, the table specifies the transition and output functions. However, this type of table is not suitable for specifying practical machines in which there is a large number of inputs, since each input combination defines a row of the table. For example, with 10 inputs, 1024 rows would be required!

Table 1. A State Transition Table

Present State	Inputs	Next State	Outputs Generated
S0 – Sn	I0 – Im	S0 – Sn	O0 – Op

Flowcharts

Another popular notation is based on flowcharts. In this notation, states are represented by rectangular boxes, and alternative state transitions are determined by strings of diamond-shaped boxes. The elements may have multiple entry points, but in general have only one exit. The state name is written as the first entry in the rectangular state box. Any Moore outputs present are written next in the state box, with a caret (^) following those that are unregistered. The state code assignment, if it is known, is written next to the upper right corner of the state box. Decision boxes are diamond or hexagonal shaped boxes containing either an input signal or a logic expression. Two exits labeled "0" and "1" lead to either another decision box, a state box, or a Mealy output. The rounded oval is used for Mealy machine outputs. Again, a caret follows those outputs that are unregistered. All the boxes may need to be expanded to accommodate a number of output signals or a larger expression.

The use of these symbols is shown in Figure 9. Each path, through the decision boxes from one state to another defines a particular combination or set of combinations of the input variables. A path does not have to include all input variables; thus, it accommodates "don't cares." These decision trees take more space than the expressions would, but in many practical cases, state machine controllers only test a small subset of the input variables in each state and the trees are quite manageable. Also, the chain of decisions often mirrors the designer's way of thinking about the actions of the controller. It is important to note that these tests are not performed sequentially in the FSM; all are performed in parallel by the FSM's state transition logic.

A benefit of this method of specifying transitions is that the problem of Figure 8 can be avoided. Such a conflict would be impossible as one path cannot diverge to define paths to two states.

This flowchart notation can be compacted by allowing more complex decisions, when there is no danger of conflicts due to multiple next states being defined, Expressions can be tested, as shown in Figure 10a, or multiple branches can extend from a decoding box, as in Figure 10b. In the second case, it is convenient to group the set of binary inputs into a vector, and branch on different values of this vector.

The three methods of state machine representation state diagrams, state tables, and flowcharts

are all equivalent and interchangeable, since they all describe the same hardware structure. Each style has its own particular advantages. Although most popular, the state transition diagrams are more complex for problems where state transitions depend on many inputs, since the transition conditions are written directly on the transition arrows. Although cumbersome, the state tables allow the designer tight control over signal logic. Flowcharts are convenient for small problems where there are not more than about ten states and where up to two or three inputs or input expressions are tested in each state. For larger problems, they can become ungainly.

Once a state machine is defined, it must be implemented on a device. Software packages are then used to implement the design on a device. The task is to convert the state machine description into transition and output functions. Software packages also account for device-specific architectural variations and limitations, to provide a uniform user interface.

Some software packages accept all three different state machine representations directly as design inputs. However, the most prevalent design methodology is to convert the three state machine design representations to a simple textual representation. Textual representations are accepted by most software packages although the syntax varies.

Since the most common of all state machine representations is the state transition diagram representation, we will use it in all subsequent discussions. Transition table and flowchart representation implementations will be very similar.

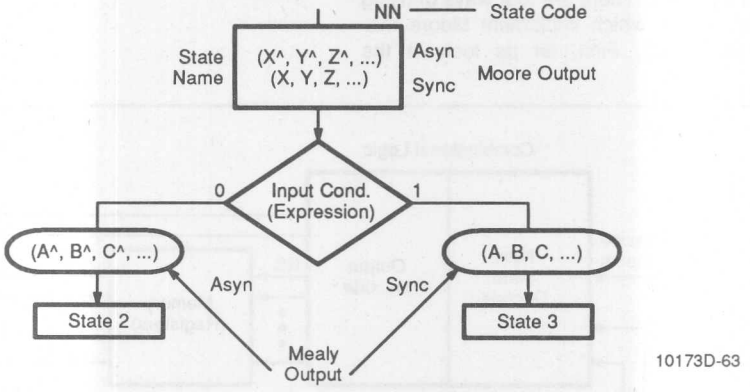
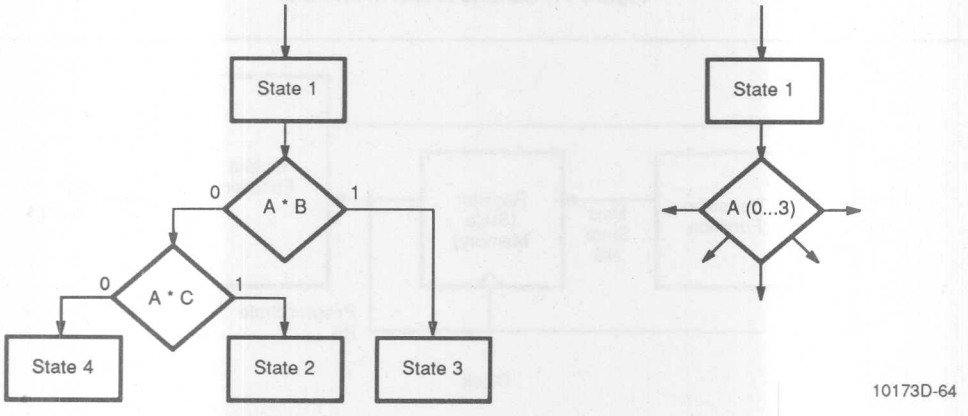


Figure 9. Flowchart Notation



a. Testing Expressions **b. Multiway Branch**

Figure 10. Using Flowcharts

State Machine Types: Mealy & Moore

With the state machine representation clarified, we can now return to the generic sequencer model of Figure 1, which has been labeled (Figure 11) to show the present state (PS), next state (NS), and output (OB, OA). This will illustrate how Mealy and Moore machines are implemented with most sequencer devices that provide a single combinatorial logic array for both next state and output decode functions. There are four ways of using the sequencer, two of which implement Moore machines and two Mealy. First, let us look at the Mealy forms.

The standard Mealy form is shown in Figure 12, where the signals are labeled as in Figure 11 to indicate which registers and outputs are used. The register outputs PS are fed back into the array and define the present state. The combinatorial logic implements the transition function, which produces the next state flip-flop inputs NS, and the output function, which produces the machine output OB. This is the asynchronous Mealy form.

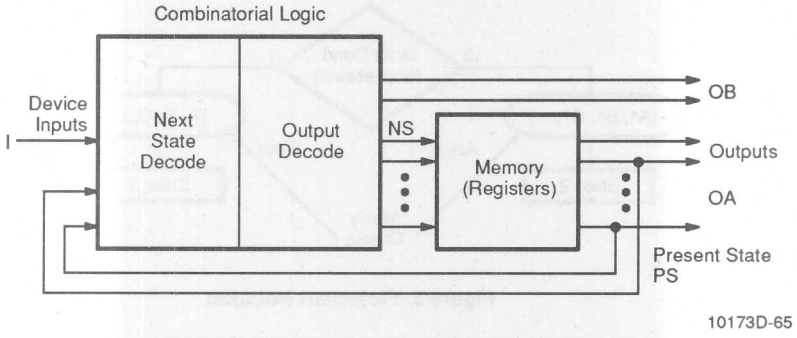


Figure 11. Generic Model of an FSM

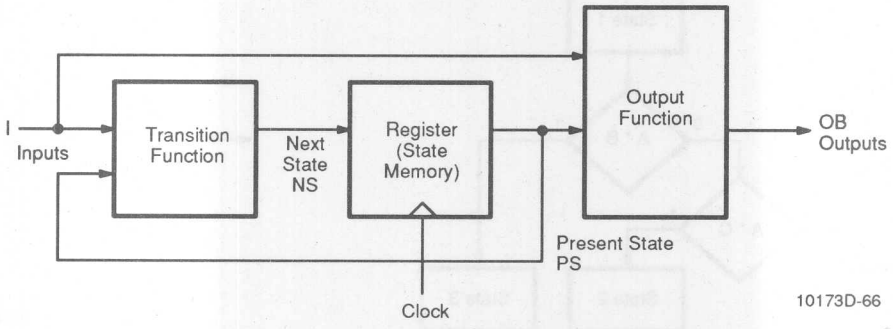


Figure 12. Asynchronous Mealy Form

An alternative Mealy form is shown in Figure 13. Here the outputs are passed through an extra output register (OA) and thus, do not respond immediately to input changes. This is the synchronous Mealy form.

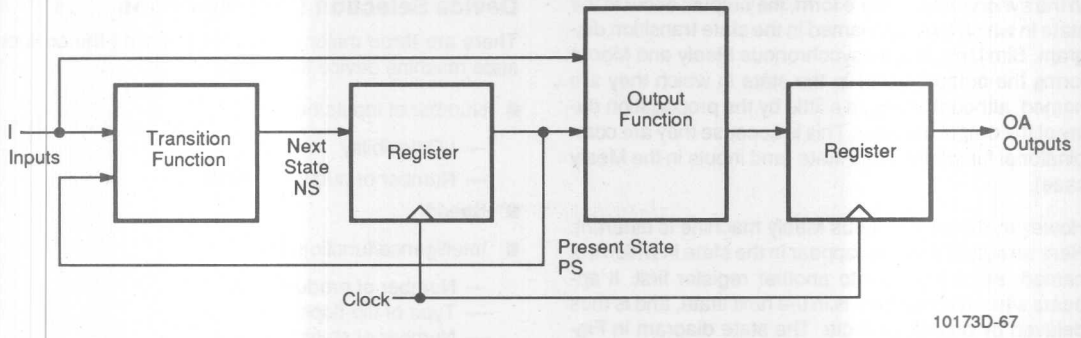


Figure 13. Synchronous Mealy Form

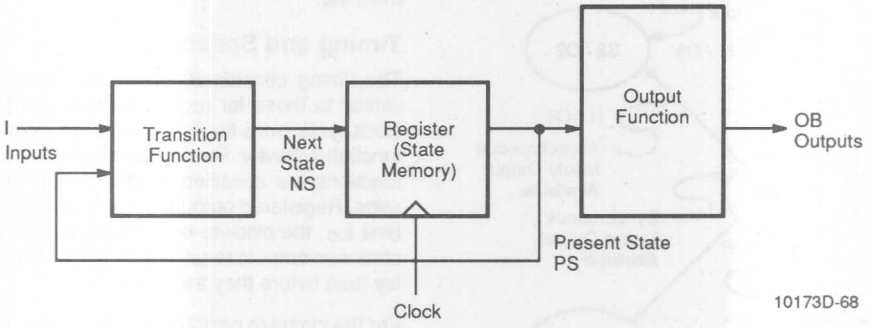


Figure 14. Asynchronous Moore Form

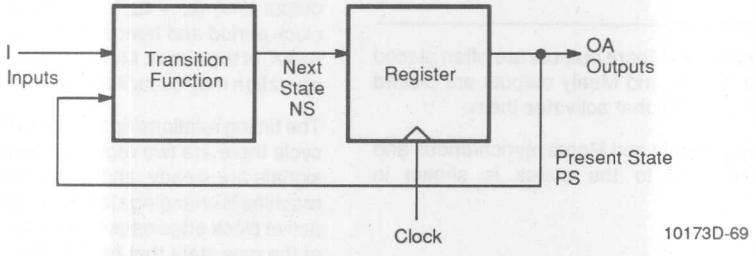


Figure 15. Synchronous Moore Form

The standard Moore form is given in Figure 14. Here the outputs OB depend only on the present state PS. This is the asynchronous Moore form. The synchronous Moore form is shown in Figure 15. In this case the combinatorial logic can be assumed to be the unity function. The outputs (OB) can be generated directly along with the present state (PS). Although these forms have been described separately, a single sequencer is able to realize a machine that combines them, provided that the required paths exist in the device.

In the synchronous Moore form, the outputs occur in the state in which they are named in the state transition diagram. Similarly, in the asynchronous Mealy and Moore forms the outputs occur in the state in which they are named, although delayed a little by the propagation delay of the output decoder. This is because they are combinatorial functions of the state (and inputs in the Mealy case).

However, the synchronous Mealy machine is different. Here an output does not appear in the state in which it is named, since it goes into another register first. It appears when the machine is in the next state, and is thus delayed by one clock cycle. The state diagram in Figure 16 illustrates all the possibilities on a state transition diagram.

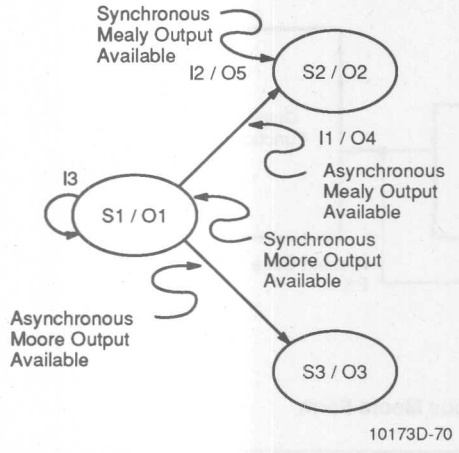


Figure 16. State Diagram Labelling for Different Output Types

As a matter of notation, Moore outputs are often placed within the state bubble and Mealy outputs are placed next to the path or arrow that activates them.

The relationship of Mealy and Moore, synchronous and asynchronous outputs to the states is shown in Figure 17.

Device Selection Considerations

There are three major criteria for selecting the correct state machine device for a design:

- Number of inputs/outputs
  - — I/O flexibility
  - — Number of output registers
- Speed
- Intelligence/functionality
  - — Number of product terms
  - — Type of flip-flops
  - — Number of state registers

Number of I/Os

The number of inputs, outputs and I/O pins determine the signals that can be sampled or generated by a state machine.

Timing and Speed

The timing considerations for sequencer design are similar to those for registered logic design. A system clock cycle forms the basic kernel for evaluating control function behavior. For the most part, all input and output functions are specified in relationship to the positive edge. Registered outputs are available after a period of time t_{CO}, the clock-to-output propagation delay. Asynchronous outputs require an additional propagation delay (t_{PD}) before they are valid.

For the circuit to operate reliably, all the flip-flop inputs must be stable at the flip-flop by the minimum set-up time (t_S) of the flip-flops before the next active clock edge. If one of the inputs changes after this threshold, then the next state or synchronous output could be stored incorrectly; the circuit may even malfunction. To avoid this, the clock period (t_P) must be greater than the sum of the set-up time of the flip-flops and the clock to output time ($t_S + t_{CO}$). This determines the minimum clock period and hence the maximum clock frequency, fMAX, of the circuit. Metastability and erroneous system operation may occur if these specifications are violated.

The timing relationships are shown in Figure 18. In each cycle there are two regions: the stable region, when all signals are steady, and the transition region, when the machine is changing state and signals are unstable. The active clock edge causes the flip-flops to load the value of the new state that has been set up at their inputs.

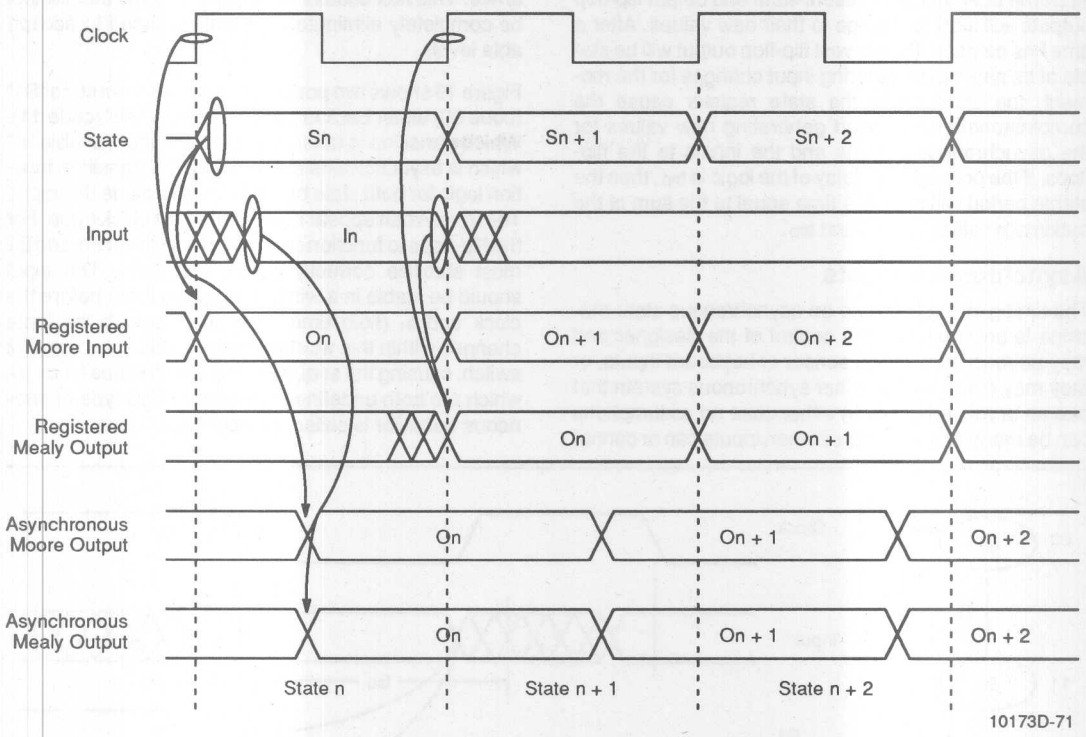


Figure 17. State Machine Timing Diagram

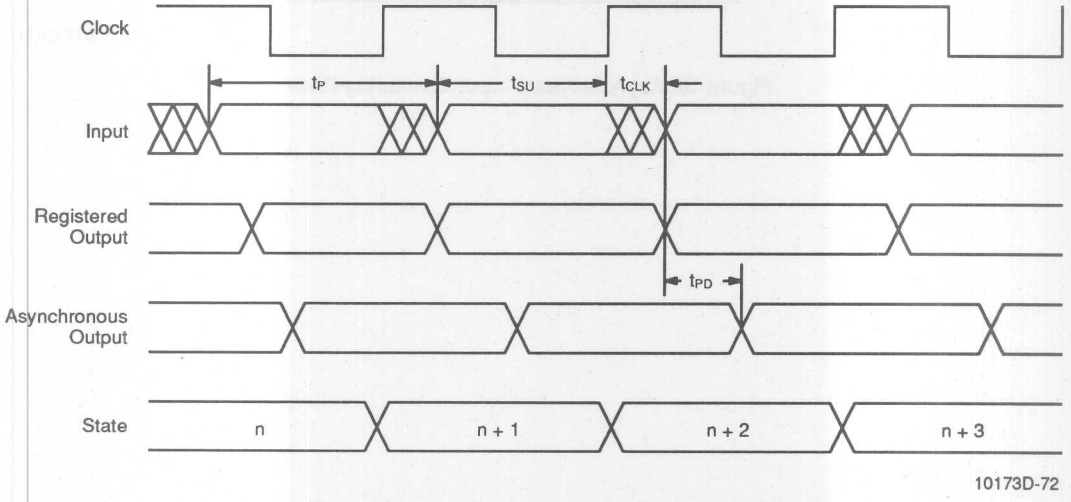


Figure 18. Timing Diagram for Maximum Operating Frequency

At a time after this, the present state and output flip-flop outputs will start to change to their new values. After a time has elapsed, the slowest flip-flop output will be stable at its new value. Ignoring input changes for the moment, the changes in the state register cause the combinatorial logic to start generating new values for the asynchronous outputs and the inputs to the flip-flops. If the propagation delay of the logic is t_{PD}, then the stable period will start at a time equal to the sum of the maximum values of t_{CO}, and t_{PD}.

Asynchronous Inputs

The timing of the inputs to an asynchronous state machine is often beyond the control of the designer and may be random, such as sensor or keyboard inputs, or they may come from another synchronous system that has an unrelated clock. In either case no assumptions can be made about the times when inputs can or cannot arrive. This fact causes reliability problems that cannot be completely eliminated, but only reduced to acceptable levels.

Figure 19 shows two possible transitions from state "S1" (code 00) either back to itself, or to state "S2" (code 11). Which transition is taken depends on input variable "A" which is asynchronous to the clock. The transition function logic for both state bits B1 and B2 include this input. The input A can appear in any part of the clock cycle. For the flip-flops to function correctly, the logic for B1 and B2 must stabilize correctly before the clock. The input should be stable in a window t_S (setup time) before the clock and t_H (hold time) after the clock. If the input changes within this window, both the flip-flops may not switch, causing the sequence to jump to states 01 or 10, which are both undefined transitions. This type of erroneous behavior is called an input race.

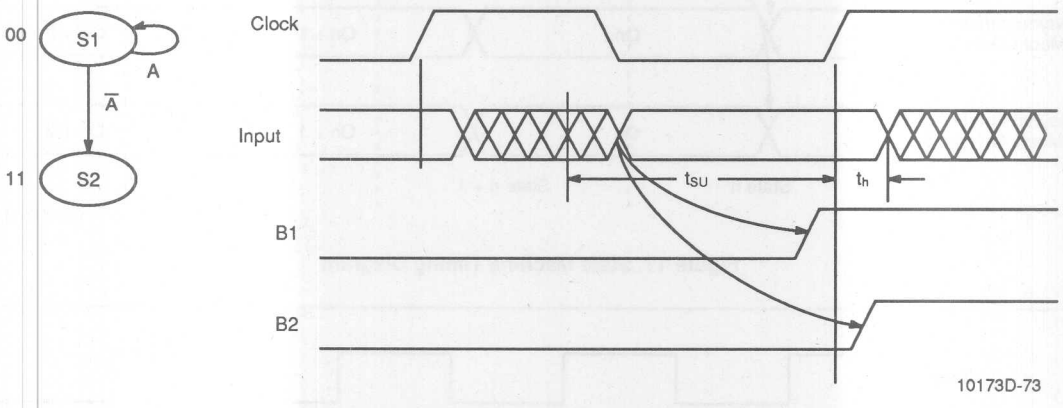


Figure 19. Asynchronous Input Cascading Race

A solution to this problem is to change the state assignment so that only one state variable depends on the asynchronous input. Thus, the 11 code must be changed to 01 or 10. Now, with only one unsynchronized flip-flop input, either the input occurs in time to cause the transition, or it does not, in which case no transition occurs. In the case of a late input, the machine will respond to it one cycle later, provided that the input is of sufficient duration.

There is still the possibility of an input change violating the setup time of the internal flip-flop, driving it into a metastable state. This can produce system failures that can be minimized, but never eliminated. The same problem arises when outputs depend on an asynchronous input.

Very little can be done to handle asynchronous inputs without severely constraining the design of the state machine. The only way to have complete freedom in the use of inputs is to convert them into synchronous inputs. This can be done by allocating a flip-flop to each input as shown in Figure 20. These synchronizing flip-flops are clocked by the sequencer clock, and may even be the sequencer's own internal flip-flops. This method is not foolproof, but significantly reduces the chance of metastability occurring.

Functionality

The functionality of different devices is difficult to compare since different device architectures are available. The number of registers in a device determines the number of state combinations possible. However, all the possible state combinations are not necessarily usable, since other device constraints may be reached. The number of registers does give an idea of the functionality achievable in a device. Other functionality measures include the number of product terms and type of flip-flop. One device may be stronger than another in one of these measures, but overall may be less useful due to other shortcomings. Choosing the best device involves both skill and experience.

In order to give an idea of device functionality, we will consider each of the architecture options available to the designer and evaluate its functionality.

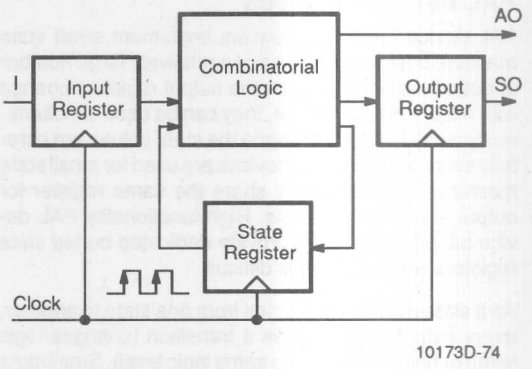


Figure 20. Input Synchronizing Register

PAL Devices as Sequencers

A vast majority of state machine designs are implemented with PAL devices. Early versions of software required the user to manually write the sum-of-products Boolean equations for using PAL devices. Second generation software allows one to specify the design in "state machine syntax," and handles the translation to sum-of-products logic automatically. PAL devices implement the output and transition functions in sum-of-products form through a user-programmable AND array and a fixed OR array.

PAL devices deliver the fastest speed of any sequencer and are ideally suited for simple control applications characterized by few input and output signals interacting within a dedicated controller in a sequential manner. The number of flip-flops in a typical PAL device range from 8 to 12, which offer potentially more than one thousand state values. Since some of the flip-flops are used for outputs, and the number of product terms is limited, the usable number of states is reduced drastically. Generally, up to about 35 states can be utilized.

PAL Device Flip-Flops

PAL device based sequencers implement small state machine designs, which have a relatively large number of output transitions. Since the output registers change with most state transitions, they can be used simultaneously as state registers, once the state values are carefully selected. Most PAL devices are used for small state machines, and efficiently share the same register for output and state functions. High-functionality PAL device based sequencers provide dedicated buried state registers when sharing is difficult.

As a state machine traverses from one state to another, every output either makes a transition (changes logic level) or holds (stays at the same logic level). Small state machine designs require relatively more transitions and fewer holds. As designs get larger, state machines statistically require relatively fewer transitions and more holds.

Most PAL devices provide D-type output registers. D-type flip-flops use up product terms only for active transitions from logic LOW to HIGH level, and for holds for logic HIGH level only. J-K, S-R, and T-type flip-flops use up product terms for both LOW-to-HIGH and HIGH-to-LOW transitions, but eliminate hold terms. Thus, D-type flip-flops are more efficient for small state machine designs. Some PAL devices offer the capability of configuring the flip-flops as J-K, S-R or T-types, which are more efficient for large state machine designs since they require no hold terms.

Many examples of PAL-device-based sequencers can be found in system time base functions, special counters, interrupt controllers, and certain types of video display hardware.

PAL devices are produced in a variety of technologies for multiple applications, and provide a broad range of speed-power options.

Testability

Advanced Micro Devices

INTRODUCTION

With digital logic design, it is all too easy to design a circuit which merely implements a specified function. When production starts it is suddenly found that the circuit cannot be tested, or perhaps that tests cannot be performed economically. Dealing with this situation can, at the very least, have a negative impact on the introduction of the system into the marketplace.

Potential headache can be avoided by taking test issues into consideration during the initial design. Instead of just designing a circuit which implements a specified function, which is the bare minimum that must be accomplished, that function needs to be implemented in a manner which can be tested.

The purpose of this section is to establish the notion of testability and its importance, and then to provide ways of avoiding the most common untestable circuits. The issues will be discussed primarily in the context of logic design in PLD's, although they are also relevant for general logic design.

In addition, test vectors will be reviewed. Various kinds of vectors are mentioned, and the general tools available for vector generation will be summarized.

Defining Testability — A Qualitative Look

A completely testable design is one in which any and all device faults can be systematically detected.

First note that the issue is one of devices, not designs. The design itself must work as specified; that is the main job of the design engineer. Once the design is implemented in a device, the issue is how to test the device to make sure that the design has been correctly implemented. Throughout this paper, then, it will be assumed that a particular design works as is; we will just be addressing its testability.

The easiest and most effective means of testing a circuit is through a systematic series of tests. A random set of tests may also do well, but does not yield much information regarding the testability of a circuit itself. No number of random (or systematic) vectors can test an inherently untestable circuit.

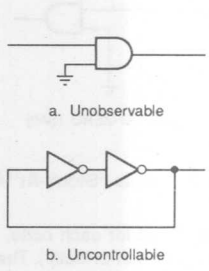
In order to be able to perform a systematic test sequence, every part of the circuit under test must be accessible, so that it can be controlled. Only then can each node be forced high or low as needed. This is essentially a requirement of complete *controllability* of the circuit.
In order to be able to detect faults every part of the circuit must also be visible to the outside world, so that the results of each test can be observed. In this manner, each node can be inspected to determine its logic level. This requires complete *observability*.

These are, of course, the age-old issues of controllability and observability, which are as important for digital logic circuits as they are for so many other kinds of systems. If any portion of a circuit is uncontrollable or unobservable, then the testability of the entire circuit is compromised.

Figure 1 shows a couple of completely untestable circuits. The integrity of the top input in Figure 1a can never be verified. No matter whether it is shorted to ground, to V_{CC}, or whether it is functioning correctly, the output will be the same. That is to say, any faults on the top input cannot be observed at the output.

The circuit in Figure 1a would appear pretty useless as is. It is possible, however, that instead of being directly grounded, the second input may be driven by some distant signal, possibly on a different PC board, which happens to be a a logic low. If you cannot bring this line to a logic high, then it might as well be grounded.

The circuit in Figure 1b essentially has no input. This circuit can be thought of as a latch, but there is no way to change its logic state. Therefore, it is completely uncontrollable.



14099-001A

Figure 1. Untestable Circuits

Quantifying Testability

In theory, if we want to quantify the testability of a given circuit, we might first attempt to make a list of all possible things that could go wrong with a circuit (no matter how unlikely), and then verify that all such "faults" can be tested, in all combinations and permutations. But for a circuit of any significance whatsoever, it will rapidly become apparent that this is not a practical solution. What we need instead is a measure which can give an empirically reliable indication of the testability of a circuit, or of the quality of a given set of tests. There are several different such measures, but the most popular of these is the *single stuck-at faults* model.

There are several ways of analyzing circuits for single stuck-at faults. For very large circuits, various *testability analysis* schemes have been developed. However, for smaller circuits, especially of the size that would be put into a PLD, the more common method uses simulation.

Simulating Single Stuck-At Faults

A given circuit is first simulated. The quality of the simulation is important; the more complete the simulation the better. A thorough simulation can then serve as a benchmark test sequence later. In this way, the fault simulation procedure also allows us to measure the quality of a given simulation, or set of tests, in addition to the testability of the circuit.

The results of the simulation are recorded. Next, one node in the circuit is modeled with a *"stuck-at" fault* — either *stuck-at-one* (SA1) or *stuck-at-zero* (SA0), as shown in Figure 2. The circuit is now resimulated. If the simulation results of the modified circuit are different from the simulation results of the good circuit, then the fault was detected. If not, then we have a faulty circuit which appears to operate correctly.

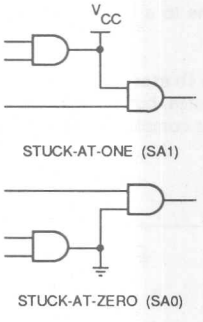


Figure 2. Single "Stuck-At" Faults

This procedure is repeated for each node, one node at a time (hence the name "single" stuck-at faults). The nodes are modeled with both SA1 and SA0 faults, so that for N nodes, we will have 2N simulations. If of those 2N simulations, D of them produced simulation results different from those of the original circuit, then we say that this simulation tested this circuit with a test coverage of D/(2N)*100%. Whereas this specifically tests only for single faults, experience shows that it is also a good test for multiple stuck-at faults.

Undetected Faults

Why are some of the faults not detected? For simple combinatorial logic, there are two basic reasons: either the simulation was not complete enough to find the fault, or the circuit itself cannot be tested for the fault. So when an undetected fault is located, the first step taken is to add vectors to the simulations which will exercise the node being tested. By doing this, we gradually improve the quality of the simulation, and thus the quality of the test sequence that we can use in production.

It is possible that certain nodes will have undetectable faults for which no new vectors can be added. These are the result of an untestable design. It is the joint job of the test and design engineers to generate a test sequence that is as complete as possible. It is the design engineer's responsibility to provide a circuit which is testable. If both of these responsibilities are carried out, the result will be a testable circuit which can be tested with an exhaustive test sequence. This will yield the highest quality system. Note, however, that the overall responsibility is shared between the design and test engineers.

Needless to say, this process of analyzing the testability of a circuit is not done all by hand; software aids are used. There are many different kinds of programs that run on many different kinds of systems, ranging from PCs to workstations to mainframes. Some of them are standalone programs; others are integrated into larger overall environments. Their specific capabilities also vary, but in general, they can simulate a given circuit with a given set of vectors; analyze the test coverage that the vectors provide for the circuit; and generate new tests, either from scratch or by improving on the coverage of a few manually generated "seed" vectors. Most can also point out potential problems areas of a circuit, such as race conditions and logic hazards.

Finally, one frequently asked question is "So what if there is a fault that can never be detected. Who cares?" Theoretically, this question is not unreasonable. However, most companies will not feel comfortable telling a customer "We only tested half of the system, but if anything goes wrong with the other half, you'll never notice it." In addition, as will be seen, many untestable circuits occur as a result of poor design practices.

Testability issues for sequential circuits have implications far beyond the test bed. Indeed, failure to take these issues into account can greatly affect the normal performance of a system. The key for state machines is controllability. The challenge is to make all elements of the circuit controllable, both for testing and for general functionality.

Designing Testable Combinatorial Circuits

All of the previous procedures dealt mostly with the ways in which existing circuits are treated. However, if a finished circuit is found to be untestable, then it must be redesigned for testability. An easier approach is to design for testability from the beginning. Unfortunately there is no direct recipe for a testable design. There are, however, many common ways of making a circuit untestable. Most of this section is devoted to pointing out such problems.

The simplest kind of problem is *redundant logic*. Figure 3a shows one such circuit. It has a purely redundant product term. If the output of either of the product terms is stuck low, for any reason, then as long as the other product term is good, the fault will never be visible at the output.

This may initially look like a benefit, since we have what we could call a "primary" circuit with a "backup." One can cover up some of the failures of the other (but not all failures). If this kind of redundancy is truly desired, this is not the way to achieve it. When you ship out this circuit, you do not know if you really have a working primary and backup. The primary may already be malfunctioning; since it was never tested, you will never know. If you want useful, reliable redundancy, test circuitry must be added, as in Figure 3b, so that each part of the circuit can be independently tested.

Figure 4 shows another redundant circuit. Although the product terms are not identical, the larger AND gate is really redundant. Any stuck-low faults at the output of this gate are not detectable.

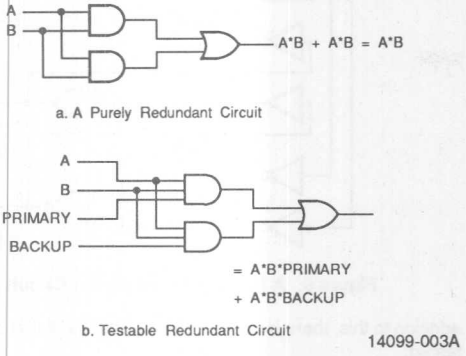


Figure 3. Making Redundancy Testable

Reconvergent Fanout

Redundant logic is a special case of what is called *reconvergent fanout*. This is a term that refers to circuits that have inputs

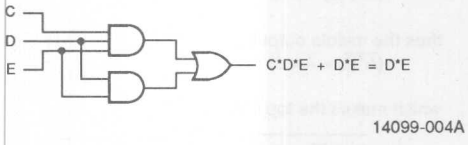


Figure 4. Circuit with a Redundant 3-input AND Gate

splitting up, going through independent logic paths, and then reconverging to form a single output, as shown in Figure 5. When this happens, it is very easy to introduce untestable nodes. It may not be easy to identify where such nodes are.

Figure 6 is an example of a reconvergent circuit. The inputs are shared between two different product terms, which are eventually summed. This circuit appears harmless enough, but it turns out that the node indicated by "SA1" cannot be tested for a stuck-at-

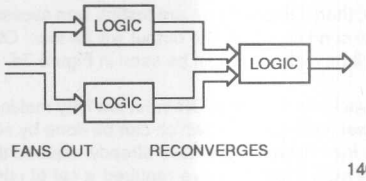


Figure 5. Reconvergent Fanout

one condition. In other words, there is no way that we can guarantee that that node is operating correctly.

It is worth analyzing this circuit a bit more closely. This will give some insight into the kinds of analyses that are necessary when evaluating circuits and generating tests, and into the ways in which untestable nodes are created.

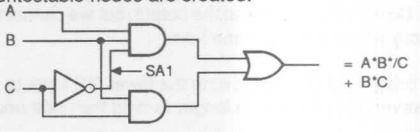


Figure 6. A Reconvergent Circuit with an Untestable Node

If we wish to prove that the node in question is not stuck high, then we must force it low and prove that we were successful in doing so. Thus we have two requirements: forcing the node low, and seeing the logic low on the output — controlling and observing the node.

First we raise input C high to force the node to a logic low condition, as in Figure 7a. This satisfies our controllability requirement. Next we need to provide a way to propagate this logic low to the output (Figure 7b). This is referred to as *sensitizing a path* to the output. The first step is to get the logic low past the AND gate. But if either input A or B is low, then the output of the AND gate will be low regardless of the node being tested. Thus we must force both A and B to a logic high, so that if there is a low on the output of the AND gate, we will know for sure that it came from the node we are testing. This is shown in Figure 7c.

Next we wish to get the logic low through the OR gate to the output. To do this, we must insure that the second OR input is always low; if it is high, then the output of the OR gate will be high regardless of the node being tested. If we can keep the lower OR

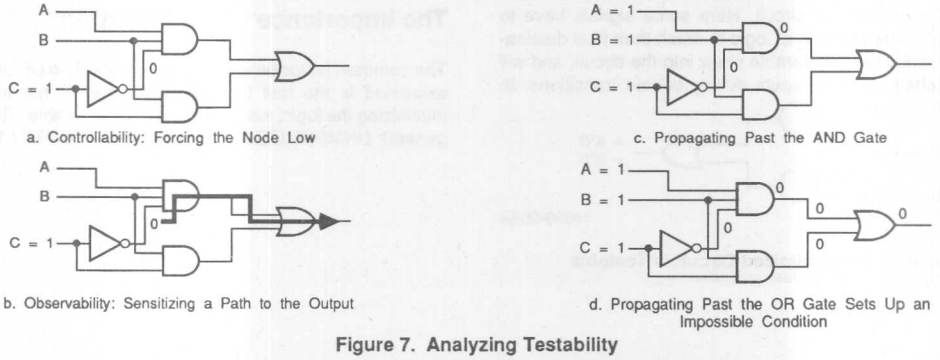


Figure 7. Analyzing Testability

input low, then if the node we are testing was sucessfully forced into a low condition, then the output will be low. Otherwise the output will be high. This can be seen in Figure 7d.

How do we keep the lower OR input low? By making the output of the lower AND gate low, which can be done by setting one of its inputs low. However, we have already required that all of the inputs be high. Thus we have required a set of conditions that cannot be met. One of three things will result:

1. The lower AND gate has both inputs high, and therefore keeps the lower OR input high. In this case, we may have been successful in forcing the node under test low, but we cannot see it at the output.

2. We bring input B low, allowing the lower OR input to go low. However, now the output of the upper AND gate will always be low. So we will see a low at the output, but we cannot be sure exactly where the low came from.

3. We bring input C low, allowing the lower OR input to go low. However, now we are no longer forcing the node under test low.

So we can either force the node low, but cannot see the low at the output; or, we can see a low at the output but cannot be sure of its source; or, we cannot force the node itself low. In any case, we will never be able to guarantee that the node under test is not stuck high.

Note that the two "independent logic blocks" which generate the signals that eventually reconverge are testable by themselves; they are just AND gates. It is only when we hook them together via the OR gate that the overall circuit becomes untestable. Thus *the testability of individual portions of a circuit does not guarantee that the entire circuit will be testable when the testable pieces are all connected.*

We can minimize this circuit using the following steps:

$$A*B*\overline{C} + B*C = A*B*\overline{C} + B*C + A*B*B \text{ (by consensus)}$$
$$= A*B*\overline{C} + B*C + A*B$$
$$= A*B + B*C$$

Thus the node we were trying to test is really not needed in the logic. The resultant circuit is shown in Figure 8, and is completely testable.

Not all reconvergent circuits are so simple. Figure 9 shows a more complicated reconvergent circuit. Here some signals have to travel through several levels of logic to reach their final destination. This introduces considerable skew into the circuit, and will produce glitches on the outputs during certain transitions. In addition to this, there is again a stuck-at-one fault that cannot be tested.

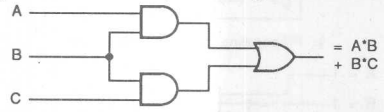


Figure 8. The Minimized Circuit is Testable

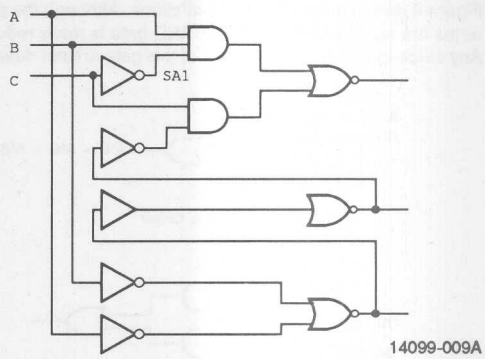


Figure 9. A Messy Reconvergent Circuit

Circuits like this can result from the design iteration process, as a designer tries to debug a circuit. By adding this and that, eventually the circuit works. But it is a mess, has poor timing characteristics, and is untestable. A little analysis of the logic itself shows that:

the bottom output is
$(\overline{A} + \overline{B}) = A*B$

thus the middle output is
$(\overline{A*B}) = \overline{A} + \overline{B}$

which makes the top output

$$\overline{(A*B*\overline{C} + C*\overline{(\overline{A} + \overline{B})})} = \overline{(A*B*\overline{C} + A*B*C)}$$
$$= (\overline{A*B})$$
$$= \overline{A} + \overline{B}$$

That is, the top two outputs are actually the same, and the third output is just the inverse of the top two. As convoluted as the original circuit looks, the logic itself is actually trivial. So if three outputs are really needed for some reason, we can generate them independently, as in Figure 10a. If only two outputs are needed, it is even easier. Figures 10b and 10c show two possibilities.

These circuits are much easier to understand, their timing characteristics are better, and they are completely testable.

The Importance of Minimization

The common factor behind all of the untestable circuits we have examined is the fact that all of them were not minimal. By minimizing the logic, we made the circuits testable. This is true in general: *UNMINIMIZED LOGIC CANNOT BE FULLY TESTED.*

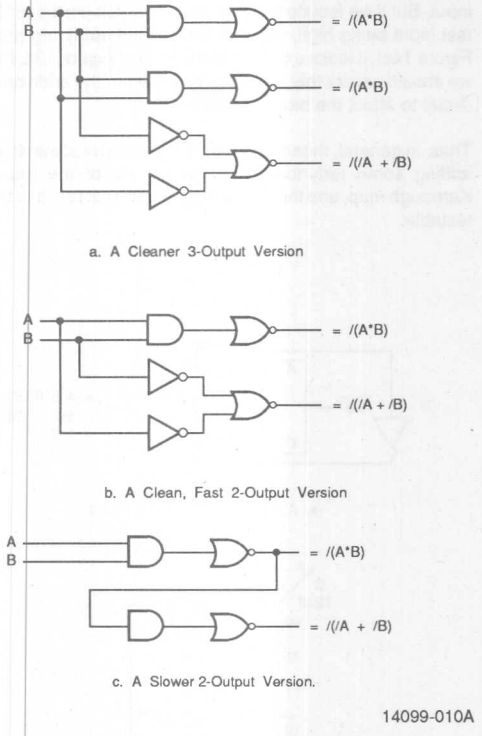


Figure 10. Simplifying the Circuit of Figure 9.

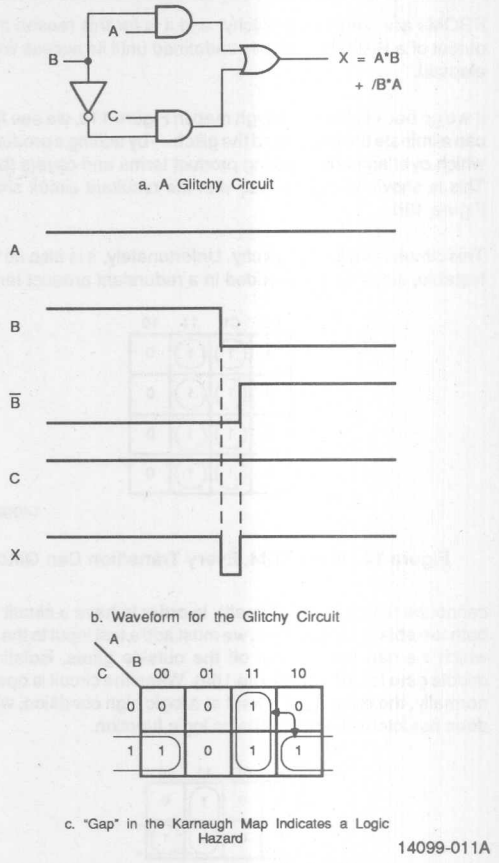


Figure 11. Examining a Glitchy Circuit

Very often, especially when designing with PLDs, an attempt is made to minimize logic only to the point where it fits into a particular PLD. Any further minimization is considered an academic waste of time. This is a grave misconception. Getting rid of all extra product terms, and eliminating all extra literals on the remaining product terms has real value. Failing to do so will result in untestable nodes in the circuit.

Minimizing is not always enjoyable, since hand techniques are usually too tedious, and Karnaugh maps are essentially useless for more than four or five inputs. However, computers have long been used to minimize logic. In particular, PALASM® software (version 2.22 and later) has a minimization routine which can minimize logic automatically before assembly.

Logic Hazards

One occasional side effect of minimization can be the introduction of *glitches* into a circuit. Figure 11a shows such a "glitchy" circuit. The waveform in Figure 11b shows that under steady-state conditions, as long as inputs A and C are high, the output is high regardless of B. However, as B changes from high to low, causing the top product term to shut off and the bottom one to turn on, the inverter adds a bit of delay to the path that will turn on the lower product term. Thus the top term may shut off before the bottom one gets a chance to turn on. In this case, we have two logic low signals going into the OR gate, giving a low on the output. As soon as the lower product term turns on, the output goes back high, but not before the appearance of the high-low-high glitch.

Figure 11c shows the Karnaugh map for this circuit. It is minimal, but there are two product terms which do not overlap; they are "adjacent" in one location. These represent the two AND gates in the circuit diagram. The arrows indicate the troublesome transition: when A and C are high, and when B changes from high to low or the reverse. We can intuitively think of this as a "gap" between the two adjacent product terms, in which a glitch may occur.

Note that glitching is not a certainty. It is called a *hazard* because in certain situation, given certain timing situations, there is a chance that a glitch will occur.

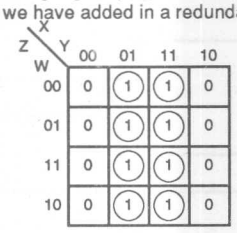
Note also that the glitch is not really caused by the minimization process itself, but is caused by these "gaps" in the Karnaugh map. Unminimized logic with such gaps may also be glitchy.

A PROM is a good example of such a circuit. PROMs can be used to implement any logic function of their inputs. However, regardless of the function, it is implemented in a completely unminimized fashion, using complete minterms. So even a function as simple as the one in Figure 12 (which could be implemented using a single product term, grouping all 1's into a single cell) is implemented with each 1 in its own cell. Thus there is a gap between every cell, meaning that every transition is a potential glitch.

PROMs are notoriously glitchy, and it is for this reason that the output of a PROM is actually undefined until its access time has elapsed.

If we go back to the Karnaugh map in Figure 11c, we see that we can eliminate the gap — and the glitch — by adding a product term which overlaps both existing product terms and covers the gap. This is shown in Figure 13a, with the resultant circuit shown in Figure 13b.

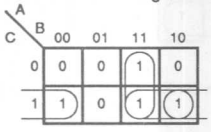
This circuit is no longer glitchy. Unfortunately, it is also no longer testable, since we have added in a redundant product term that



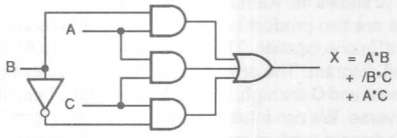
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Figure 12. In a PROM, Every Transition Can Glitch

cannot be tested (try it yourself). In order to have a circuit that is both testable and glitch-free, we must add a test input to the circuit which we can use to shut off the outside gates, isolating the middle gate for testing (Figure 14a). When the circuit is operating normally, the extra input is kept at a logic high condition, where it does not interfere with the basic logic function.



a. A Redundant Product Term Can Eliminate the Glitch



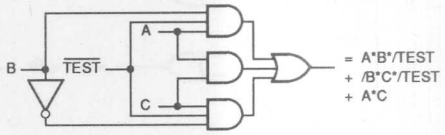
b. A Glitch-Free, but Untestable Circuit

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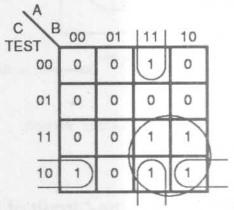
Figure 13. Eliminating Glitches

The Karnaugh map for this circuit is shown in Figure 14b. Note that all product terms overlap, but now the circuit is minimal. The size of the Karnaugh map has doubled, since we added another input. But if we isolate just that portion which corresponds to the test input being high, which is the normal operating mode (see Figure 14c), it looks exactly like the map of Figure 13a. Of course we should expect this, since we do not want the addition of a test circuit to affect the basic function.

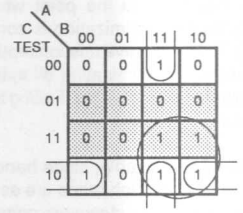
Thus, in general, these types of glitches can be eliminated first by adding some redundant logic to get rid of the gaps in the Karnaugh map, and then by adding a test input to make the circuit testable.



a. A Testable, Glitch-Free Circuit



b. Karnaugh Map



c. Karnaugh Map Showing Non-Test-Mode Portion

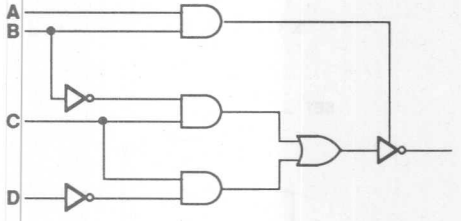
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Figure 14. Making a Glitch-Free Circuit Testable

Using Output Enable

Most state machine PLDs are equipped with an enable pin for disabling the outputs. This is a key feature when the circuit board is to be tested in a bed-of-nails tester. When the devices driven by by the PLD are tested, it is recommended that the PLD be disabled so that there is no output level contention. Since the enable pin is usually grounded to keep outputs permanently enabled, it can instead be made available for use during testing.

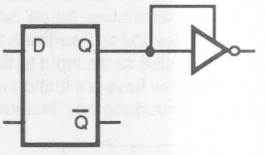
Note that for combinatorial devices, there is generally no output enable pin. The disabling feature is instead implemented through a product term. This feature is called programmable three-state. Designing the part such that the outputs can be disabled during bed-of-nails testing is also encouraged for these combinatorial designs.



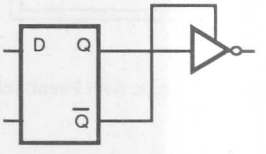
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Figure 15. Untestable combinatorial circuit with programmable three-state

The user must be especially aware of the observability of outputs with programmable output three-state. In Figure 15, input B controls both the basic circuit logic and the three-state control logic. Therefore, any function which involves B in a LOW state will not be observable, since the output will not be on. Figure 16a is a simplified representation of a register whose output cannot be observed because the three-state buffer is disabled when the output is LOW. Likewise, the circuitry in Figure 16b cannot be observed when the flip-flop output is HIGH. The user must make sure that an output will not be disabled when the results of a test are to be observed.



a. LOW state observable



b. HIGH state unobservable

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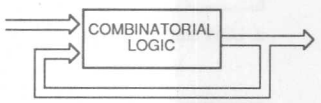
Figure 16. Untestable registered output with programmable three-state

Designing Testable Sequential Circuits

The design of sequential circuits involves considerations above and beyond those required for simple combinatorial circuits. Latches and oscillators are circuits which appear combinatorial, but which use feedback to introduce sequential properties. State machines use flip-flops and feedback to generate what can be complex sequential circuits.

Feedback

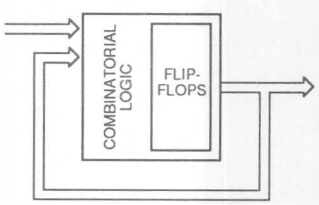
Whereas combinatorial circuits depend only on the conditions of present inputs, *sequential* circuits depend on both present conditions and past behavior to determine future behavior. This is made possible primarily by *feedback*. Feedback takes an output signal and routes it back for use as an input to the same circuit, as shown in Figure 17. We now have a situation where an output depends on itself; this can introduce new testability problems.



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Figure 17. Logic with Feedback

Most sequential circuits (under varying circumstances also called *state machines*, *finite state machines*, and *sequencers*) make use of *flip-flops* as memory elements. These memory elements serve to remember a past condition (called a *state*) so that a future decision can be made based on it. This state is then fed back as input. With PLDs, the flip-flops and combinatorial logic are contained within a single device, as shown in Figure 18.



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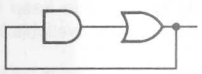
Figure 18. Structure of a Sequential PLD

Of course, the effects of feedback may have to be considered even when there are no flip-flops. The circuit in Figure 17 has feedback, but has no flip-flops. Such a circuit will either function as a *latch* or as an *oscillator*, as will be seen.

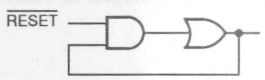
Before we look into the special needs of circuits with feedback, bear in mind that all of the testability criteria discussed for combinatorial logic still hold. The blocks of combinatorial logic shown in Figures 17 and 18 must be testable by themselves. What we will discuss here are issues which must be considered in addition to the issues involving combinatorial logic.

Latches

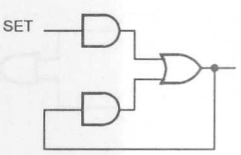
A combinatorial logic circuit which uses positive feedback is a latch. The simplest possible latch is shown in Figure 19a. The output is fed back as an input in its TRUE form. This means, of course, that the output will stay at its present level; hence the name "latch."



a. Completely Uncontrollable



b. Cannot Set Output HIGH



c. Cannot Reset Output LOW

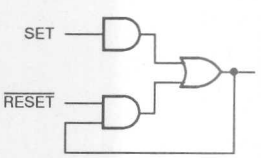
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Figure 19. Uncontrollable Latches

The circuit as shown is clearly not useful, since it will always remain in its power-up state. If another input is added, as in Figure 19b, a HIGH output could be made to go LOW by setting the $\overline{\text{RESET}}$ input LOW. However, once the output goes LOW, there is no way to make it go HIGH again. Likewise, the circuit could be modified as in Figure 19c. Now a LOW output can be made HIGH by setting the SET input HIGH. However, once HIGH, the output can never be made to go back LOW.

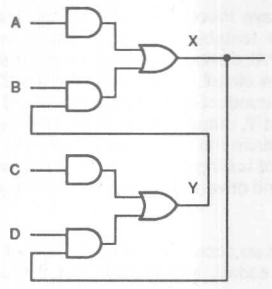
Controllable latches

For a latch to be useful, it must be completely controllable. The previous latches cannot be completely controlled. In order for a latch to be controllable, it must have both SET and RESET controls, as shown in Figure 20.



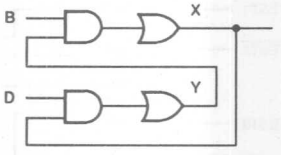
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Figure 20. A Controllable Latch



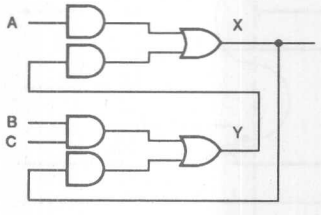
X = A
+ B*Y
= A
+ B*(C + D*X)
= A
+ B*C
+ B*D*X
SET
RESET

a. Latch with SET and RESET



X = B*Y
+ B*D*X
RESET

b. Latch with RESET Only



X = A + Y
= A
+ B*C
+ X
SET

c. Latch with SET Only

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Figure 21. More Complex Latches

In PLDs, a latch can be detected by simplifying the logic for each function. If an output is a function of itself in TRUE form, then it is a latch. To be controllable,

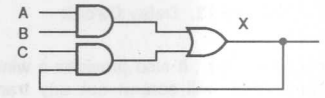
- product terms containing the feedback should have at least one other direct input in the product (providing RESET control).
- there should be at least one product term with no feedback (providing SET control).

The circuit in Figure 21a provides an example. At first it is not immediately obvious that the circuit is a latch, but when the logic is simplified, we see that indeed it is. It is controllable since it has both SET and RESET controls. If the logic were as shown in Figures 21b or 21c, the latch would be uncontrollable under some circumstances.

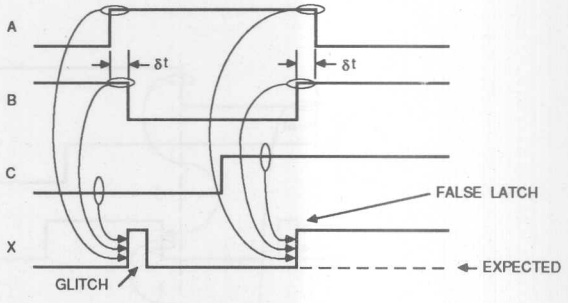
Latch hazards

The circuit of Figure 20 can be generalized to have several inputs on both the set and reset controls. Such a circuit is shown in Figure 22. In this case, we have two inputs on the set AND gate. If the two set inputs A and B change from 0 and 1 to 1 and 0, respectively, then there will be a glitch or a false latch at the output if both inputs were 1 at some time during the transition (Figure 22). For this transition, it is important to make sure that the 1-0 transition be made before the 0-1 transition to avoid anomalous output behavior. Merely delaying one input will not help, since it will delay both rising and falling transitions.

The simplest solution to this problem is the use of an edge-triggered flip-flop to synchronize the signals. This will eliminate any such glitches. If a flip-flop cannot be used, it is possible to delay reaction to a "11" condition to make sure that such a condition is not transitory. A circuit that accomplishes this is This delay circuit will delay the effect of an "11" input by an extra



a. Circuit

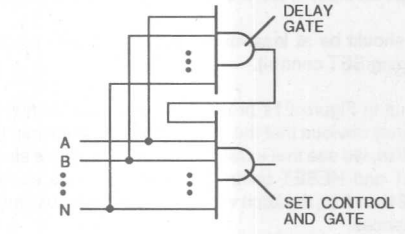


b. Glitch and False Latch

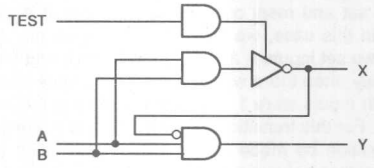
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Figure 22. A Latch with More Complex SET Logic

shown in Figure 23a. This is relatively efficient in that only one delay circuit is required regardless of the number of inputs used on the set control (within the limits of the size of the AND gate). It will require an extra output on a PAL device.



a. Circuit Which Delays "11...1" signals



b. Testable Delay Circuit

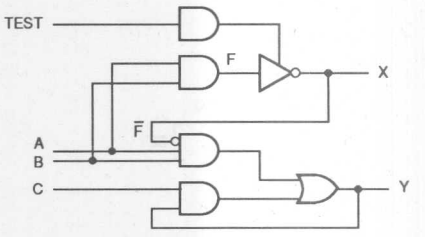
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Figure 23. Delay Circuit

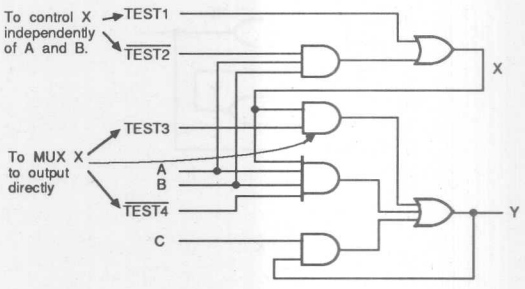
propagation delay. However, it also provides a window of one propagation delay which will screen out any transitory "11" conditions that occur within that window. This allows up to one propagation delay's worth of skew between inputs during a transition from "01" to "10."

Because we have introduced redundancy, the circuit must be modified to be testable. If the circuit is implemented in a combinatorial PAL device, then programmable three-state can be used to test the circuit, as shown in Figure 23b. By enabling output X, the redundant circuit can be observed without regard to Y. Then, to test Y, output X is disabled and then the pin is used as an input to drive the circuitry for Y directly. This provides a simple means of testing the circuit, but it only works if pin X can be measured and driven. The complete circuit is shown in Figure 24a.

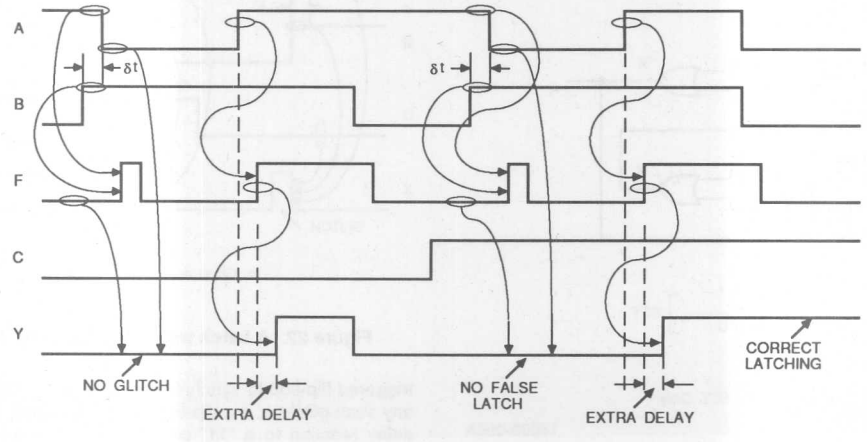
If node X is not so accessible, then additional circuitry and test inputs must be added. In the worst case, if node X is completely



a. Complete Latch Circuit



b. Circuit if Node X is Completely Inaccessible



c. Latch Circuit Behavior

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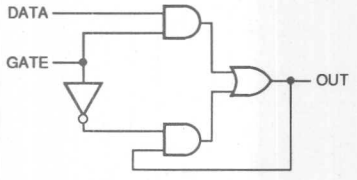
Figure 24. A Testable Glitch-Free Latch

inaccessible, the resulting testable circuit is shown in Figure 24b. Note that although the three-state capability is not needed, the circuit requires two extra gates, and, worst of all, four test inputs.

Figure 24c shows the behavior of either of the testable glitch-free latches.

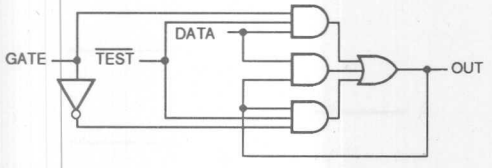
Transparent latches

Many designers like to use PLDs to design standard D-type "transparent" latches. A D-type latch is a very simple circuit, shown in basic form in Figure 25a. As it turns out, however, this is a glitchy circuit of the type discussed in the combinatorial section. The problem is compounded in this case, since, given the right timing, the glitch can actually be latched; the glitching problem is no longer transitory. If this type of circuit is desired, it must be designed to be both glitch-free and testable; the resultant circuit is shown in Figure 25b.



OUT = GATE*DATA
+ /GATE*OUT

a. Glitchy



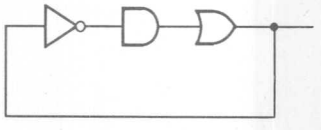
OUT = GATE*DATA*/TEST
+ /GATE*OUT*/TEST
+ DATA*OUT

b. Glitch-Free and Testable 14099-024A

Figure 25. D-Type Transparent Latches

Oscillators

Circuits whose outputs are fed back in TRUE form are latches. If the outputs are fed back in COMPLEMENT form, then the circuit is an oscillator. A simple oscillator circuit is shown in Figure 26.

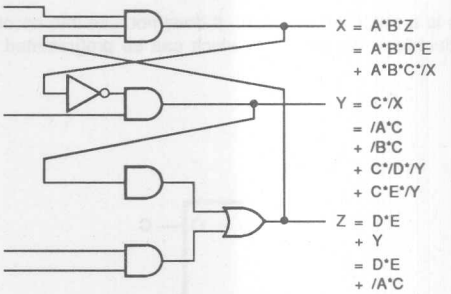


14099-025A

Figure 26. A Simple Oscillator

Latches are very often useful in circuits; oscillators rarely are. Crystals and other specialized oscillators are useful when it is necessary to generate a clock signal, for example. Trying to build an oscillator out of standard logic or PLDs will not yield a very predictable, accurate oscillator; where these circuits occur, it is usually by accident.

An oscillatory circuit may not always be obvious. It also may not oscillate all of the time. The oscillator shown in Figure 26 is uncontrollable; it always oscillates. However, just as we can design controllable latches, we can also design controllable oscillators (on purpose or by accident). This means that there may be an oscillator hidden in the circuit which will sometimes oscillate and sometimes be stable. Such a circuit is shown in Figure 27a.



a. Complete Circuit

X = A*B*D*E TERM 1
+ A*B*C*/X TERM 1

b. The Equation for X

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Figure 27. A Conditional Oscillator

Detecting oscillators

The oscillator in the circuit is not obvious. But if we simplify the logic completely, we can see that output X depends on /X; output Y depends on /Y; and output Z depends on /Z. Since the outputs are fed back to themselves in COMPLEMENT form, the circuit constitutes an oscillator.

This circuit will sometimes be stable. If we examine the logic function determining X, we see that it has two product terms, shown in Figure 27b. Term 1 is independent of /X; term 2 is dependent on /X. If inputs A, B, D, and E are all TRUE, then term 1 becomes TRUE, and the output stays HIGH regardless of the status of the rest of the circuit. It is thus stable. However, if signals D and/or E are LOW, then term 1 will be FALSE. If, at the same time, input C is HIGH, then, as long as the output X is LOW, term 2 will be TRUE, making the output HIGH (which makes the product term FALSE, which makes the output LOW, etc.). That is, the circuit oscillates.

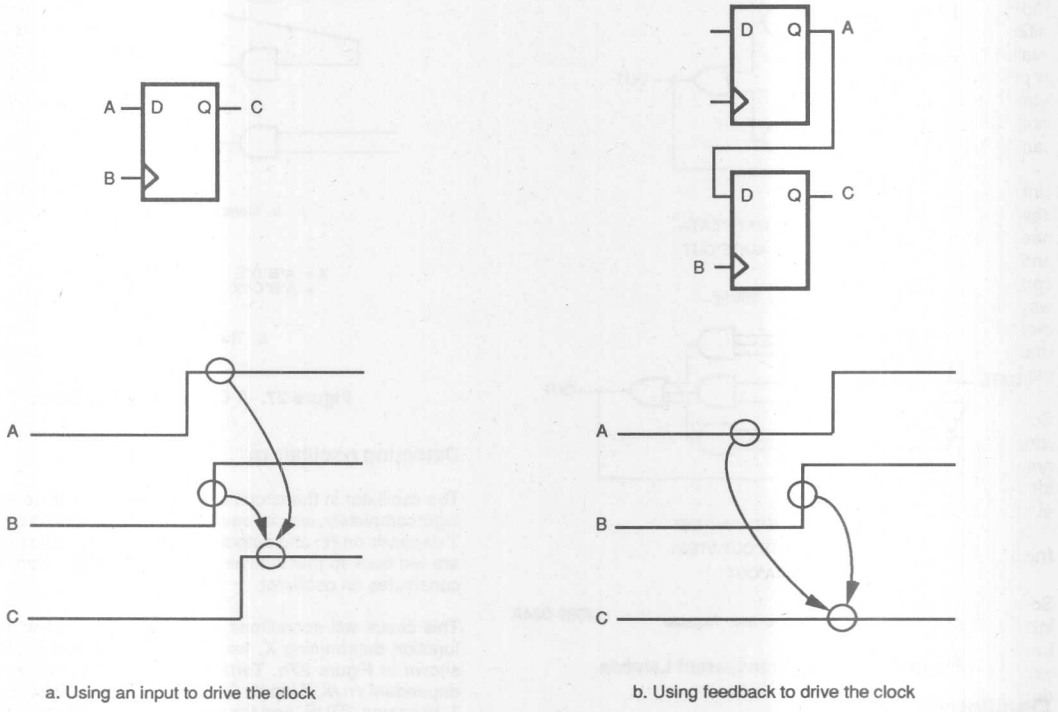
In this manner, we can identify the conditions under which a conditional oscillator will oscillate. The mere presence of an oscillator is usually an indication that the circuit needs to be changed. It may be that the circuit only oscillates under conditions that could never possibly exist. One must be very certain of the impossibility of such a condition, however, if a conditional oscillator is to be tolerated. In addition, a thorough test sequence will usually expose a circuit to conditions that it may never encounter in a real system. Thus oscillators may interfere with the test process even if they do not disrupt the system.

Using a Programmable Clock

When using the programmable clock on an asynchronous device, caution must be exercised with data setup. Refer to Figure 28a, where A and B are primary inputs. One setup time (t_s) after signal A goes active, signal B goes active, clocking signal A into the register. In Figure 28b, B is a primary input but signal A is fed back from another register. In this case it may be harder to ensure that the proper setup time is allowed before signal B is asserted, possibly causing improper information to be clocked into the register.

This is a simplified scenario. It does not take into account the product term on the clock, which can be programmed with a combination of any of the array inputs. A complex clock term can be a hidden source of frequently-violated setup time when feedback terms are used. Always be aware of which input or combination of inputs and feedbacks will clock each register, and calculate setup time backwards from the last input which will assert the clock term. This is the best and probably the easiest method for determining when data must be made available at the D input of the register.

This is an important testability issue because with a programmable clock, the tester may no longer be in control of the clock timing. Automatic test equipment is capable of handling the timing for dedicated clock pins, but the programmable clock feature does not allow the tester the luxury of a single controlled clock pulse.



a. Using an input to drive the clock

b. Using feedback to drive the clock

14099-027A

Figure 28. Using a programmable clock

Designing Testable State Machines

State machines have their own set of controllability issues. These essentially boil down to the concepts of *initialization* and *illegal states*.

State machine initialization

The nature of a state machine is that there is a well-defined sequence of states through which the machine will traverse as it operates. This implies the existence of a "first" state. Of course, these initial states vary from design to design. One obvious problem is the fact that many flip-flops — especially older varieties — do not power up in a predictable state.

Power-up initialization

Flip-flops that truly power up into a random state must be initialized explicitly. Lately, however, flip-flops have become available which have "power-up reset". This allows the flip-flops to power up into a predictable state every time. This is helpful when the power-up state also happens to be the initial state. But even if it is not the initial state, a predictable initialization sequence can bring the state machine into its start-up state.

Unfortunately, such initialization schemes rely on the ability of the device to initialize itself when being powered up. If the system needs to be re-initialized, it will have to be completely turned off and then turned on again. Anyone who has had to turn off a computer in order to reboot will know that this is not an elegant way of re-initializing. By building initialization into the design, a means of performing a "warm boot" is provided. It is for this reason that initialization must be considered along with all other aspects of the design.

Some devices have mechanisms specifically designed for initializing a state machine. These are usually in the form of global preset and reset product terms. By programming the conditions for initialization onto such terms, the device can be re-initialized at any time.

Including initialization in a design

Some of the simpler devices do not have specific provisions for initialization. However, the need is still present in these devices; here the initialization should be included in the design. This is a very simple process; it can be added in after all of the other design details have been worked out. Adding initialization will use up one input pin and potentially one product term on some outputs; this can affect the choice of device for the design.

To provide initialization in an otherwise complete design when Boolean equations are being used:

- determine the start-up state.
- assign each bit as being initialized active or inactive, based on the desired start-up state.
- if a bit is to be initialized inactive, add "/INIT" to every product term for that bit.
- if a bit is to be initialized active, add one product term consisting solely of "INIT."

Here we have assumed that the initialization pin has been called "INIT." "Active" would mean HIGH for an active high device; LOW for an active low device. "Inactive" is just the reverse.

The equation in Figure 29a can be initialized inactive as shown in Figure 29b, or active as shown in Figure 29c. Initialization is accomplished by asserting the INIT pin and clocking once. This "cookbook" approach is very reliable.

```
Q0 := Q1*Q2
    + Q2*/Q3
```

a. Uninitializable

```
Q0 := Q1*Q2*/INIT
    + Q2*/Q3*/INIT
```

b. Initialized Inactive

```
Q0 := Q1*Q2
    + Q2*/Q3
    + INIT
```

c. Initialized Active

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Figure 29. Designing in Initialization

PALASM software also makes it possible to design state machines with a special syntax which essentially allows the state diagram to be transferred directly into a design file. For devices which have no dedicated initialization features, the initialization branches should be explicitly built into the state diagram. The software then performs the remainder of the processing needed.

Illegal states

A state machine is formed by using a set of flip-flops to remember states, and assigning a code to each state. Since there are 2^n different codes that can be assigned to a group of n flip-flops, there is a good chance that some codes may not be used. For example, if a state machine is to have 6 states, 2 flip-flops will not be sufficient; 3 are needed. But 3 flip-flops allow 8 states, which will result in 2 unused states (see Figure 30).

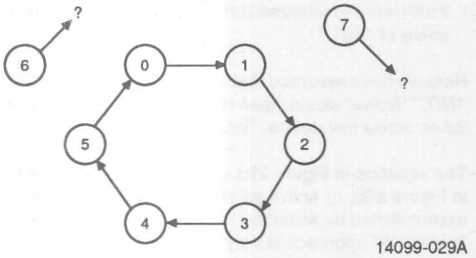


Figure 30. Illegal States

Assuming that the state machine has been designed correctly, there is no reason why these extra states should ever be entered; therefore they are called "illegal" states. Unfortunately, situations do occur, thanks to noise and other unpredictable occurrences, which result in the state machine being in an illegal state. When this happens, the immediate need is to return to a normal sequence of states: *there must be a predictable means of getting from any illegal states into a legal state.*

Illegal state recovery is a controllability issue which actually affects functionality more than it affects testability. But the concepts used for functionality and testing are so closely related that it is worth treating here.

Recovering from illegal states

There are three basic ways to get out of an illegal state:

- re-initialize
- make sure that one can continue clocking until the machine recovers
- design the machine such that the start-up state is reached from any illegal state in one clock cycle, independent of any conditional inputs

Of course, re-initializing will take the machine back into its start-up state from any state, legal or illegal (Figure 31). The disadvantage here is that outside control is needed to force initialization.

Very often, a path will exist which eventually takes the state machine back into a normal sequence (Figure 32). These paths are not usually designed in; they just happen to be there. In fact, if D-type flip-flops are used, it is surprisingly difficult to get a "closed" set of illegal states (that is, a set such that once one of the illegal states is entered, the machine will forever remain in illegal states) by accident. In most cases, there will be a path

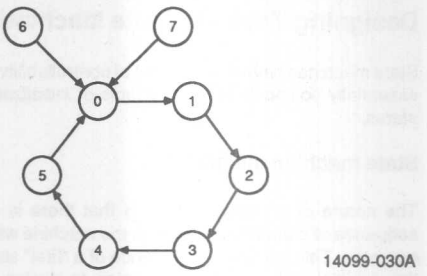


Figure 31. Using Initialization to Recover

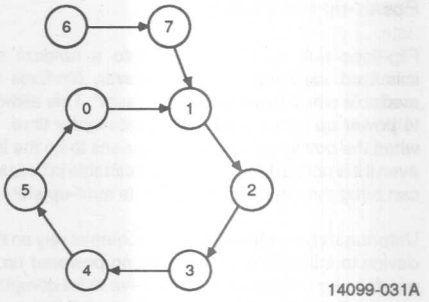


Figure 32. Cycling Back to a Legal State

which eventually leads back to a legal state. In these cases, merely clocking enough times will cause the machine to recover.

The drawback here is that one does not know ahead of time how many clock cycles will be needed. This necessitates some built-in way of knowing just when a legal state has been re-entered. And once that state has been reached, further cycling may be needed to get to a point where operation can resume.

Designing-in one-step recovery

The most predictable way of dealing with illegal states is to provide a one-step path back to a legal state. Depending on the state desired, more or less work may be involved to do this. For PAL devices, we can consider three cases:

- all illegal states go to state 00...0
- all illegal states go to one state other than 00...0
- each illegal state goes to some legal state

The cause of poor illegal state recovery can be illustrated conceptually with Karnaugh maps (although realistically, Karnaugh maps are often not used). When calculating the equations for a particular bit, it is tempting to use Don't Care cells from the Karnaugh map (Figure 33) to simplify the logic. The success of illegal state recovery depends on how these Don't Care cells are treated.

Recovering into state 00...0

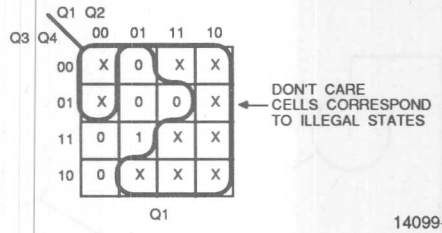


Figure 33. Illegal State

This is the simplest case; it is illustrated in Figure 34. It is accomplished by not using any illegal states to generate the logic for any of the bits. Since most PAL devices have only D-type flip-flops, a bit will go HIGH only as a result of legal states. Any illegal states will cause all bits to be LOW.

This procedure does not work when J-K or T-type flip-flops are used. In fact, it is deadly. Whereas a D-type flip-flop defaults to LOW, J-K and T-type flip-flops hold their present state as a

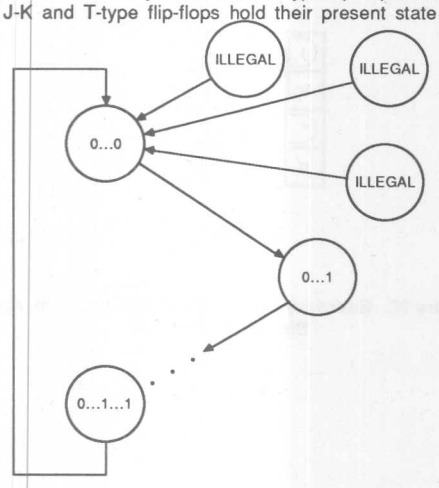


Figure 34. Recovering to State 0...0

default. Thus if illegal states are not considered in the transfer functions, an illegal state will cause the state machine to be locked up in that state.

Recovering into one fixed state

This case is shown in Figure 35a. The procedure can be illustrated conceptually with a Karnaugh map. It must first be decided which legal state will be entered, and the resultant value of each state bit. The Don't Care cells for each bit are then filled with the corresponding next state bit value; if the next state for a bit is to be 1, then Don't Care cells are filled with 1's for that bit's Karnaugh

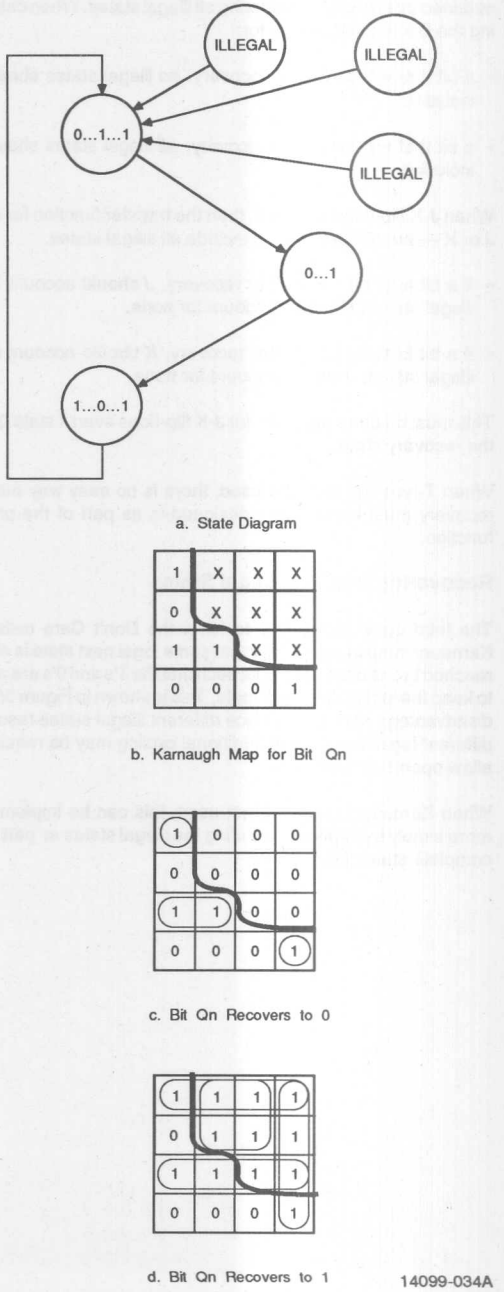


Figure 35. Recovering to a State Other Than 0...0

map; the procedure for a 0-bit is analogous. The equations are now taken by including either all Don't Care cells if filled with 1's, or none of them if filled with 0's. This procedure is illustrated in Figures 35b, c, and d.

When Karnaugh maps are not used, the same result can be obtained by explicitly considering all illegal states. When calculating the Boolean equations for:

- a bit that will be 0 after recovery, *no* illegal states should be included.
- a bit that will be 1 after recovery, *all* illegal states should be included.

When J-K flip-flops are used, then the transfer function for either J or K — but not both — will include all illegal states.

- If a bit is to be HIGH after recovery, *J* should account for all illegal states; *K* should account for none.
- If a bit is to be LOW after recovery, *K* should account for all illegal states; *J* should account for none.

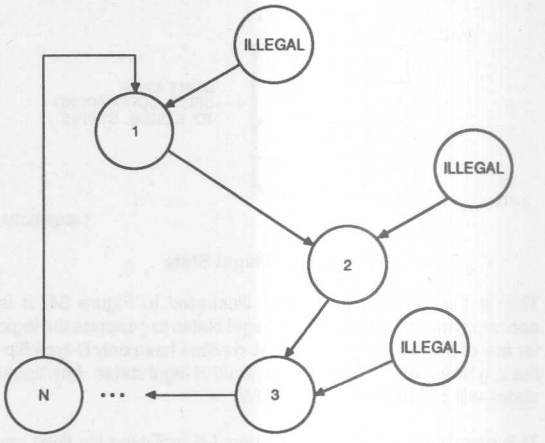
This must be done explicitly for J-K flip-flops even if state 0...0 is the recovery state.

When T-type flip-flops are used, there is no easy way out; any recovery must be explicitly designed-in as part of the original function.

Recovering Into Any Legal State

The third case allows one to fill in the Don't Care cells of a Karnaugh map in such a way that some legal next state is always reached in one clock cycle, but such that the 1's and 0's are placed to keep the logic functions simple. This is shown in Figure 36. The disadvantage here is that since different illegal states result in a different legal state, some additional cycling may be required to allow operation to resume.

When Karnaugh maps are not used, this can be implemented more simply by explicitly including the illegal states as part of the complete state diagram.



a. State Diagram

1	1	1	1
0	0	0	1
1	1	1	1
0	0	0	1

b. Karnaugh Map

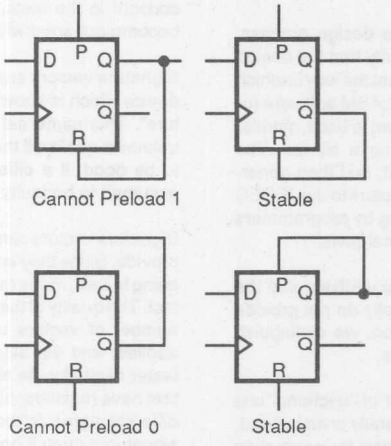
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Figure 36. Recovery Such That Logic Functions Are As Simple As Possible

Testing illegal state recovery

One of the difficulties of designing illegal state recovery into a circuit is the fact that it is difficult to test. Because the state is illegal, it is impossible to force the circuit into such a state. The use of register preload circumvents this problem. With preload, any state — legal or illegal — can be loaded into the register. If an illegal state is loaded, then the circuit can be tested to verify that correct recovery does indeed occur.

The use of preload must be considered carefully with devices having programmable asynchronous preset and reset features. If these are driven by feedback from an output, then situations can occur where preloading one state immediately causes a preset or reset to the opposite state (Figure 37). There are two alternatives: either avoid preloading such states, or include a control input in the preset and/or reset product terms which can disable the feature when testing.



Stable Case: Can preload any state
Other Cases: Preloading any state will cause PRESET or RESET to opposite state.

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Figure 37. Preloading Registers with PRESET and RESET

Using Test Vectors

Digital systems are generally tested by applying a sequence of test vectors. A test vector is a group of signals which are applied (forced) and measured (sensed) on a device or a board. The vector thus defines all inputs and expected outputs for a given test. As we have noted, the sequence of tests performed greatly affects the quality of the overall tests, as measured by the fault coverage.

In general, we can talk in terms of three kinds of vectors. *Simulation* (or application) vectors, *functional* test vectors and *signature* test vectors.

Simulation vectors are generated during the design process. Their main purpose is to help the designer verify that the design has been correctly implemented. They represent the way in which the circuit was intended to operate. When PALASM software (or almost any other PLD design software package) is used, simulation may be performed prior to programming a device. The software simulates the operation of the circuit, and then generates vectors from the simulation, adding the vectors to the JEDEC file. These vectors can then be used for testing by programmers that have the capability of performing functional tests.

While simulation vectors may be adequate for verifying that the design is operating as expected, they generally do not provide very extensive test coverage. For this reason, we distinguish functional test vectors from simulation vectors.

It is very difficult to generate a complete set of functional test vectors by hand; computer programs are generally used instead. The simulation vectors are often used as a basis for generating a more comprehensive set of functional test vectors; in this capacity, the simulation vectors serve as *seed* vectors. There are many programs which perform this function although many of the programs require larger computers and take a long time to run. AMD also generates functional test vectors for patterns that are used in ProPAL devices.

Programs have been developed to generate vectors for use in testing PLDs. These programs use the programming information in the JEDEC file to generate tests.

On most patterns, they can generate test sequences of high quality. If complex internal feedback is used in a particular design, then some manual test generation may still be needed to improve the test coverage. Both of these programs support the use of register preload for initializing states.

While functional vectors provide more extensive tests, they may not exercise the circuit in the manner in which it was meant to be used. Thus, for example, a conditional oscillator in a circuit (as discussed previously) may not be a problem during simulation, since the conditions causing oscillation are not thought to be possible by the designer. However, the functional vectors will take all situations (some of which may not be physically possible) into account in the tests. Thus more subtle design problems may become apparent when functional test vectors are generated.

Signature vectors are random vectors which are first applied to a device which is known to be good in order to generate a "signature". This same set of vectors is then applied to a device of unknown quality; if the same signature results, the device is said to be good; if a different signature results, then the device is assumed to be faulty.

Signature vectors can vary greatly in the quality of testing they can provide. Since they are generated with no knowledge of the circuit being tested, many more vectors must be used to perform a good test. The quality of the test depends on the circuit being tested, the number of vectors used, the speed with which the tests are applied, and the algorithm used to generate the vectors. The tester must also be able to apply a preload sequence to devices that have registers; otherwise two devices may power up into two different states. In that case, both devices will generate different signatures even if both are good devices.

Quality signature testing can be very cost effective, since no advance knowledge of a device pattern is needed. This reduces the amount of resources that must be dedicated to test vector generation.

The different types of vectors are summarized in Table 1 below.

TYPE OF VECTOR	PURPOSE	GENERATED BY:
Simulation (Application)	Used for verifying whether or not a design will operate as expected when implemented.	Sequence defined by the design engineer, usually by hand. Actual vectors generated by design software, placed in the JEDEC file.
Functional	Used for verifying that a device is operating correctly.	Usually generated by a computer program. The simulation vectors can be used as seed vectors
Signature	Used for verifying that a device is operating correctly without functional vectors.	The tester generates the test sequence during the test.

Table 1. Test vectors

SUMMARY

The time to start considering ways of testing a circuit is before the circuit has been designed. The key to testability lies in the way the circuit is implemented.

Basic combinatorial logic can be made completely testable simply by minimizing logic. It is not even necessary to analyze the circuit for redundancy or reconvergent fanout; automatically minimizing all logic will eliminate any occurrences.

Where a sequential circuit is generated from simple feedback paths in the logic, the circuit must be analyzed as a combinatorial circuit. All combinatorial logic must be included to determine whether the circuit is a latch or an oscillator. If a latch is desired, it should be completely controllable. If an oscillator is found, it is probably not desired, and will generally indicate a mistake in the design. If a conditional oscillator is to be tolerated, one must be sure that the oscillation conditions can never occur, and that the test procedure will not cause oscillation.

In general, combinatorial circuits should be analyzed completely for the presence of latches and oscillators (wanted or unwanted). This can be done by simplifying each combinatorial logic block to see whether any signal ultimately depends on itself.

When the sequential nature of a circuit is derived through the use of flip-flops to generate a state machine, the two key issues are initialization and illegal state recovery. A combination of device features and careful circuit design will yield circuits that can behave predictably even in unexpected situations.

It is important to analyze the testability of a circuit before committing it too far. Thus any changes can be made early on. In particular, if the test analysis software points out any logic hazards in your circuit, you can easily remedy them by modifying the design.

These simple steps, taken early in the design phase, can help avoid later redesigns, and ultimately provide a higher quality system.

Finally, the ultimate test quality depends also on the quality of the test sequence used for production, functional test vectors and high quality signature tests will provide you with the highest confidence in the quality of your system.

Ground Bounce

Advanced Micro Devices

INTRODUCTION

The development of fast PAL devices has increased the importance of analog considerations the digital designer has been able to overlook in the past. One of these is ground bounce. Ground bounce refers to the ringing on an output signal when one or more outputs on the same device are being switched from HIGH to LOW. This ringing can be in excess of 3 V. The system cannot consider the data valid until the ringing settles to below the V_{IL} of the receiving devices. The ringing in a fast device can last so long that a slower device with less ground bounce could actually be a faster solution.

The phenomenon of ground bounce is associated with the inductance and resistance of the ground connection in the integrated circuit. As there is always some inductance and resistance, ground bounce cannot be totally eliminated; however, it can be reduced to a level tolerable to the system.

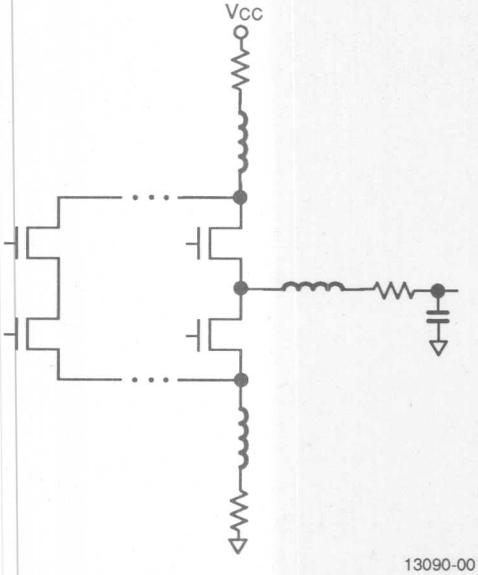
This article will discuss the mechanism of ground bounce in CMOS circuitry and the utilization of slew-rate control used by AMD to keep ground bounce down to reasonable limits.

Mechanism

Figure 1 shows a schematic of an output driver and load including parasitic elements. The load capacitor is charged to the HIGH-level voltage. When the transistor turns on, the capacitor discharges into the transistor and lead impedance. The resultant RLC circuit will have a damped ringing (Figure 2). The peak amplitude depends on the edge rate of the switch and the RLC values, while the frequency of the ringing and the rate of decay depend only on the RLC values.

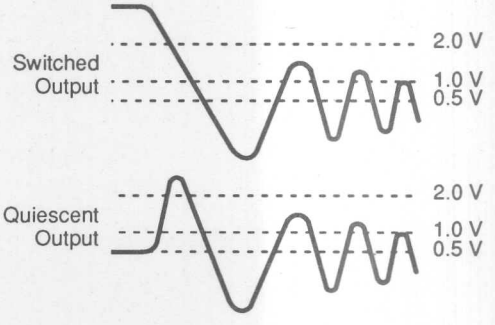
The ringing caused by a single output switching is normally below the LOW-threshold voltage. However, the voltage at the ground pad of the device is proportional to the number of outputs switching simultaneously. In addition, the voltage at the ground pad is coupled to any LOW output through its output transistor. Therefore, if enough outputs switch, ringing on the ground pad will be coupled to LOW outputs, causing the detection of false HIGHs.

Most PAL devices used today have relatively low output drive current: 16 mA or 24 mA. It is tempting to think that the low current level will somehow limit the switching en-



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Figure 1. Simplified Schematic of an Output Driver



13090-002A

Figure 2. Ground Bounce

Publication# 13090 Rev. A Amendment/0
Issue Date: January 1990

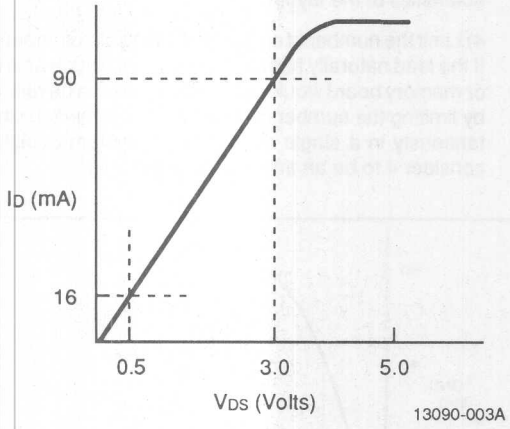
ergy and therefore ground bounce. Actually, even a low-power transistor can pass a relatively large current. The transistor I-V curve in Figure 3a shows that a MOS transistor designed for 16 mA at 0.5 V will pass 90 mA at 3.0 V. Figure 3b shows the V/I path when the output transistor switches between HIGH and LOW. Notice that the transistor switches from 3.5 V at 0 mA to 3.0 V at 90 mA. If eight outputs were to switch simultaneously, 90 mA X 8, or 720 mA, would flow through the ground lead.

This sudden current surge is actually self-limiting. As the ground-pad voltage rises due to the high current change, the internal V_{DS} and the available gate bias voltage are reduced, lowering the drive current. However, the ringing can still exceed 3 V.

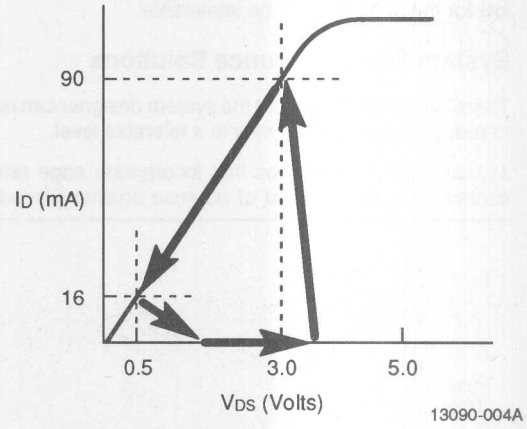
Controlled Edge Rate

The parameters that influence ground bounce are the inductances and resistances of the device, the capacitance of the load, and the edge rate. Of these, the only one that the chip manufacturer can directly control is the edge rate.

Turning on the output-driver transistor is equivalent to switching the charged load capacitor to ground. This can be represented by a step-voltage source in series with the capacitor (Figure 4a). Slowing down the rate that the output transistor can turn on changes the voltage source from a step to a ramp (Figure 4b). With a

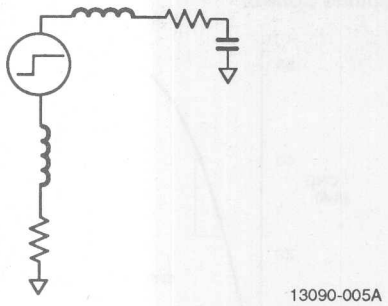


3a. The DC Curve of an Output Driver Transistor

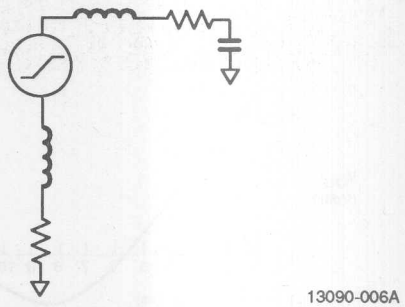


3b. The Path Followed as the Transistor Switches between the HIGH and LOW Levels

Figure 3.



4a. Equivalent Circuit of an Output Driver Transistor with a Capacitive Load



4b. Output Driver Circuit with Slew-Rate Limiting

Figure 4.

shallower slope, less energy is available for ringing and the ground-bounce amplitude is reduced.

A Spice simulation (Figure 5) illustrates the effect. The device without risetime control will have a very high charging current with a large di/dt: 2.1 X 10^7 A/s. Risetime control reduces the di/dt about 25%. This will result in a corresponding reduction in the voltage that can develop across the ground inductance.

AMD has a proprietary technique that slows the edge rate of the output transistor, thereby reducing the amplitude of the ringing. Slowing down the fall time will add about a nanosecond to the output delay, but the system speed will still be greatly increased. On a high-capacitance load, a non-edge-rate-controlled device could ring for more than 25 ns. The additional delay required to allow for the ringing would be intolerable.

System Ground Bounce Solutions

There are some things that the system designer can do to reduce the ground bounce to a tolerable level.

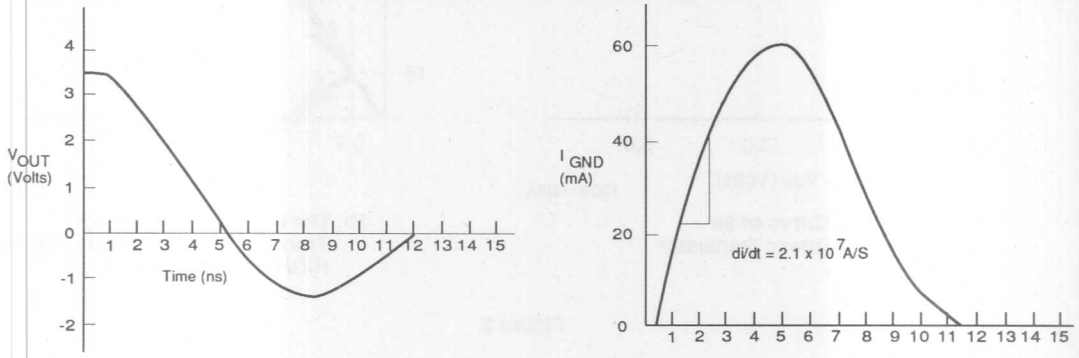
1) Use AMD PAL devices that incorporate edge rate control. This the first line of defense against ground-bounce-related problems, and the most effective.

2) Use shorter lead packages. The bonding wires in a PLCC are 1/4 the length of the ground bonding wire in a DIP. The inductance is reduced proportionally. Any reduction in inductance will reduce the amplitude of the ringing.

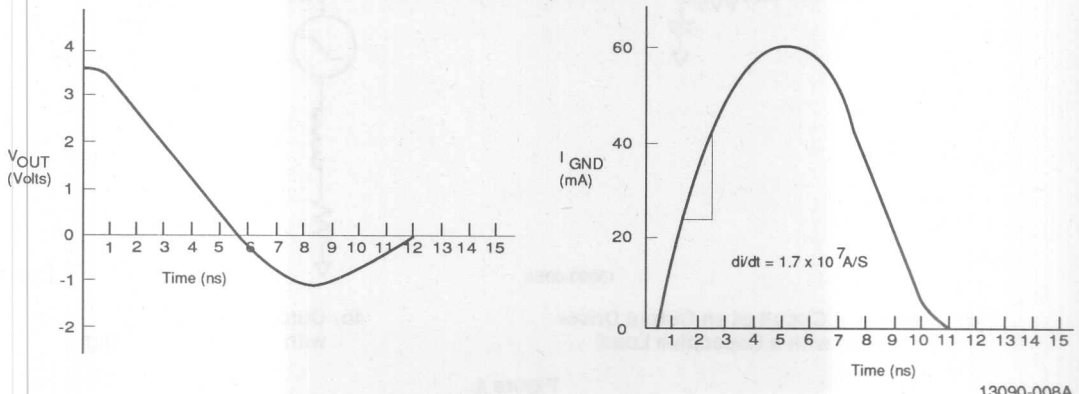
Some devices have center power and ground pins. The ground pin will be substantially shorter and have a proportionately reduced inductance. This will reduce the coupling between outputs. A good example is the PALCE26V12.

3) Reduce capacitive loading. Capacitive loading in any system should be reduced as much as possible. This may involve consideration of the transmission line characteristics of the layout.

4) Limit the number of outputs switching simultaneously. If the load naturally has high-capacitance such as a bus or memory board would, ground bounce can be reduced by limiting the number of outputs that can switch simultaneously in a single device. Many system designers consider 4 to be an acceptable upper limit.



5a. Without Risetime Control



5b. With Risetime Control

Figure 5. Effect of Risetime Control

Metastablility

Advanced Micro Devices

INTRODUCTION

A significant number of digital systems must deal with inputs not synchronized to their own internal clocks. These asynchronous signals can arise from any of the various asynchronous protocols, such as are often used in bus designs; they can be the result of trying to share signals from systems with different clocks; or they may be the response of a system user, who is of course not synchronized with the system. The result can be metastability, a problem which can plague unwary designers. It is not a newly discovered phenomenon, but is normally dealt with somewhat qualitatively, and, unfortunately, is usually ignored as much as possible.

Causes of Metastability

The flip-flop setup time is the parameter that is most often at the root of metastability. The setup time is basically a requirement that data be made available at the input to the flip-flop before the clock signal arrives. The data must not only be there, but must also be stable.

In a PAL device, the use of an array for the data adds to the setup time. The data passes through the array on its way to the flip-flop (Figure 1). The clock signal, on the other hand, goes directly from the clock pin to the flip-flop. Its path is much shorter than the data path. The setup time is therefore essentially a requirement that the data signal must be given more time to get to the flip-flop before the clock signal.

If the published setup time is satisfied, the data arrives at the flip-flop well before the clock, and the output to the flip-flop will change as desired (Figure 2). If the setup time is violated, then no guarantee can be made about what the output will do. The output may be normal, since the published setup time is a worst-case number. However, if the timing between the clock and data is just right, the output will be unstable for some time before it

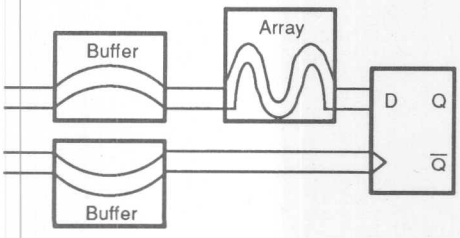


Figure 1. The clock and data paths in a PAL device

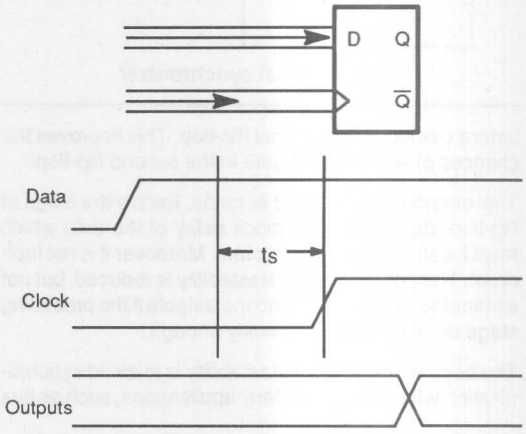


Figure 2. Output response when the setup time is satisfied

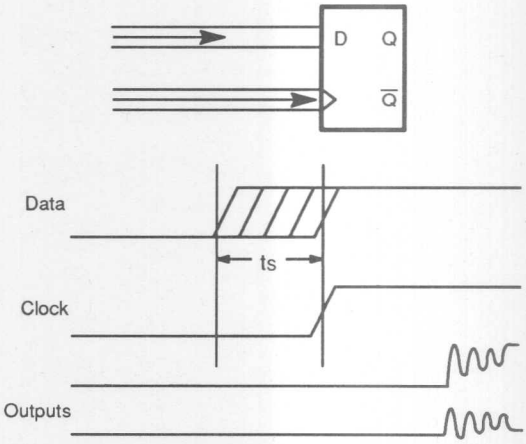


Figure 3. Possible output response when the setup time is violated

settles into some state. Neither the time the output remains unstable nor the final state is predictable (Figure 3). This condition is metastability.

Ways of Dealing with Metastability

The most common way of dealing with this problem is to synchronize the inputs with an extra flip-flop (Figure 4). If the first flip-flop goes metastable, hopefully the delay between clock pulses will allow the ringing to die down

Publication# 14104 Rev. A Amendment/0
Issue Date: January 1992

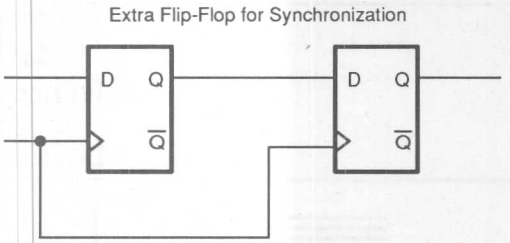


Figure 4. Dual synchronizer

before clocking into the next flip-flop. This improves the chances of having good data in the second flip-flop.

This method is not without its costs. Each extra stage of flip-flop means an extra clock delay of the data which must be absorbed by the system. Moreover it is not foolproof. The possibility of metastability is reduced, but not eliminated. A flip-flop can go metastable if the preceding stage does not recover quickly enough.

The best way to avoid metastability is to avoid synchronization when possible. Many applications, such as bus arbitration schemes, use synchronization not because synchronization itself is necessary, but because it provides the only convenient way to store data. This unfortunately takes a system that is inherently asynchronous and adds some synchronizing elements in the middle.

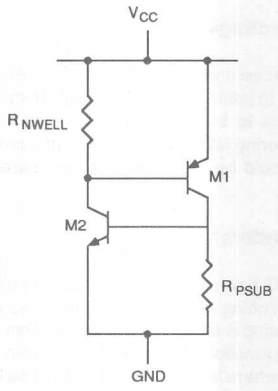
Summary

Metastability can occur in a number of different kinds of asynchronous systems, usually due to the inability to guarantee that the setup time of the flip-flops will be satisfied. In standard synchronous systems, where the setup time (along with all other timing requirements) is specifically designed in, metastability will never be a problem.

In some situations, metastability is caused by the need to interface systems with different clocks. In this case, it will never be possible to completely eliminate the possibility of metastability. Instead, the designer must take steps to reduce the probability of a system failure due to metastability.

Latchup Circuit

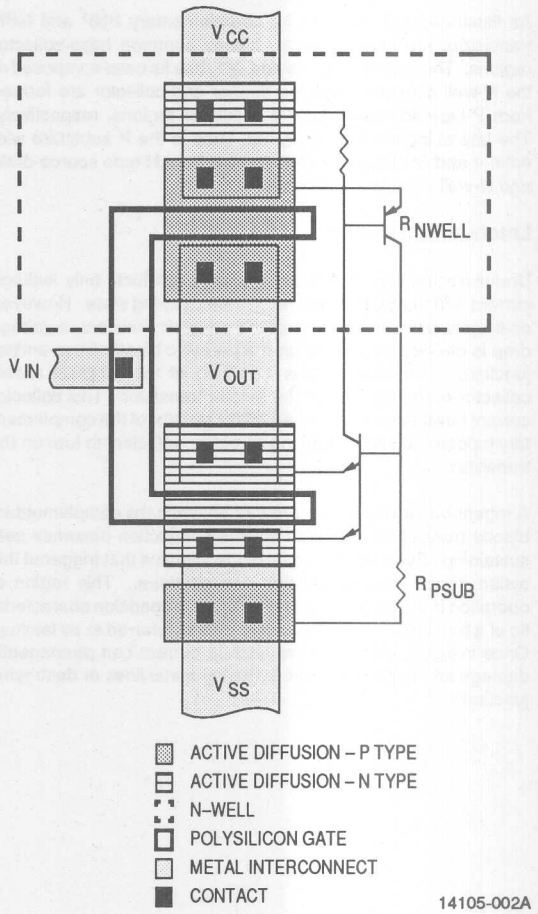
Latchup is caused by an SCR (Silicon Controlled Rectifier) circuit. Fabrication of CMOS integrated circuits with bulk silicon processing creates a parasitic SCR structure. The behavior of this SCR is similar in principle to a true SCR. These structures result from the multiple diffusions needed for the formation of complementary MOS transistors in CMOS processing. The SCR structure consists of a four layer device formed by diffused PNPN regions. These four layers create parasitic bipolar transistors illustrated in Figure 1.



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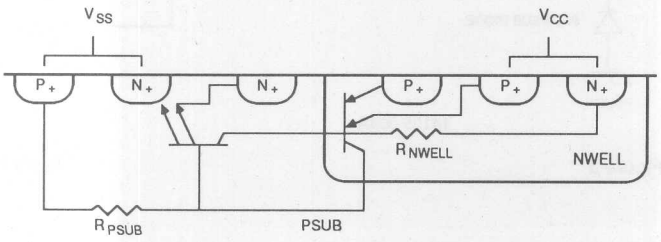
Figure 1

Figure 2a shows a typical CMOS inverter layout with the schematic of the parasitic bipolar SCR structure. Figure 2b is a cross sectional representation of the CMOS inverter, again with the schematic of the bipolar SCR structure.



14105-002A

Figure 2a



14105-003A

Figure 2b

to which the resistors resist current flow depends upon geometric size and doping level.

As illustrated in Figure 1, the complementary PNP and NPN transistors are cross-coupled, having common base-collector regions. The vertical PNP device, M1, has its base composed of the N-well diffusion while the emitter and collector are formed from P-type source-drain and substrate regions, respectively. The lateral bipolar transistor, M2, base is the P substrate with emitter and collector junctions formed from N-type source-drain and N-well diffusions, respectively.

Latchup Conditions

Under normal bias conditions the SCR conducts only leakage current and the SCR structure is in the blocking state. However, as current flows across any of the parasitic resistors, a voltage drop is developed, turning on the parasitic bipolar base-emitter junction. The forward bias condition of this junction allows collector current to flow in the bipolar transistor. This collector current flows across the base-emitter resistor of the complementary bipolar transistor, creating a voltage sufficient to turn on the transistor.

A regenerative loop is now created between the complementary bipolar transistors such that current conduction becomes self-sustaining. Even after removal of the stimulus that triggered this action, the current conduction can continue. This region of operation is a high-current, low-resistance condition characteristic of a four layer PNPN structure. This is referred to as latchup. Once initiated, the excessive latchup current can permanently damage an integrated circuit by fusing metal lines or destroying junctions.

discussed. These include power up, supply overvoltage, and overshoot/undershoot at device pins.

Power-Up

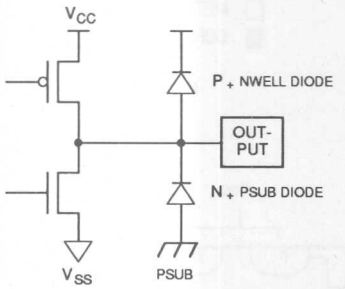
Caution must be exercised when powering up CMOS ICs to avoid driving device pins before the supply voltage has been applied to the circuit. Placing a device or board in a "hot socket" will create this situation. When subjected to hot socket insertion, voltage conditions at the device pins are uncertain such that the input diodes may be forward biased. Forward biasing the input diodes with a delayed or uncontrolled application of V_{CC} could cause the device to latch up. Advanced Micro Devices' CMOS circuits have substantial immunity to hot-socket power up, but since this condition is uncertain, and difficult to characterize, test, and guarantee, it should be avoided.

Supply Overvoltage

Supply levels exceeding the absolute maximum rating can cause a CMOS circuit to latch up. Elevated supply voltage may cause internal junctions to break down, producing substrate current capable of triggering latchup. Latchup is just one of the reasons overvoltage should be avoided; other undesirable effects may result from this.

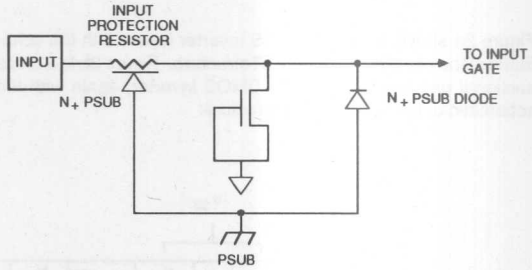
Overshoot/Undershoot

Generally the I/O pins experience the noisiest electrical environment. Fast switching signals with a large capacitive load may overshoot, creating a transient forward bias condition at the I/O junction. These junction diodes are illustrated in Figures 3 and 4. Typically this is where latchup is most likely to be induced. Proper design of the input and output buffers is essential to minimize the risk of latchup due to overshoot.



14105-004A

Figure 3



14105-005A

Figure 4

Testing For Latchup

Advanced Micro Devices characterizes the latchup sensitivity of its devices before they are released to the market. Testing is done in such a way as to completely cover every possible latchup condition, including V_{CC} overvoltage, pin overcurrent, and pin overvoltage.

V_{CC} Overvoltage Test

The V_{CC} overvoltage test is applied to all power (V_{CC}) pins. The test is performed at the highest guaranteed operating temperature of the device. All inputs and I/Os acting as inputs are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open).

V_{CC} max is applied to the V_{CC} pin. A positive high voltage pulse is then applied to the V_{CC} pin and returned to V_{CC} max. The occurence of latchup is detected if the voltage across the device is less than V_{CC} max, and the current through the device is greater than the normal DC operating current.

Pin Overcurrent Test

The pin overcurrent test is performed on every output, I/O pin, and non-current-limited input pin. Non-current-limited inputs are inputs which present a diode-like (or otherwise "infinite") current characteristic for input voltages in the range $(GND - 5\ V) < Vin < (V_{CC} + 5\ V)$.

The pin overcurrent test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs should be floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. A three-state output under test should be disabled. A non-three-state output type under test should be a logic High when applying a positive current and a logic Low when applying a negative current. An I/O pin should be placed into the input mode.

A high current pulse is then applied to the pin under test. The magnitude of the pulse is stepped until latchup is induced. Both positive and negative currents are tested. Latchup is observed as described previously. The sensitivity of the device is the worst case sensitivity found on any pin of the device.

Pin Overvoltage Test

The pin overvoltage test is performed on current-limited inputs. Current-limited inputs are inputs which present a resistor-like (or otherwise "limited") current characteristic for input voltages in the range $(GND - 5\ V) < Vin < (V_{CC} + 5\ V)$.

The pin overvoltage test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. Both positive and negative voltage pulses are applied to the pin under test. Latchup is observed as described previously. The sensitivity of the device is the worst-case sensitivity found on any pin of the device.

Converting Bipolar PLD Designs to CMOS

Application Note

by Bryon Moyer

Advanced Micro Devices

The world learned about programmable logic through the use of bipolar PLDs. As PAL device designs proliferated, bipolar fuse technology was the only production-worthy vehicle for implementing the programming feature. As CMOS floating-gate technology was adapted to programmable logic, CMOS has increasingly become the technology of choice for new system designs. By using CMOS, bipolar speeds can be attained with lower power consumption. Electrical erasability joins a number of other reasons why designers now prefer CMOS.

Today bipolar PLDs are being purchased largely to supply those designs that were done before CMOS was viable. Many systems makers are now looking for ways to convert their production systems to CMOS. The intent is always to have a seamless, "engineeringless" transition, or as close to that as possible. Few companies have access to the engineers that designed a system five years earlier. The purpose of this application note is to discuss issues that may arise when converting a socket from a bipolar PLD to its CMOS equivalent.

In theory, when converting from a bipolar device to a CMOS device, either of the two should work in the socket. In practice this is true for most designs, especially those that have been well adapted for high-speed signals. **Most designs will not require that you take any special actions**. It is only with more sensitive designs that one may have some applications issues to deal with.

The conversion issues discussed apply to devices from any manufacturer; the specific solutions apply primarily to AMD PAL devices. In particular, this article focuses on conversion where there is a direct CMOS architecture counterpart to the bipolar device, as shown in Table 1. For bipolar architectures where an exact CMOS equivalent is not available, or when using other CMOS architectures, additional logic design work may be needed. For more information on the CMOS architectures available, please refer to the application note *Selecting the Correct CMOS PLD*.

There are a number of specific areas that need to be discussed for those designs that may have an easy architectural conversion, but more difficult electrical conversion. They are:

- Floating unused input pins
- Edge rates, termination, and layout
- Overshoot
- Ground bounce

In addition, the issue of checksum consistency will be addressed where there is a chance of the checksum changing as a result of a conversion.

Table 1. Bipolar/CMOS Direct Equivalents

Bipolar Device	CMOS Equivalent	Bipolar Device	CMOS Equivalent
PAL16R8	PALCE16V8	PAL20R8	PALCE20V8
PAL16L8		PAL20L8	
PAL16R4		PAL20R4	
PAL16R6		PAL20R6	
PAL10L8		PAL12L10	
PAL10H8		PAL14L8	
PAL12L6		PAL16L6	
PAL12H6		PAL18L4	
PAL14L4		PAL20L2	
PAL14H4		PAL22V10	PALCE22V10
PAL16L2		PAL20RA10	PALCE20RA10
PAL16H2			

Floating Unused Input Pins

No input to a digital device likes to see its value kept at the threshold voltage for any length of time. These inputs expect a high or low signal level; the input signal should switch quickly and smoothly from one state to another, passing cleanly through the threshold voltage. If an input lingers too long at threshold, the input transistors will be in the active region, and, essentially being high-gain amplifiers, may oscillate as they decide whether they should be high or low.

On a PAL device, this oscillation will not typically cause any first-order problems on unused pins. However, since this oscillation involves the rapid switching of a lot of current, it could generate internal ground noise, and affect other internal circuits.

Bipolar devices tend to pull unused input pins to a high state. Many designers count on this to give their unused pins a default level, although it is not a recommended practice. Despite pull-up capability (typically 50 kΩ – 100 kΩ effective), a standard TTL input will only pull up to at most a diode drop above threshold, as shown in Figure 1. In the presence of noise, the input can start to move across threshold and cause some disturbances.

Publication# 17764 Rev. A Amendment/0
Issue Date: April 1993

It is therefore always better to tie an unused pin high or low on the board.

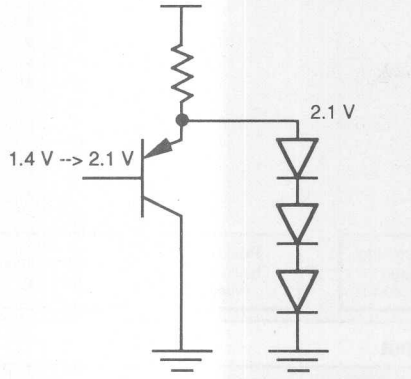
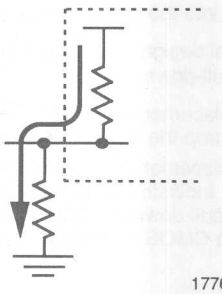


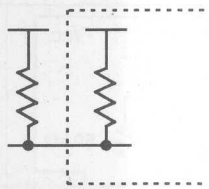
Figure 1. A Typical Bipolar Input. All Voltages Are Nominal.

When tying a pin high or low, a resistor is not needed. However, many designers feel safer putting in a current-limiting resistor to protect the system if there is an accidental short on the pin. In addition, the resistor allows the pin to be used later without needing to break the pull-up or pull-down connection.

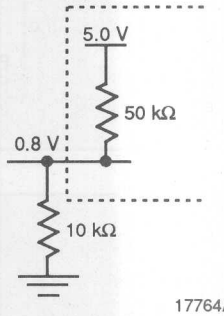
It often makes no difference whether an unused input is tied high or low. However, when using a device with internal pull-up capability, tying high can save some power. If an input has a pull-up and is tied low, then up to 100 µA will be expended through the input. In addition, care must be taken to make sure that V_{IL} is not exceeded when tying an unused pin low through a resistor. The external resistor will form a voltage divider with any on-chip pull-up. With a 50-kΩ internal pull-up, a 10-kΩ pull-down will bias the input at 0.8 V (maximum V_{IL}) if V_{CC} is 5.0 V. This is the maximum pull-down that should be left intact if the input has a built-in pull-up.



a. Current Flows if Pull-Down Used



b. No Current if Pull-Up Used



c. Pull-Down Forms a Voltage Divider

Figure 2. External Pull-Up/ Pull-Down Configurations

Traditional CMOS devices have absolutely no pull-up or pull-down, so the pin is truly floating. Therefore it is completely at the mercy of leakage and noise as it seeks out some default level. Recent CMOS PAL devices from AMD have pull-up resistors that provide a default high level. The input will be pulled to about a diode drop below V_{CC}, giving sufficient noise margin. The minimum effective pull-up resistance is 50 kΩ, so it is still a high impedance input. Thus it is still a good idea to tie such an unused pin high for maximum noise immunity. The equivalent input schematic on the data sheet will indicate whether or not the product has built-in pull-up resistors.

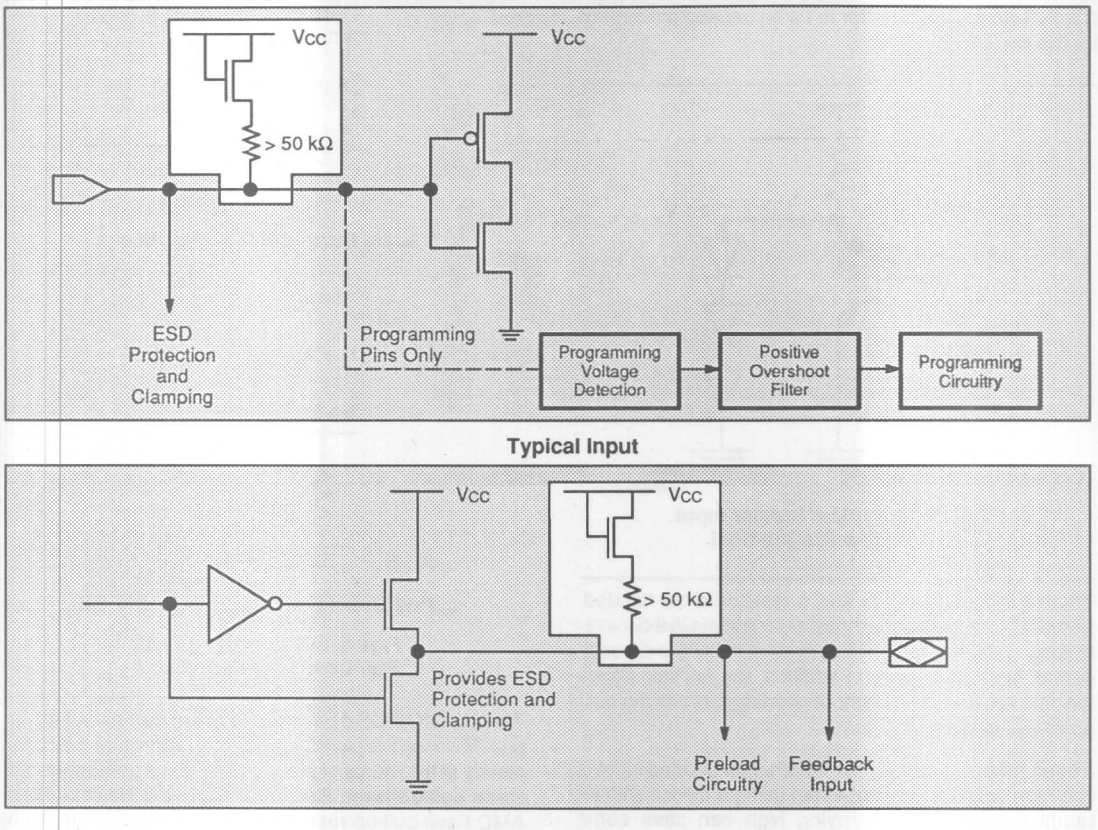


Figure 3. Input Pull-Up Resistors as Shown in the Datasheet

This discussion applies primarily to unused input pins. There actually are three basic kinds of pin on a PLD: input, output, and I/O. If an output pin is unused and has no three-state capability, then the output will be high or low, and does not need any external pull-up or pull-down. If the pin is an I/O pin, or an output with three-state, then the action taken depends on the default state of the unused I/O pin. Most software packages configure unused I/O pins as inputs; in this case, the I/O pin should be treated just like an input. If the I/O pin is configured like an output, then no extra action is needed. Note that PALASM software normally configures unused I/O pins as inputs; in the case of MACH devices, however, the software gives the option of configuring unused I/O pins as outputs instead.

What To Do

What action you take when converting from bipolar to CMOS depends on the original design.

- If the original design has unused pins tied directly to V_{CC} or ground, then the new device can simply be dropped into the old socket.
- If the original design has unused pins tied high through a resistor, then the new device can simply be dropped into the old socket.
- If the original design has unused input pins tied low through a pull-down resistor:
  - — if the replacement part has no internal pull-up resistors, drop the CMOS part into the socket
  - — if the replacement part has internal pull-up resistors (as indicated in the data sheet), and the board's pull-down is less than about 10 kΩ, then drop the CMOS part into the socket

— if the replacement part has pull-up resistors (as indicated in the data sheet), and the board's pull-down resistor is greater than 10 kΩ, then either remove the pull-down resistor when using the new CMOS part or replace it with a smaller resistor.

- If the original design has unused pins that are floating, be sure to use one of AMD's newer CMOS devices that have pull-up resistors built in.

Edge Rates, Termination, and Layout Sensitivity

Edge rates are important when converting from bipolar to CMOS. While there are exceptions, CMOS devices tend to have faster edge rates than their bipolar equivalents. The edge rates determine whether or not a signal needs termination. The faster the edge rate is, the more a PCB trace looks like a transmission line, which can generate reflections that impact system performance. More information on these issues is available in the Application Note *High-Speed Board Design Techniques*.

With slow edge rates, long traces can be fabricated with no need for termination. As edge rates speed up, even short traces will need termination. There is no standard cutoff, and the need for termination will depend on many variables. These include PC board materials, layout, the number and kind of other components on the line, and the amount of noise that the design can tolerate. If a design is marginal with respect to edge rate sensitivity, then any changes in the edge rate of the component in that socket can affect the behavior of the system.

As an example, the maximum unterminated line length for a particular trace may be 2"–4" with a 1.5-ns rise-time device, but 4"–7" with a 3-ns rise-time device. If a particular trace is 5" long, it is within the window for the slower device, and might work. But this definitely qualifies as marginal. If a replacement device has a 1.5-ns rise time, then this 5" line is now outside the allowable window for the faster device, and will require termination.

Design sensitivity to edge rates is also affected by layout. The following items can contribute to increased noise in a system, and therefore may make it harder to replace one device with another that has a faster edge rate.

- 90° corners: these are impedance discontinuities. Use two 45° corners instead. The ideal is to have a rounded corner.
- Long unterminated stubs: these can introduce reflections onto a line that may be otherwise terminated at the end. Keep the stubs shorter than the maximum critical line length. If they must be longer, then they will have to be individually terminated. Note that multiple DC terminations on a single line may severely impact the DC loading on the drivers.
- Too many vias (feedthroughs): each of these is a discontinuity. While some vias may be necessary for routing, use as few as possible. Do not route between an outside layer and an inside layer on multilayer boards.
- Headers, sockets, and other components that act as discontinuities: these should be used as sparingly as possible, since they can cause reflections, excessive EMI, and add to the inductance of the line.
- Poorly decoupled V_{CC} and ground: this can sabotage the best attempts at termination. Good termination relies on a solid ground system, and any noise being carried on the V_{CC} or ground can make its way onto signals. It can also make an otherwise perfect termination ineffective, causing reflections.

What To Do

When converting from bipolar devices to CMOS devices in a given design, the following considerations apply, depending on how the original PAL device output is terminated.

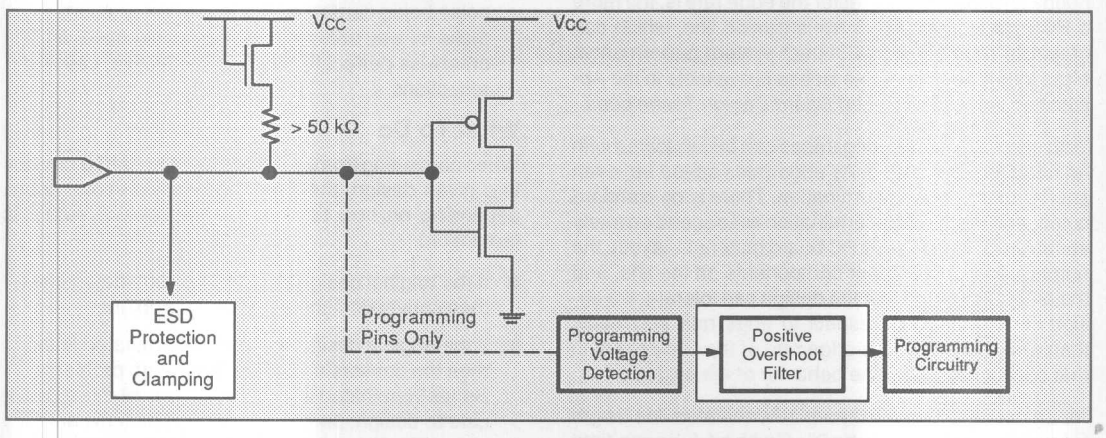
- If the original design has parallel-terminated lines, then conversion should pose no problem.
- If the original design has series-terminated lines, then the conversion will likely pose no problems. Series-terminated lines tend to be a bit more delicate to design; parallel-terminated designs are generally more robust, but cause greater power dissipation.
- If the original design has no termination, but the CMOS device has a slower edge rate than the bipolar device (as in the case of the 10-ns 22V10, for example), then the conversion should pose no problem.
- If the original design has no termination and the CMOS device has a faster edge rate than the bipolar device, then your action depends on the length of the trace. No absolute rule can be given, but the following rules of thumb should generally be safe:
  - — if the line is longer than about 5 inches, add termination.
  - — if the line is shorter than 2 inches, the direct conversion will likely work.
  - — if the line is between 2 and 5 inches, try the direct conversion, but be prepared to add termination if noise proves to be excessive.

In general, terminate if you feel that it will save you future headaches.

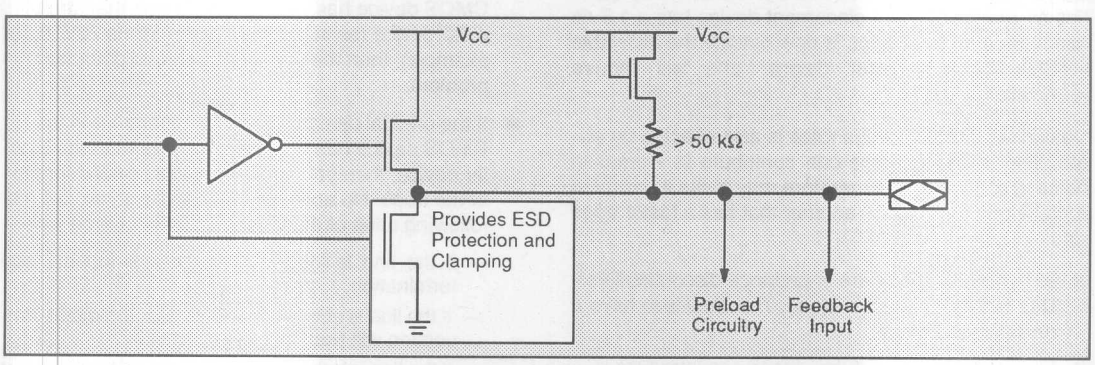
Overshoot

A design that is well terminated will likely have very little overshoot. As reflections grow, overshoot increases in both the positive and negative direction (note that "negative overshoot" is sometimes called "undershoot", although this is technically a misnomer). The effects of overshoot on inputs to a PAL device differ depending on whether it is positive or negative overshoot.

- Negative overshoot: AMD's CMOS devices on EE4 technology or later (comprising all of the bipolar-equivalent devices being manufactured today) are able to clamp negative overshoot effectively. Details can be found in the Application Note, *Inside AMD's CMOS PLD Technology*. Even in the presence of large amounts of negative overshoot, no anomalous behavior has been observed in AMD's CMOS products. Negative overshoot should pose no conversion problem.
- Positive overshoot: this can be an issue if the CMOS device used in the replacement has no positive overshoot filter. Not all PLD manufacturers use overshoot filters, but all of AMD's bipolar-equivalent CMOS devices are being given overshoot filters; with these filters, positive overshoot will pose no conversion problems. The equivalent input schematic in the data sheet will indicate whether or not a device has overshoot filters.



Typical Input



Typical Output

17764A-5

Figure 4. Overshoot Clamping and Filters as Shown in the Datasheet

Ground Bounce

CMOS devices of any kind have a reputation of causing more ground bounce than their bipolar counterparts. While this is changing on AMD's fastest devices, it is generally true on many devices. The actual amount of ground bounce encountered will depend on the output loading and the number of outputs switching. The more current being switched, whether due to more outputs or heavier loads, the greater the ground bounce may be.

AMD's newer CMOS devices have a special design that uses a split leadframe, as conceptualized in Figure 5. This technique allows for CMOS devices with less ground bounce than their bipolar equivalents. This means that faster CMOS devices will be possible without ground bounce making them unusable.

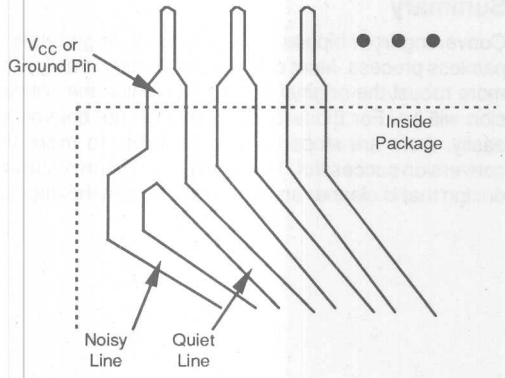


Figure 5. Conceptualization of Split V_{CC} and Ground Leads

What To Do

When converting from bipolar to CMOS, the following ground bounce considerations apply.

- If the CMOS replacement part has a split leadframe design (as indicated in the data sheet), then there will likely be no conversion issue (the PALCE22V10H-7 is presently the best example of this).
- If the outputs in the design are lightly loaded, then there will likely be no conversion issue. While the amount of loading that can be tolerated will vary from design to design, outputs with 75–100 pF or greater should be considered heavily loaded.
- If the design has few outputs switching at a time, then there will likely be no conversion issue.
- If many outputs switch at a time, or if the loads are heavy, the conversion may work just fine anyway; try it, but observe ground and signal conditions closely to see if any design modifications will be needed.

In the last case, design changes may be difficult to accomplish, depending on the amount of ground bounce, the design flexibility, and the availability of engineering resources. Such changes will likely require more substantial board changes than a simple conversion would require, and may not be feasible. If design changes are possible, however, the following are some things to try.

- Reduce the loading on the outputs.
- If using DIP packages, switching to PLCC packages instead may help. PLCC packages have shorter, more uniform, lower-inductance leads, and offer lower ground bounce.
- Keep the board-level ground inductance as low as possible to make sure that board-level ground bounce does not exacerbate any internal chip ground bounce.
- Try to reduce the number of outputs switching. This may be difficult in many designs, but a good candidate for this would be a state machine. If the existing state bit assignment has transitions that switch many outputs at once, try redoing the state bit assignment so that fewer simultaneous transitions occur. Please refer to the Application Note, *Basic Design with PLDs* for more information on tailoring state machines.

Keeping Consistent Fuse Checksums

As shown in Table 1, direct bipolar conversions can only be made between 16XX families and the 16V8; 20XX families and the 20V8; the bipolar and CMOS 22V10s; and the bipolar and CMOS 20RA10s. In the last two cases, the architectures are identical, and there will be no fuse checksum inconsistencies between the bipolar and CMOS versions.

Note that there are actually two checksums in a JEDEC file: the fuse checksum and the transmission checksum. Only the fuse checksum reflects the array contents specifically, and is usually the only one of interest. Transmission checksum changes will occur if anything at all in the JEDEC file changes—even a comment; this may not reflect any functional change to the pattern, and can generally be ignored. For more information on checksums, please refer to JEDEC Standard 3.

In the case of the 16R8 families and the 20R8 families, individual bipolar architectures are converted to a single universal CMOS architecture: the 16V8 and 20V8, respectively. The CMOS devices have extra architecture bits that determine the macrocell configuration. For example, the 16V8 can be configured differently to emulate a 16R4 or a 16L8 (as well as other architectures).

Because of this, the CMOS equivalent will generally have a different fuse checksum from the bipolar original.

If all outputs on a device are used, then converting from bipolar to CMOS will give a consistent CMOS checksum, regardless of which software performs the conversions (of course, this checksum will be different from the original bipolar one). However, if some outputs are not used, then software defaults generally determine how the unused architecture bits are set. Different software programs may have different defaults; therefore they may generate different checksums for the same design.

Note that it is also possible to perform these conversions directly through cross-programming with no apparent change in checksum. However, this is not recommended as a long-term conversion mechanism, since it makes the production file being used inconsistent with the original source file. Cross-programming does not change the source file or the original JEDEC file.

What To Do

To convert designs with unused outputs, the following procedure is recommended if a consistent checksum is needed. The solution shown below uses PALASM syntax; similar equations can be specified in any PLD compiler.

1. Obtain the original source file. If the original source file is unavailable, then disassemble the JEDEC file to obtain a source file.
2. Change the device type in the source file from the original bipolar device type to the 16V8 or 20V8, as appropriate.
3. For each unused output, add a "dummy" equation as follows:

   for a combinatorial output, add

   ```
   OUTPUT.TRST = GND
   ```

   ```
   /OUTPUT = GND
   ```

   for a registered output, add

   ```
   /OUTPUT := GND
   ```

4. Recompile the design.

Summary

Converting from bipolar to CMOS PLDs is generally a painless process. Most designs can convert easily. The more robust the original design, the easier the conversion will be. For those designs that do not convert as easily, there are steps that can be taken to make the conversion successful. These steps can often result in a design that is cleaner and more robust than the original.

High-Speed-Board Design Techniques

Advanced Micro Devices

Application Note

INTRODUCTION

The most important factor in the design of many systems today is speed. 25-MHz processors are common; 40- and 50-MHz processors are becoming readily available. The demand for high speed results from: a) the requirement that systems perform complex tasks in a time frame considered comfortable by humans; and b) the ability of component manufacturers to produce high-speed devices. An example of a) is the large amount of information that must be processed to perform even the most rudimentary computer animation. Currently, Programmable Array Logic (PAL) devices are available with propagation delays of 4.5ns. While this might seem fast, it is not the propagation delay that creates the potential for problems, but rather the fast edge rates needed to obtain the fast propagation delays. In the future, much faster devices will become available, with correspondingly faster edge rates.

Designing high-speed systems requires not only fast components, but also intelligent and careful design. The analog aspect of the devices is as important as the digital. In high-speed systems, noise generation is a prime concern. The high frequencies can radiate and cause interference. The corresponding fast edge rates can result in ringing, reflections, and crosstalk. If unchecked, this noise can seriously degrade system performance.

This application note presents an overview of the design of high-speed systems using a PC-board layout. It covers:

- the power distribution system and its effect on board-noise generation,
- transmission lines and their associated design rules,
- crosstalk and its elimination, and
- electromagnetic interference.

1. POWER DISTRIBUTION

The most important consideration in high-speed board design is the power distribution network. For a noise-free board, it is necessary to have a noise-free power distribution network. Note that it is just as important to develop a clean V_{CC} as it is to get a clean ground. For AC purposes, which is what this application note mainly discusses, V_{CC} *is* ground.

The power distribution network also must provide a return path for all signals generated or received on the board. This is often overlooked because the effect of the return path is less apparent at lower frequencies. Many designs work even when the nature of the return path is ignored.

1.1 Power Distribution Network as a Power Source

1.1.1 The Effect of Impedance

Consider a 5" x 5" board with digital ICs and a power supply of +5.0 V. The goal is to deliver exactly +5.0 V to the power pins of every device on the board, regardless of its position relative to the power source. Furthermore, the voltage at the pins should be free of line noise.

A power source with these characteristics would be schematically represented as an ideal voltage source (Figure 1a), which has zero impedance. Zero impedance would ensure that the load and source voltages would be the same. It also would mean that noise signals would be absorbed because the noise generators have finite source impedance. Unfortunately, this is only an ideal.

Figure 1b illustrates a real power source with associated impedances in the form of resistance, inductance, and capacitance. These are distributed over the power distribution network. Because of the network's impedance, noise signals can add to the voltage.

The design goal is to reduce the power distribution network impedances as much as possible. There are two approaches: power buses and power planes. Power planes generally have better impedance characteristics than power buses; however, practical considerations might favor buses.

Publication# 16356 Rev. A Amendment/0
Issue Date: February 1993

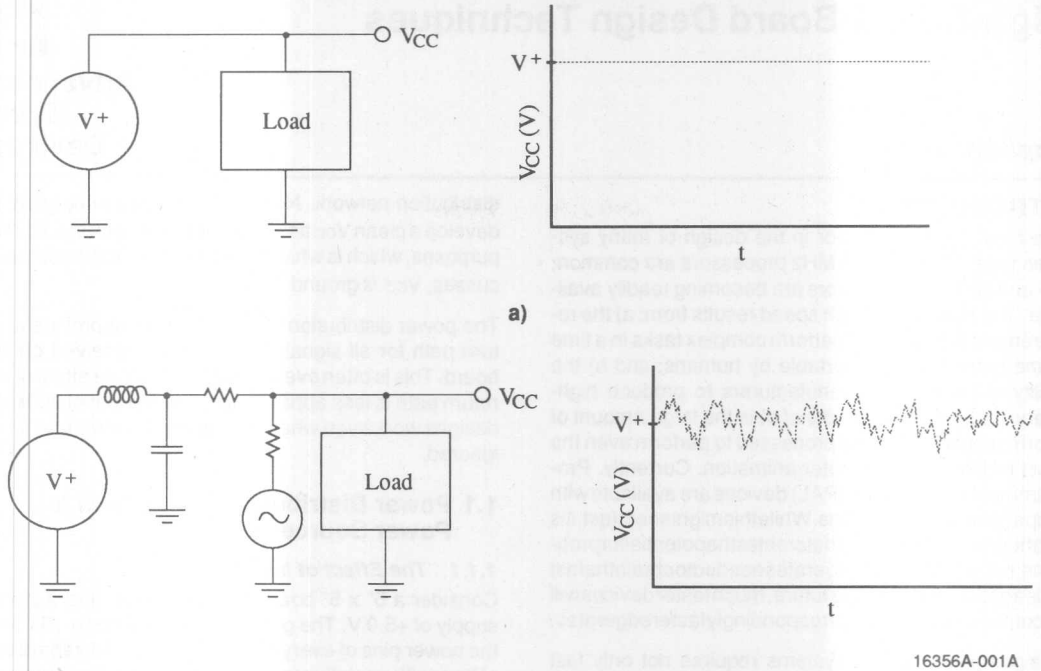


Figure 1. The Power Source. a) Ideal Representation; b) More Realistic Representation

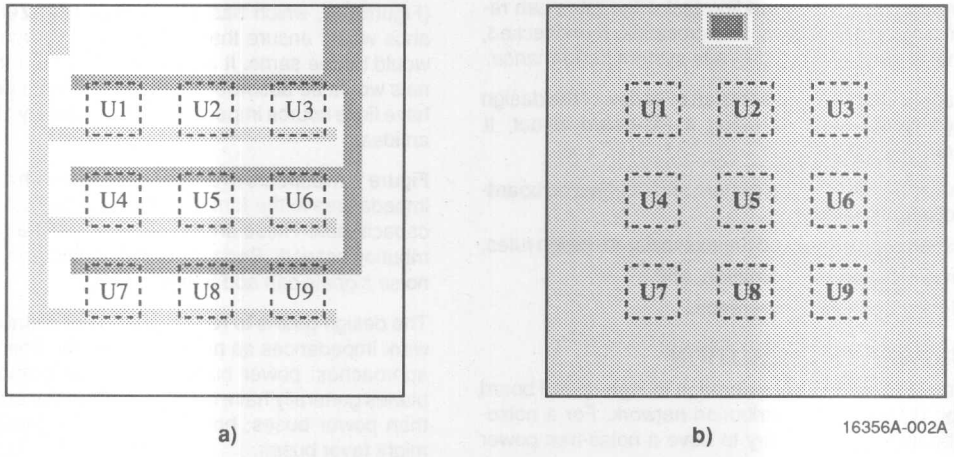


Figure 2. Power Distributions System. a) Power Buses; b) Power Planes

1.1.2 Power Buses vs Power Planes

Two power-distribution schemes are shown in Figure 2. A bus system (Figure 2a) is composed of a group of traces with the various voltage levels required by the system devices. For logic, these are typically +5 V and ground. The number of traces required for each voltage level varies from system to system. A power-plane system (Figure 2b) is composed of entire layers (or sections of layers) covered with metal. Each voltage level requires a separate layer. The only gaps in the metal are those needed for placing pins and signal feed-throughs.

Early designs favored buses because of the expense of devoting entire levels to power distribution. The power

bus shares layers with the signal lines. The bus must supply power to all devices, while leaving room for the signal traces; therefore, buses tend to be long, narrow ribbons. This results in a relatively small cross-sectional area with a small resistance.

Although the resistance is small, it is significant. Even a small board can have 20 to 30 devices on it. If each device on a 20-device board sinks 200 mA, the total current would be 4 A. A bus resistance of only 0.125 Ω has a 0.5 V drop. With a 5 V power supply, the last device on the bus might receive only 4.5 V.

Because the power plane fills an entire layer, the only area constraints are the dimensions of the board. The resistance of a power plane is a small fraction of that of a power bus supplying the same number of devices. Thus a power plane is more likely than a bus to supply full power to all the devices.

On a bus, currents are restricted to paths defined by the bus. Any line noise generated by a high-speed device is introduced to other devices on that power bus. On the board in Figure 2a, noise generated by U9 is sent to U7 by the bus.

On the power plane, the noise currents are distributed because the current path is not restricted. This, along with lower impedance, makes power planes quieter than power buses.

1.1.3 Line Noise Filtering

The power plane alone does not eliminate line noise. Since all systems generate enough noise to cause problems, regardless of the power distribution scheme, extra filtering is required. This is done with bypass capacitors. Generally, a 1 µF to 10 µF capacitor is placed across the power input to the board, and 0.01 µF to 0.1 µF capacitors are placed across the power and ground pins of every active device on the board.

The bypass capacitor acts as a filter. The larger capacitor (≈ 10 µF) is placed across the power input of the board to filter lower frequencies (like the 60-Hz line frequency) that usually are generated off the board. Noise generated on the board by the active devices have harmonics in the range of 100 MHz and higher. A bypass capacitor is placed across each chip and generally is much smaller (≈ 0.1 µF) than the capacitor across the board.

Since the goal is to filter out any AC component on the power supply, it might seem initially that the largest possible capacitor is the best, minimizing the impedance as much as possible. However, this does not take into account that real capacitors do not have ideal characteristics.

A capacitor, which is ideally represented in Figure 3a, is more realistically represented by Figure 3b. Resistance and inductance are the result of the construction of the plates and the leads necessary to build the capacitor. Because the parasitic components are effectively in series with the capacitance, they are called equivalent-series resistance (ESR) and equivalent-series inductance (ESL).

Thus the capacitor is a series resonant circuit for which

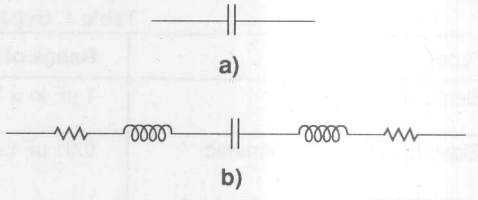
$$f_R = \frac{1}{\sqrt{LC}}$$

As shown in Figure 4a, it is capacitive at frequencies below f_R, and inductive at frequencies above f_R. As as result, the capacitor is more a band-reject filter than a high-frequency-reject filter.

As an example, the 10 µF capacitors used for the board-power connections are typically made with rolls of metal foils separated by an insulating material (Figure 5). This results in large ESLs and ESRs. Because of the large ESLs, f_R is generally less than 1 MHz. They are good filters for 60-Hz noise, but not good for the expected 100-MHz and higher switching noise.

The ESL and ESR result from the construction of the capacitor and dielectric material used, rather than from capacitance value. The high-frequency reject capabilities cannot be improved by replacing a capacitor with a larger one of the same type. The impedance of a large capacitor is smaller than that of a small capacitor at frequencies below the f_R of the small capacitor. But at frequencies above f_R, the ESL dominates and there is no difference between the impedance of the two capacitors (Figure 4b). This is because only the capacitance has changed; unless the construction is changed, the ESL remains essentially unchanged. To improve high-frequency filtering, one must replace the capacitor with a type that has a lower ESL.

Various types of capacitors are available for specific frequencies and applications. Table 1 gives a small overview of some available device types.



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Figure 3. a) Ideal Representation of a Capacitor b) Parasitic Components added to Emulate Real Conditions

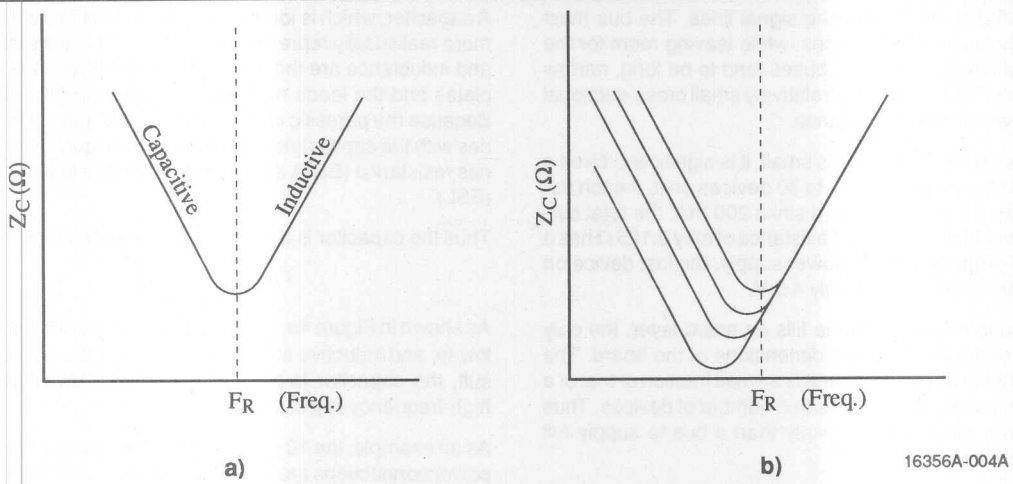


Figure 4. a) Capacitor Impedance Versus Frequency; b) the Effect of Lowering Capacitance While Using the Same Type of Construction (Constant ESL)

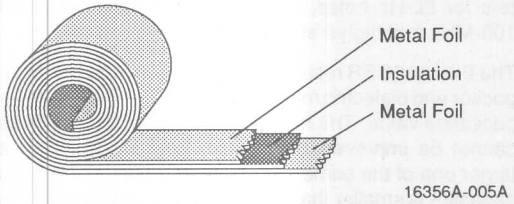


Figure 5. Internal Construction of a Large (> μF) Capacitor

The lowest ESL capacitors often are made with non-ferromagnetic materials, which have a low voltage-capacitance product. Thus it is difficult to make large capacitors with practical breakdown voltages to prevent board failure. However, because of better filtering characteristics, larger values might not be needed. Figure 6 compares a 0.01 μF capacitor of type C0G (non-ferromagnetic) to a 0.1 μF capacitor of another type. Note that the 0.01 μF capacitor gives better filtering at higher frequencies.

The capacitor graphs imply that any one capacitor has a limited effective frequency operating range. Because systems have both high- and low-frequency noise, it is desirable to extend this range. This can be done by putting a high-capacitance, low-ESL device in parallel with a lower-capacitance, very-low-ESL device. Figure 7 shows that this can significantly increase the effective filtering frequency range.

1.1.4 Bypass Capacitor Placement

After the filter capacitors have been chosen, they must be placed on the board. Figure 8a shows the standard placement for boards with slow device speeds. The capacitor is placed near the top of the device to help ensure its accessibility. While simple for layout, this does not give the best high-speed performance.

Note that the V_{CC} capacitor connection is quite close to the chip's V_{CC} connection, but the ground connection is far away. Because noise is not uniform on a power plane, the capacitor is not filtering noise at the chip leads; it is only filtering noise near the chip.

Table 1. Bypass Capacitor Groups

Type	Range of Interest	Application
Electrolytic	1 μF to > 20 μF	Commonly used at power-supply connection on board.
Glass-Encapsulated Ceramic	0.01 μF to 0.1 μF	Used as bypass capacitor at the chip. Also often placed in parallel with electrolytic to widen the filter bandwidth and increase the rejection band.
Ceramic-Chip	0.01 μF to 0.1 μF	Primarily used at the chip. Also useful where low profile is important.
C0G	< 0.1 μF	Bypass for noise-sensitive devices. Often used in parallel with another ceramic chip to increase rejection band.

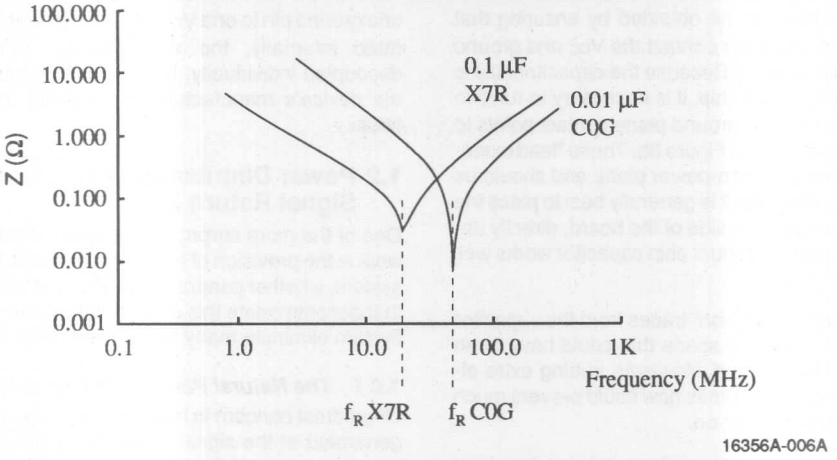


Figure 6. Frequency Response of X7R and C0G Type Construction

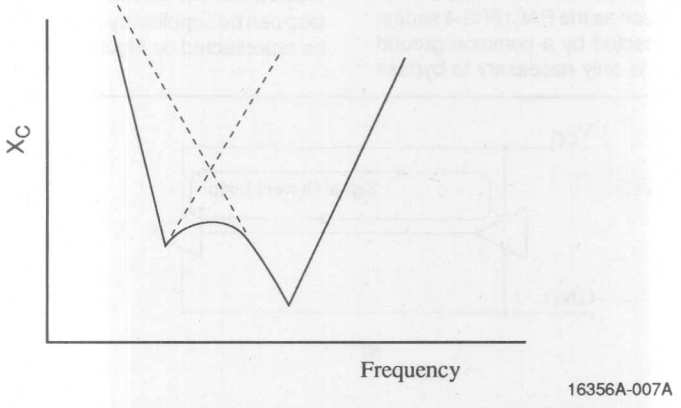


Figure 7. Frequency Response of Two Capacitors in Parallel

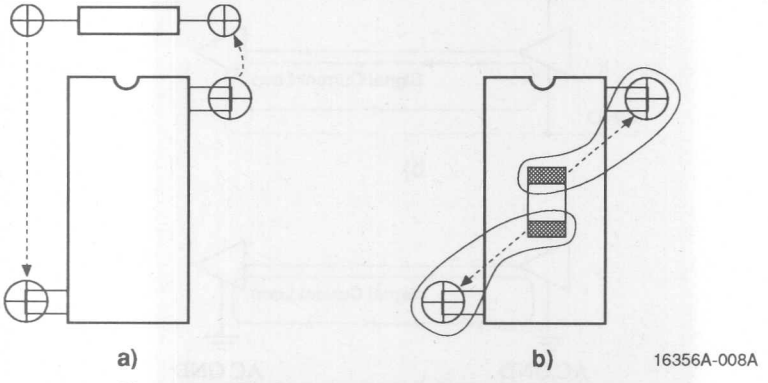


Figure 8. a) Typical Placement of Bypass Capacitors; b) Preferred Placement of Bypass Capacitors

Better performance can be obtained by ensuring that the chip and the capacitor contact the V_{CC} and ground planes at the same point. Because the capacitor size is different from that of the chip, it is necessary to run two traces from the V_{CC} and ground plane contact points to the capacitor, as shown in Figure 8b. These "lead extensions" are placed on a non-power plane and should be kept as short as possible. It is generally best to place the capacitor on the opposite side of the board, directly under the chip. A surface-mount chip capacitor works well here.

Note that the "lead extension" traces from the capacitor to the power pins take up space that could have been used for signal-line routing. However, putting extra effort into routing the signal lines now could prevent much noise-reduction work later on.

For devices with multiple V_{CC} and ground pins, how best to bypass depends on the device. In particular, it depends on whether the power pins are connected internally. On some devices, such as the PAL16R8-4 series, the ground pins are connected by a common ground bus. On these devices, it is only necessary to bypass one ground pin to one V_{CC} pin. If the power is kept separated internally, the separate V_{CC} pins must be decoupled individually. In general, it is best to contact the device's manufacturer for specific recommendations.

1.2 Power Distribution Network as a Signal Return Path

One of the more surprising functions of the power network is the provision of a return path for all signals in the system, whether generated on or off the board. Designs that accommodate this aspect of the power distribution system eliminate many high-speed noise problems.

1.2.1 The Natural Path of the Signal-Return Line

Of greatest concern in high-speed design is the energy generated at the signal switching edges. Each time a signal switches, AC current is generated. Current requires a closed loop. As illustrated schematically in Figures 9a and 9b, the return path needed to complete the loop can be supplied by the ground or V_{CC}. The loop can be represented by Figure 9c.

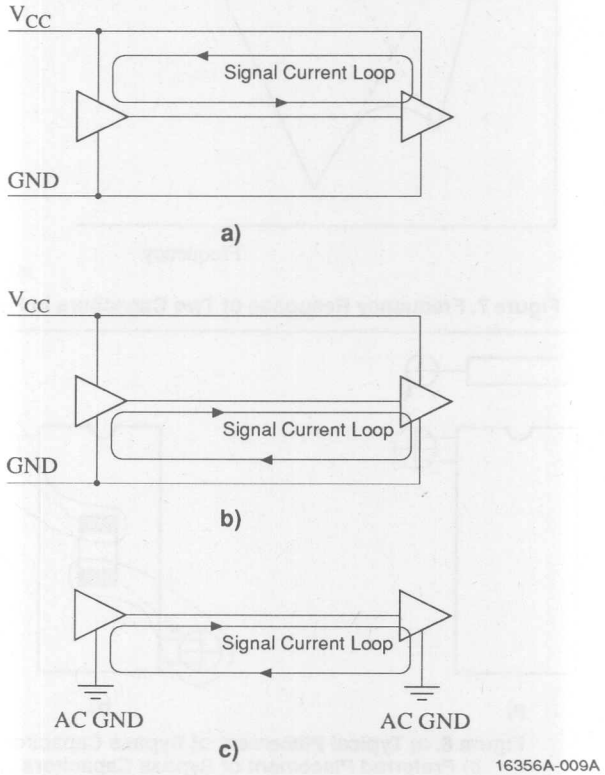
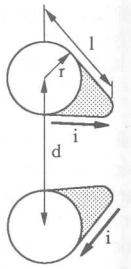


Figure 9. Current Loop of a Signal on the Board.
a) Through V_{CC}; b) Through Ground; c) The Equivalent AC Path



$$L = Kl\,ln\,\frac{d - r}{r}$$

16356A-010A

Figure 10. Inductance Increases as the Signal and Return Path are Separated

Current loops have inductance and can be thought of as single-turn coils. They can aggravate ringing, crosstalk, and radiation. The current-loop inductance and associated problems increase with loop size. Minimizing the size of the loop minimizes these problems.

AC return signals have an entire plane in which to choose a path, but they take the path of least impedance (not necessarily least resistance) to the current. Impedance also includes inductance and capacitance. Metal has very little resistance; therefore, the impedance is primarily inductive. Because impedance increases with inductance, the path of least impedance is the path with the smallest inductance.

If the signal line goes from A to B on a random path, the natural return path is not necessarily a straight line, as would be dictated for least resistance. As noted in Figure 10, the inductance of a signal line and its return line increases with the separation of the two paths. The path of least impedance is the path bringing the signal-return line closest to the signal line. If it can, the signal return follows the signal line as closely as possible, resulting in the smallest loop. In multiple layer boards, "as closely as possible" usually means in a ground or V_{CC} plane above or below the signal trace. In a two-layer board, this means the closest ground or V_{CC} trace.

1.2.2 Bus vs Planes for a Signal Return Path

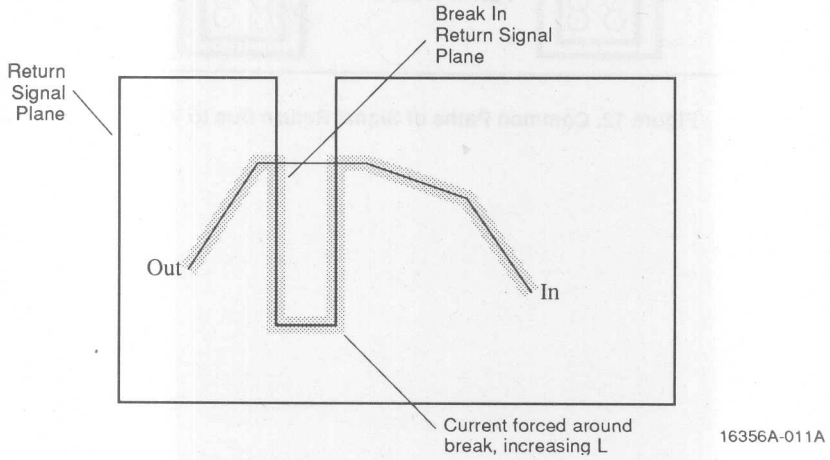
Figure 2a shows that a power bus has a fixed path. The return signal must follow this path, whether optimal or not. Unless the signal lines are purposely laid out near the power buses and oriented to minimize loop size, there will probably be large loops. If the layout of a board using buses for power distribution is not thought out carefully, it can result in a configuration that generates much noise.

The power plane imposes no natural restrictions on current flow. Thus the return signal can follow the path of least impedance, which is the path closest to the signal line. This results in the smallest possible current loops, which makes it the preferred solution for high-speed systems.

Although power planes have an advantage over buses, the benefits they provide can be defeated by the designer. Any break in the natural path of the return signal forces it to go around the break, increasing the loop size (Figure 11). Be careful about cuts in the ground and power planes.

1.3 Layout Rules With Power Distribution Considerations

The following layout rules will help you take advantage of power planes and avoid pitfalls.



16356A-011A

Figure 11. The Increase in Loop Size Due to a Break in the Power Plane

a. Be Careful with Feedthroughs

Cuts in the power plane tend to show up at feedthroughs or vias. These are necessary for traces to cross sides of the board and to connect components and connectors to the board. They are surrounded by small gaps where the power planes are etched away to avoid shorts in the signal lines. If the vias are close and the etchings wide, they might touch and form a barrier to any return path. This can occur with backplane connectors and device sockets.

For example, this can occur on the connectors on VME backplanes. The 104-pin connector has vias that can block the signal return. All the return signals are forced to the edge of the board. Not only are the loops longer, but the edge is shared by all the return signals; as we will see, this can result in crosstalk (Figure 12).

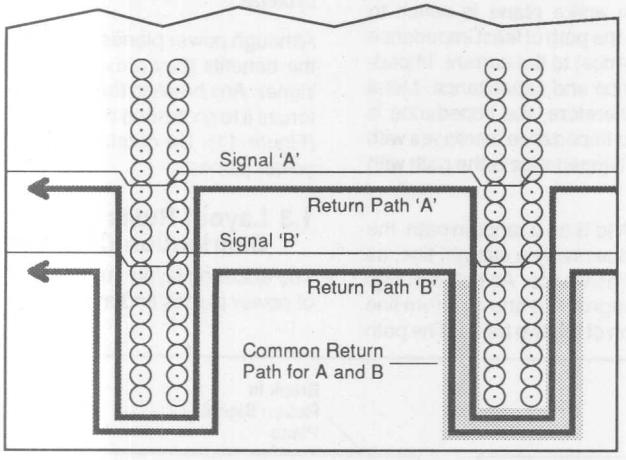
b. Ground Cables Sufficiently

Current loop considerations are also applicable for cables going off the board. Every signal should be a two-wire pair: one for the signal, and one for the return. The two lines should be kept next to each other to minimize the loop size. Figures 13a and 13b illustrate poorer configurations. Figure 13c illustrates the proper configuration.

c. Separate Analog and Digital Power Planes

High-speed analog devices tend to be sensitive to digital noise. For example, amplifiers can amplify switching noise, making it appear as spikes. Thus on boards with analog and digital functions, the power planes are commonly separated; the planes are tied together at the power source. This causes a problem for devices using both types of signals (such as DACs or voltage comparators). The signal lines must cross the plane boundaries. These boundaries force the return path to the power source before returning to the driver.

The solution is to place jumpers across the ground planes where signals cross (Figure 14). The jumper provides a bridge across the break for the return signal; this helps minimize the current loop.



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Figure 12. Common Paths of Signal Return Due to Vias

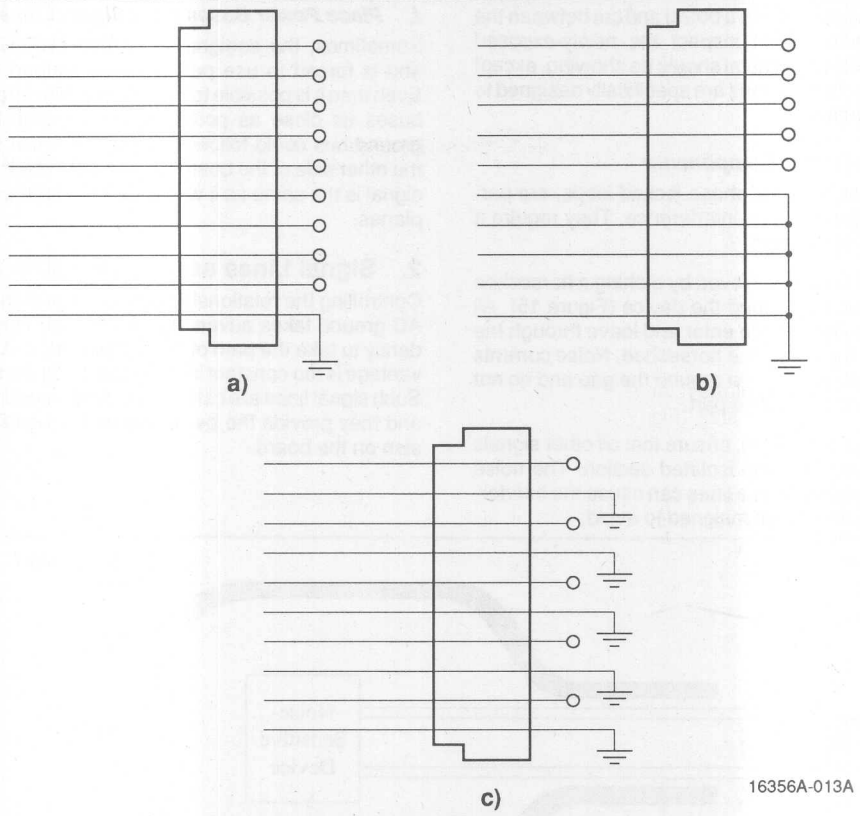


Figure 13. Connector Configuration. a) Insufficient Grounds; b) Enough Grounds but Grounds lumped Together Resulting in Larger Current Loops; c) Grounds Evenly Distributed Among Signal Lines

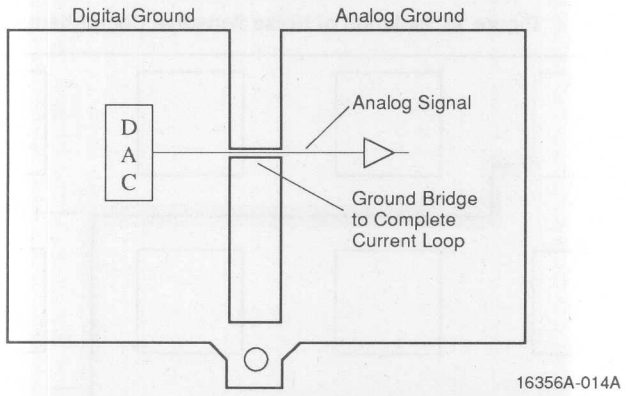


Figure 14. Jumper Between Analog- and Digital-Power Planes for Signal-Return Path

d. Avoid Overlapping Separated Planes

When separate power-planes are used, do not overlap the power plane of the digital circuitry and the power plane of the analog circuitry. The analog and digital power planes are separated to isolate the currents from each other. If the planes overlap, there is capacitive coupling, which defeats isolation.

To ensure separation, take a board and cut between the separated planes. Then inspect the newly-exposed edges of the board. No metal should be showing, except where traces or connections are specifically designed to cross the boundary.

e. Isolate Sensitive Components

Certain devices, such as phase-locked loops, are particularly sensitive to noise interference. They require a higher degree of isolation.

Good isolation can be achieved by etching a horseshoe in the power planes around the device (Figure 15). All signals used by the device enter and leave through the narrow gap at the end of the horseshoe. Noise currents on the power plane must go around the gap and do not come close to the sensitive part.

When using this technique, ensure that all other signals are routed away from the isolated section. The noise signals generated by these lines can cause the interference this technique was designed to avoid.

f. Place Power Buses Near Signal Lines

Sometimes, the designer must use two-layer boards and is forced to use power buses instead of planes. Even then it is possible to control loop size by placing the buses as close as possible to the signal lines. The ground bus could follow the most sensitive signals on the other side of the board (Figure 16). The loop for that signal is the same as it would be if the load used power planes.

2. Signal Lines as Transmission Lines

Controlling the relationship between the signal line and AC ground takes advantage of the return signal's tendency to take the path of least impedance. Another advantage is the constant impedance along the signal line. Such signal lines are called controlled-impedance lines, and they provide the best medium for signal transmission on the board.

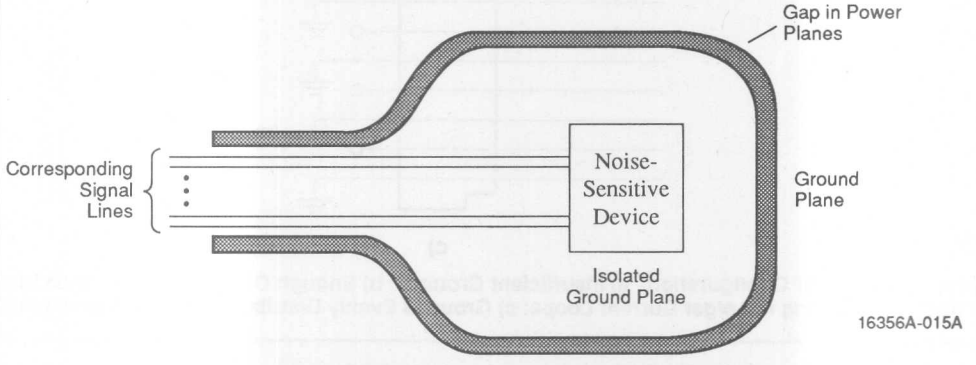


Figure 15. Isolation of Noise Sensitive Components

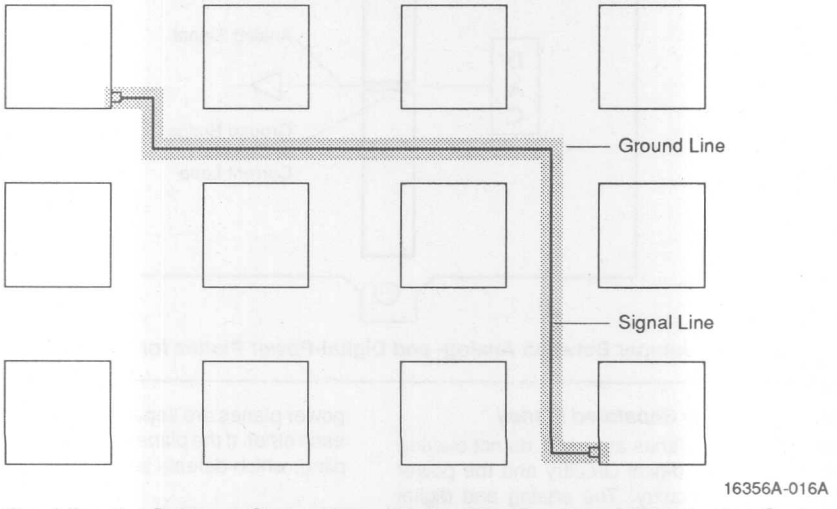


Figure 16. Providing the Optimum Signal-Return Path with a Bus-Power Distribution System

However, when the signal delay is greater than a significant portion of the transition time, the signal line must be treated as a transmission line. An improperly terminated transmission line is subject to reflections, which distort the signal. The signal at the load end of the line can resemble ringing (Figure 17), slowing down the system. It can also cause false clocking, destroying system functionality.

A controlled-impedance signal line can be modeled as shown in Figure 18. Inductance and capacitance are evenly distributed along the length of the line. Their units are henrys per unit length and farads per unit length, respectively.

From the model, we can derive two important parameters: impedance (Z_0), and propagation delay (t_{PD}). On a lossless signal line, Z_0 is an AC resistance; i.e., Z_0 appears to the driver as a pure resistor. Its units are ohms (Ω), and it is equal to

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

where

L_0 = Signal Line Inductance in henrys per unit length

C_0 = Signal Line Capacitance in farads per unit length

The propagation delay also depends on L_0 and C_0. It has units of time per unit length, and it is equal to

$$t_{PD} = \sqrt{L_0 C_0}$$

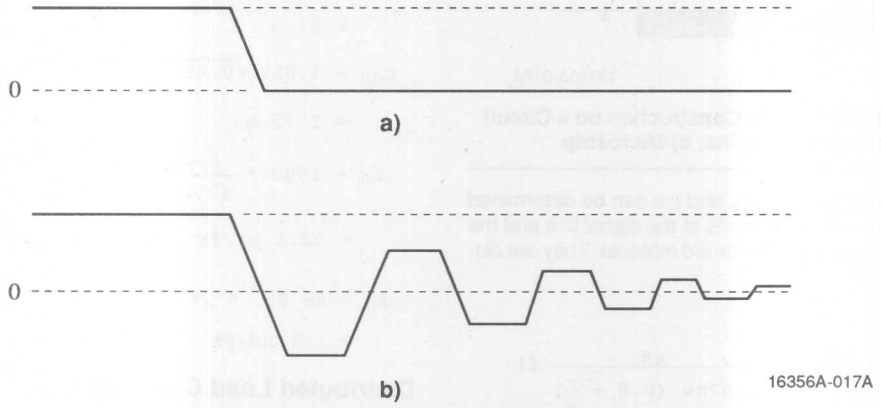


Figure 17. Reflections on a Signal Line. a) at the Driver; b) at the Load

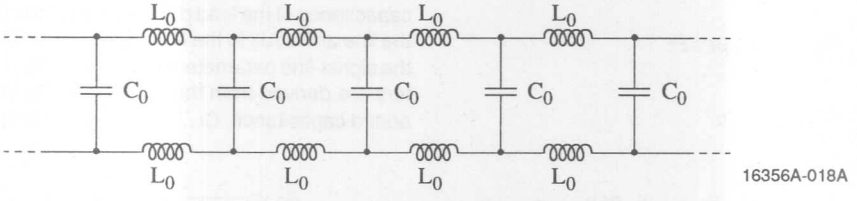


Figure 18. Transmission Line

Transmission Line Categories

Given that the designs discussed in this paper are for printed circuit boards, the possible types of signal lines fall into one of two categories: stripline and microstrip (Figure 19). The stripline has the signal line sandwiched between two power planes. This technique theoretically offers the cleanest signals because the signal line is shielded on both sides. However, the lines are hidden; there is no easy access to the signal lines. Microstrip has the signal line on an outer layer. The ground plane is to one side of the signal line. This technique allows easy access to the signal line.

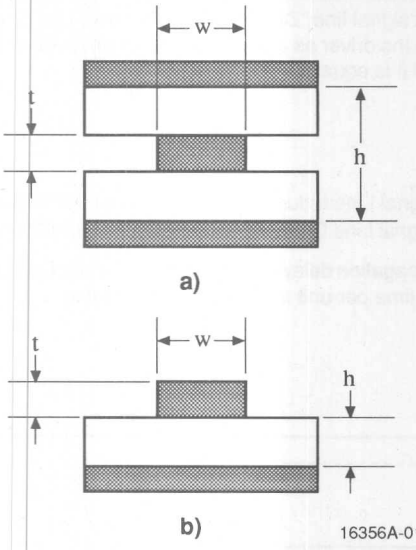


Figure 19. Signal Line Construction on a Circuit Board. a) Stripline; b) Microstrip

The parameters C_0, L_0, Z_0, and t_{PD} can be determined from the physical dimensions of the signal line and the dielectric properties of the board material. They are discussed below.

For Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_R}} \ln \frac{4h}{0.67\pi w\ (0.8 + \frac{t}{w})}\ \Omega$$

$$t_{PD} = 1.017\sqrt{\varepsilon_R}\ ns/ft$$

$$C_0 = 1000\ \frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

For Microstrip

$$Z_0 = \frac{87}{\sqrt{\varepsilon_R + 1.41}} \ln \frac{5.98h}{0.8w + t}\ \Omega$$

$$t_{PD} = 1.017\ \sqrt{0.457\varepsilon_R + 0.67}\ ns/ft$$

$$C_0 = 1000\ \frac{t_{PD}}{Z_0}\ pF/ft$$

$$L_0 = Z_0^2 C_0\ pH/ft$$

e_R is the relative dielectric constant of the board material. A common material is epoxy-laminated fiberglass, which has an average e_R of 5.

Example

The dimensions of the trace and board are restricted by certain rules. Generally, the vendor sells the board with 1 oz of copper, so the metal thickness is about 1 mil. The trace width should be between 8 and 15 mils. Signal lines thinner than 8 mils tend to be harder to control. Signal lines thicker than 15 mils tend to have excess capacitance. A typical value is 10 mils. The layer separation is determined by the required board thickness and the number of layers to be used. For this example, 30 mils is adequate.

Based on these assumptions, it is possible to calculate the parameters for a typical signal line: width = 10 mils, thickness = 1 mil, separation = 30 mils, and $e_R = 5$.

$$Z_0 = \frac{87}{\sqrt{5} + 1.41} \ln \frac{5.98 * .03}{0.8 * .001 + .01}\ \Omega$$

$$= 67.0$$

$$t_{PD} = 1.017\ \sqrt{0.456 * 5 + 0.67}\ ns/ft$$

$$= 1.75\ n$$

$$C_0 = 1000 * \frac{1.75}{67.05}\ pF/ft$$

$$= 26.1\ pF/ft$$

$$L_0 = 67.05^2 * 26.1\ pH/ft$$

$$= 117\ nH/ft$$

Distributed Load Calculations

The calculations above are for a signal line with a lumped load at the end of the trace (Figure 20). If the load is distributed along the signal line (Figure 21), the capacitance of the load devices is also distributed along the line and adds to the line capacitance. This changes the signal-line parameters Z_0 and t_{PD}. The new parameters are derived from the original values based on the added capacitance, C_L, in farads per unit length:

$$Z_0 = \frac{Z_0}{\sqrt{1 + \frac{C_L}{C_0}}}\ \Omega$$

$$t_{PD} = t_{PD} * \sqrt{1 + \frac{C_L}{C_0}}\ ns/ft$$

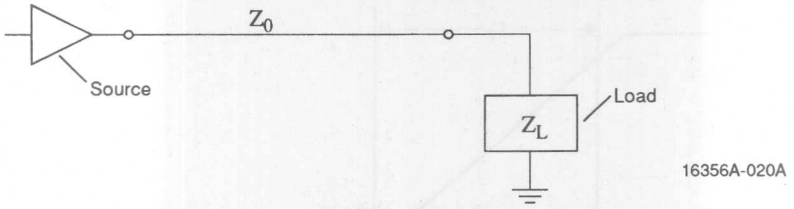


Figure 20. Transmission Line with a Lumped Load

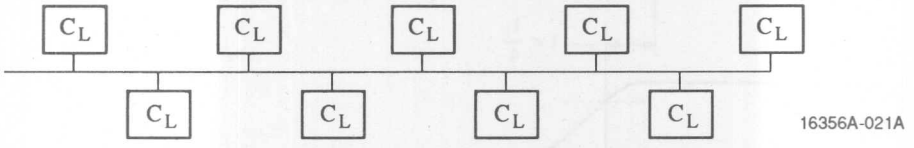


Figure 21. Transmission Line with a Distributed Load

Distributed loading is common in memory banks. The input capacitance on these devices can range from 4 pF to 12 pF. The following example uses 5 pF. The physical size of memory devices usually permits placing two of them per inch. The distributed added capacitance is then:

$$C_L = \frac{5\ pF}{0.5\ in * \frac{1\ ft}{12\ in}}$$

$$= 120\ pF/ft$$

The new values of Z_0 and t_{PD}, based on distributed loading, are:

$$Z_0 = \frac{67.05\ \Omega}{\sqrt{1 + \frac{120\ pF/ft}{26.1\ pF/ft}}}$$

$$= 28.34\ \Omega$$

$$t_{PD} = 1.75\ ns/ft * \sqrt{1 + \frac{120\ pF/ft}{26.1\ pF/ft}}$$

$$= 4.14\ ns/ft$$

With this distributed load, the impedance has been greatly reduced, and the signal is now much slower.

Reflections

The source generates a signal with an energy content determined by $Z_0\ \Omega$. Even though the line is seen as a resistance, the signal line does not dissipate energy. The energy in the signal must be dissipated by the load impedance (Z_L), as shown in Figure 20.

The maximum transfer of energy from source to load requires that the load impedance equal the source impedance. For the entire signal to be transferred to Z_L, Z_L must equal Z_0. If they are not equal, some of the signal energy is dissipated, and the rest is reflected back toward the source. The source generator output then adjusts to compensate for the "new" load.

The waveform of the signal at the load can be thought of as the sum of the originally generated signal and the reflection from the load. The appearance of the waveform depends on the mismatch of the load and line impedances and the ratio of the signal-transition time (t_R) to the propagation delay of the line (τ), t_R/τ. If the transition time is significantly longer than the propagation delay of the line, the reflection reaches the source when the original signal has changed only a small amount. The generator compensates for the "new" load and transmits the corrected signal with little signal disturbance. The signal at the load then has a small overshoot.

If the propagation delay of the line is long enough for the reflection to reach the source after the signal has changed a significant percentage, the generator must change significantly to compensate for the load. The load reflects the new transition, which results in the ringing shown in Figure 17.

The amount of overshoot usually varies proportionally with the signal-line length until the signal-line delay is equal to the transition time. At this point, the overshoot can be as much as the original transition, effectively doubling the swing of the transition.

A signal line long enough to produce significant reflections acts like a transmission line. The point at which the signal line is considered a transmission line depends on the amount of tolerable distortion. A liberal rule of thumb is to consider a signal line a transmission line when the transition time of the original signal is less than four times the propagation delay of the signal (Figure 22); that is, when $t_R/\tau \geq 4$.

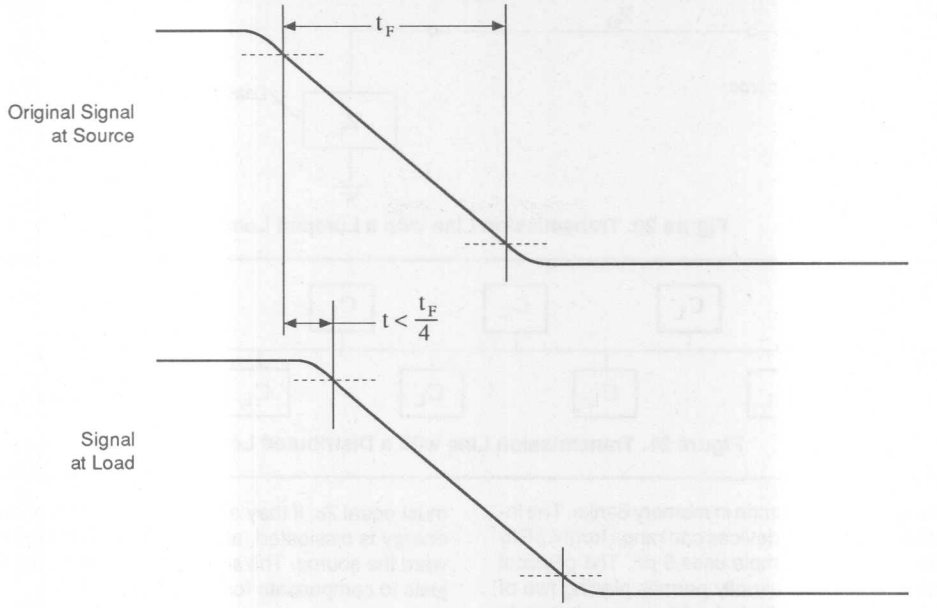


Figure 22. Minimum Delay Between Original and Reflected Signal Which Results in a Transmission LIne

A more conservative rule is to consider the signal line a transmission line when t_R/τ is less than eight times the propagation delay. Generally, the larger the transition time is in relation to the propagation delay of the signal line, the cleaner the resultant signal.

From this it is possible to determine what length of the microstrip line discussed above must be treated as a transmission line. On available devices, t_R ranges from 5 ns (especially those using bipolar technology) to 1 ns (newer bipolar and CMOS devices). The rise times and corresponding signal-line lengths are shown in Table 2 for the example given above.

Table 2
Example: t_R and Corresponding Transmission-Line Length for $\frac{t_R}{\tau} = 4$

t_R (ns)	Line Length (inch)
5	8.6
4	6.9
3	5.1
2	3.4
1	1.7

For older devices with 5 ns transition times, signal lines shorter than 8.6" do not have to be treated as transmission lines. For newer, high-speed devices, even a two-inch line is a transmission line. Practically all signal lines are transmission lines on boards with high-speed devices.

If the transmission line has the distributed load in the example above, then the minimum transmission-line length must be reconsidered. As shown in Table 3, a four-inch line is a transmission line when t_R = 5 ns. If t_R = 1 ns, a signal line smaller than one inch is a transmission line.

Table 3
Example: t_R and Corresponding Transmission-Line Length with Lumped and Distributed Loads for $\frac{t_R}{\tau} = 4$

	Line Length (inch)	
t_R (ns)	Lumped Load	Distributed Load
5	8.6	3.6
3	5.1	2.17
2	3.4	1.4
1	1.7	0.75

Quantifying Reflections

Given that the signal line is long enough to be considered a transmission line, the size of the reflected signal depends on the difference between Z_0 and Z_L. The numerical indicator of the percentage, or the original signal that is reflected, is called the reflection coefficient (K_R). K_R is equal to:

$$K_R = \frac{Z_L - Z_0}{Z_L + Z_0}$$

The percentage of the original signal reflected back is 100 * K_R.

Referring back to the open load:

$$K_R = \frac{\infty - Z_0}{\infty + Z_0}$$

$$= 1$$

For an shorted load:

$$K_R = \frac{0 - Z_0}{0 + Z_0}$$

$$= -1$$

For open and shorted loads, the entire signal is reflected without attenuation. K_R is negative for the shorted load. This indicates that the reflected signal is inverted from the original.

With a printed-circuit board, it is possible to estimate the expected type of mismatch. Z_0 typically ranges from 30 Ω to 150 Ω. Input impedances range from 10 kΩ (for bipolar devices) to over 100 kΩ (for CMOS devices). Output impedances can be very low. A CMOS PAL device, such as the PALCE16V8, has a typical-output LOW voltage of 0.2 V at 24 mA for about 8 Ω. The output-HIGH impedance is about 50 Ω, which is closer to the expected Z_0.

Consider the microstrip line derived earlier, with a CMOS device as its load. The following discussion shows what happens on the HIGH to LOW transition.

The driver's output impedance (Z_S) is:

$$Z_S \approx \frac{V_{OL}}{I_{OL}}$$

$$= \frac{0.2\ V}{24\ mA} \approx 8.3\ \Omega$$

A more accurate number can be obtained from an actual I/V curve of the output.

The input impedance of the load is greater than 100 kΩ. This is so much greater than Z_0 (67 Ω), that K_R at the load is practically equal to one. K_R at the source is:

$$K_R = \frac{8.3 - 67}{8.3 + 67}$$

$$= -0.78$$

The driver generates a signal switching from 3.5 V to 0.2 V. Since the driver-output impedance and Z0 make up a voltage divider, the generated signal is:

$$\Delta V = \frac{(0.2\ V - 3.5\ V)\ Z_0}{Z_0 + Z_S}$$

$$= \frac{(0.2\ V - 3.5\ V)\ 50}{50 + 8}$$

$$= 2.84\ V$$

The resultant signal at the source is:

$$V_S = 3.5\ V - \Delta V = 3.5\ V - 2.84\ V$$

$$= .066\ V$$

When the signal reaches the load, V_L changes by –2.84 V from the original transmission and a further –2.84 V from the reflection. Since V_L originally was 3.5 V, it is now –2.19 V.

At the start, V_S = 0.66 V. The reflected signal returns to the source. Some of it is reflected per the source KR. VS is equal to the sum of the original signal, the reflected signal, and the second reflected signal. The second reflection is equal to:

$$V_R = -.78 * -2.84$$

$$= 2.21\ V$$

$$V_S = 0.66\ V + -2.84\ V + 2.21\ V$$

$$= -0.035\ V$$

The second reflection goes to the load. When it arrives,

$$V_L = -2.19 + 2.21 + 2.21$$

$$= 2.24$$

The signal continues like this, bouncing back and forth, getting smaller each time. This is illustrated in the lattice diagram in Figure 23. The lines at the left and right are the voltage at the source and load, respectively. The angled lines show the value of the transmitted signal and the reflections.

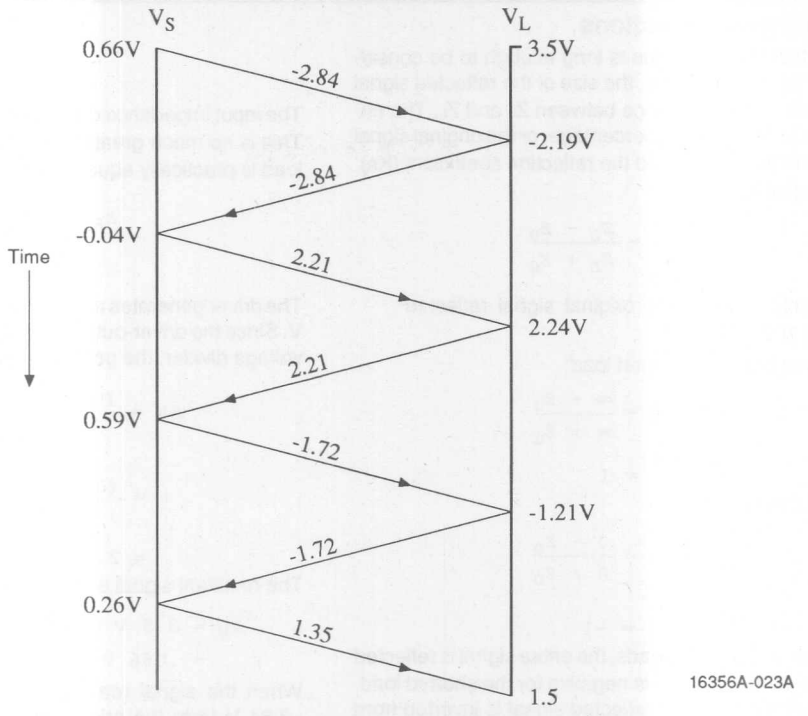


Figure 23. Lattice Diagram Representation of a Reflected Signal

The same information in the time domain is shown in Figure 24. The top part of the Figure shows the source; the bottom shows the load signal. Note that it takes five complete cycles for the signal strength to drop below the input threshold. Propagation delays are typically from 2 ns/ft to 5 ns/ft. With t_{PD} = 3 ns/ft and a 6-inch line, the delay across the line is about 1.5 ns. The signal can be safely considered valid at about 13.5 ns after the original transition.

TERMINATION

The amount of reflections shown in the last example would be too much for most systems. A technique is needed to eliminated, or at least reduce, the reflections. Since the reflections are eliminated when $Z_L = Z_0$, it is necessary to change Z_L to equal Z_0.

To understand this, look at the nature of the input and output impedances of the PAL devices. As noted above, input impedances tend to be high. Bipolar is in the 10 kΩ range, while CMOS is in the 100 kΩ range. Output drivers tend to have low impedance.

There are two schemes for termination: reduce Z_L to Z_0 to eliminate load reflections, or increase Z_S to Z_0 to eliminate secondary reflections at the source. Z_L can be reduced by placing a resistor in parallel with the load—parallel termination; Z_S can be increased by placing a resistor in series with the source and the line—series termination.

Parallel termination is shown in Figure 25a. Because of the extremely high input resistance of most devices, R_L can be made equal to Z_0.

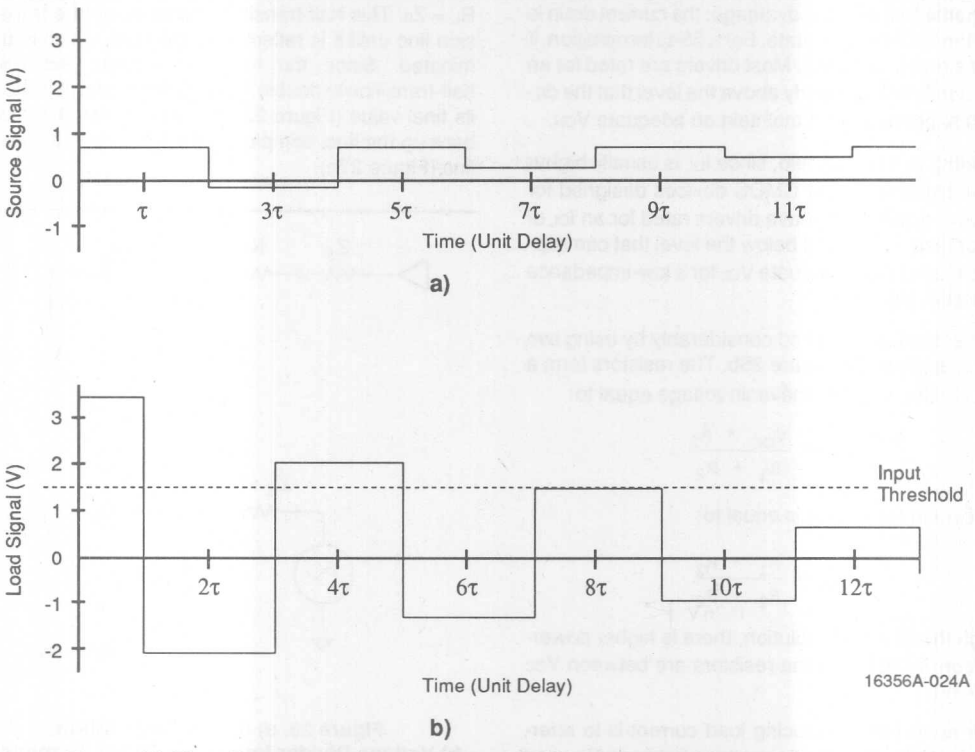


Figure 24. Time Representation of a Reflected Signal; a) at the Source b) at the Load

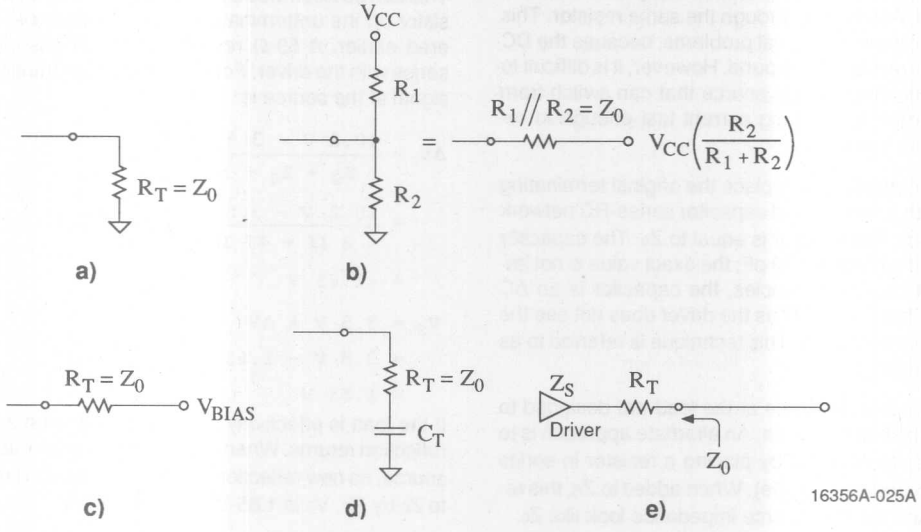


Figure 25. a) Parallel Termination; b) Thévenin Equivalent; c) Active Termination; d) Series Capacitor; e) Series Termination

This scheme has one disadvantage: the current drain is high for the HIGH-output state. For a 50-Ω termination, it can be as much as 48 mA. Most drivers are rated for an I_{OH} of 3.2 mA. This is clearly above the level that the device can support and still maintain an adequate V_{OH}.

Terminating to V_{CC} can help, since I_{OL} is usually higher than I_{OH}. However, most CMOS devices designed for board-level applications have drivers rated for an I_{OL} of 24 mA or less. This is still below the level that can support and maintain an adequate V_{OL} for a low-impedance transmission line.

The current can be reduced considerably by using two resisters, as shown in Figure 25b. The resistors form a voltage divider with the Thévenin voltage equal to:

$$V_{TH} = \frac{V_{CC} * R_2}{R_1 + R_2}$$

The Thévenin resistance is equal to:

$$R_{TH} = \frac{R_1 * R_2}{R_1 + R_2}$$

Although this is a good solution, there is higher power-supply current because the resistors are between V_{CC} and ground.

Another approach to reducing load current is to reference the resistor to a positive voltage between V_{OH} and V_{OL} (Figure 25c). The current flow from 3 V to 2.5 V through a 50-Ω resistor is considerably less than the flow from 3 V to ground through the same resistor. This does not present any signal problems, because the DC voltage reference is AC ground. However, it is difficult to find a terminating voltage source that can switch from sinking current to sourcing current fast enough to respond to the transitions.

Another technique is to replace the original terminating resistor with a resistor and capacitor series-RC network (Figure 25d). The resistor is equal to Z_0. The capacitor can be on the order of 100 pF; the exact value is not important. At these frequencies, the capacitor is an AC short but it blocks DC. Thus the driver does not see the DC loading effect of R_L. This technique is referred to as AC termination.

Techniques that terminate at the load are designed to eliminate the first reflection. An alternate approach is to increase Z_S to equal Z_0 by placing a resistor in series with the source (Figure 25e). When added to Z_S, this resistor makes the new source impedance look like Z_0.

This type of termination works best with a lumped load because the voltage divider formed by the Z_S and Z_0 attenuates the signal (Figure 26 a and b). The original transition is cut in half by this voltage divider, since $Z_S + R_L = Z_0$. This half-transition tracks down the transmission line until it is reflected at the load, which is unterminated. Since the reflection causes the original half-transition to double, it brings the signal at the load to its final value (Figure 27a). The reflection then travels back up the line, completing the transition all along the line (Figure 27b).

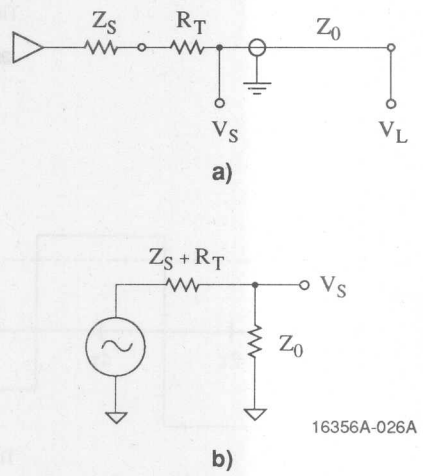


Figure 26. a) Series Termination; b) Voltage Divider formed by Series Termination

This can be illustrated by putting a series terminating resistor on the unterminated microstrip example considered earlier. A 59-Ω resistor (68Ω - 9Ω) is placed in series with the driver. For a LOW to HIGH transition, the signal at the source is:

$$\Delta V = \frac{(0.2\ V - 3.5\ V)\ Z_0}{Z_S + Z_0 + 59\ \Omega}$$

$$= \frac{(0.2\ V - 3.5\ V) * 67\ \Omega}{8\ \Omega + 67\ \Omega + 59\ \Omega}$$

$$= -1.65\ V$$

$$V_S = 3.5\ V + \Delta V$$

$$= 3.5\ V - 1.65\ V$$

$$= 1.85\ V$$

If the load is effectively an open circuit, then a -1.65 V reflection returns. When the reflected signal reaches the source, no new reflections occur because Z_S is matched to Z_0 by R_T. V_S is 1.85 V - 1.65 V = 0.2 V.

The reflection at the load causes V_L to equal 0.2 V when the original signal arrives. V_S does not equal 0.2 V until the reflected signal returns, in this example, 3 ns later (Figure 27).

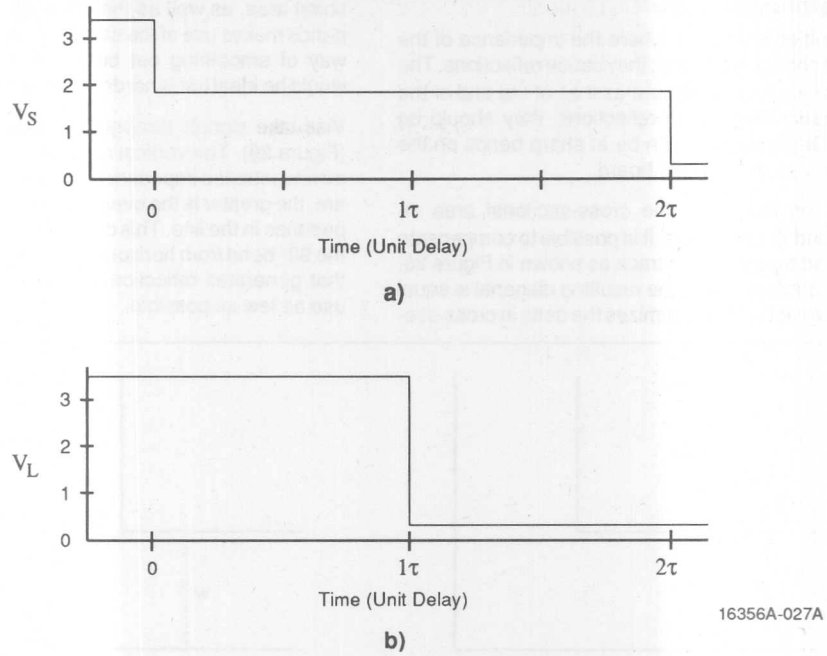


Figure 27. a) Signal at Source; b) Signal at Load end

This can be a risky approach if the load is distributed along the line, since those loads not at the end of the line will see some intermediate voltage until the reflection cleans them up on its return to the source. In addition, this technique adds the delay of the return trip because the signal cannot be considered valid until the device closest to the driver has a valid input. The input to the device closest to the driver becomes valid upon the return of the reflection. The delay is longer than indicated in the last example because the added capacitance of the distributed load reduces Z_0 and increases t_{PD}.

Despite this drawback, series termination is successfully used with DRAM drivers, even when the DRAMs are distributed along the signal line. The risk of the signal spending time near threshold and the extra delay are reduced by choosing R_T so that the resultant Z_S is slightly less than Z_0. The voltage swing at the line is larger, and the voltage level is closer to V_{OL}, below the input threshold. If the line is terminated with 20 Ω, Vs becomes:

$$V_S = 3.5\ V + \frac{(0.2\ V - 3.5\ V)\ Z_0}{Z_S + Z_0 + 20\ \Omega}$$

$$= 3.5\ V + \frac{(0.2\ V - 3.5\ V) * 67\ \Omega}{8\ \Omega + 67\ \Omega + 20\ \Omega}$$

$$= 1.17\ V$$

Because the termination is not an exact match, some ringing occurs. However, if the ringing is below a tolerable level, it can be used successfully. The designer must decide on the compromise. Furthermore, the high capacitance of memory lines often swamps out the ringing.

Often, an exact match is not possible because of the differences between the HIGH- and LOW-output impedances. The output impedance of TTL-compatible devices is different for HIGH and LOW levels. For example, the PALCE16V8 is 8 Ω when LOW, and about 50 Ω when HIGH. This complicates the choice of a terminating resistor because no single value is ideal for both cases. A compromise value must be chosen that results in acceptable results in both transition directions.

Layout Rules for Transmission Lines

The controlled impedance signal line is the best practical medium for signal transfer on a board, and proper termination helps ensure proper noise-free operation. However, it is still possible to generate noise with an inefficient layout. The following layout rules further enhance board operation.

1. *Avoid Discontinuities*

Discontinuities are points where the impedance of the signal line changes abruptly; they cause reflections. The formula for K_R is as valid here as it as at the end of the line. Because they cause reflections, they should be avoided. Discontinuities can be at sharp bends on the trace or at vias through the board.

At bends on the trace, the cross-sectional area increases, and Z_0 decreases. It is possible to compensate for the bend by cutting the trace as shown in Figure 28. The cut is chosen so that the resulting diagonal is equal to the trace width. This minimizes the delta in cross-sectional area, as well as the discontinuity. Using two 45° bends makes use of the same concept and is a common way of smoothing out bends. A smooth circular arc would be ideal but is harder to generate with many tools.

Vias take signals through the board to the other side (Figure 29). The vertical run of metal between layers is an uncontrolled impedance, and the more of these there are, the greater is the overall amount of uncontrolled impedance in the line. This contributes to reflections. Also, the 90° bend from horizontal to vertical is a discontinuity that generates reflections. If vias cannot be avoided, use as few as possible.

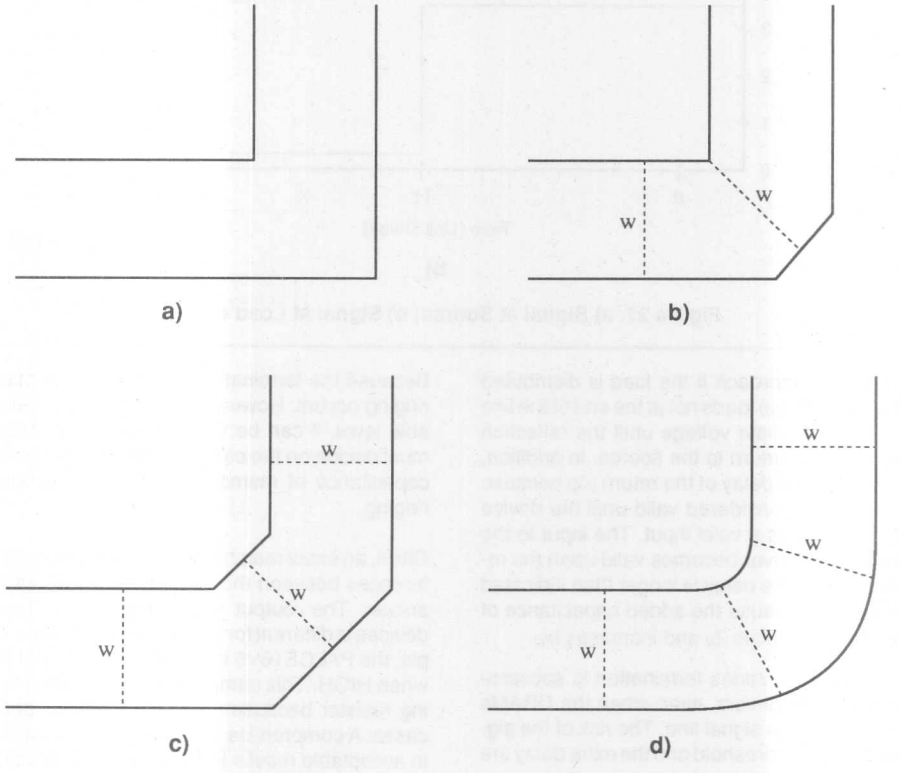


Figure 28. Reducing Discontinuity. a) Corner on PC Board Trace which Causes Discontinuity; Solved: b) by Shaving the Edge; c) by 45° Corner; d) by Using Curves

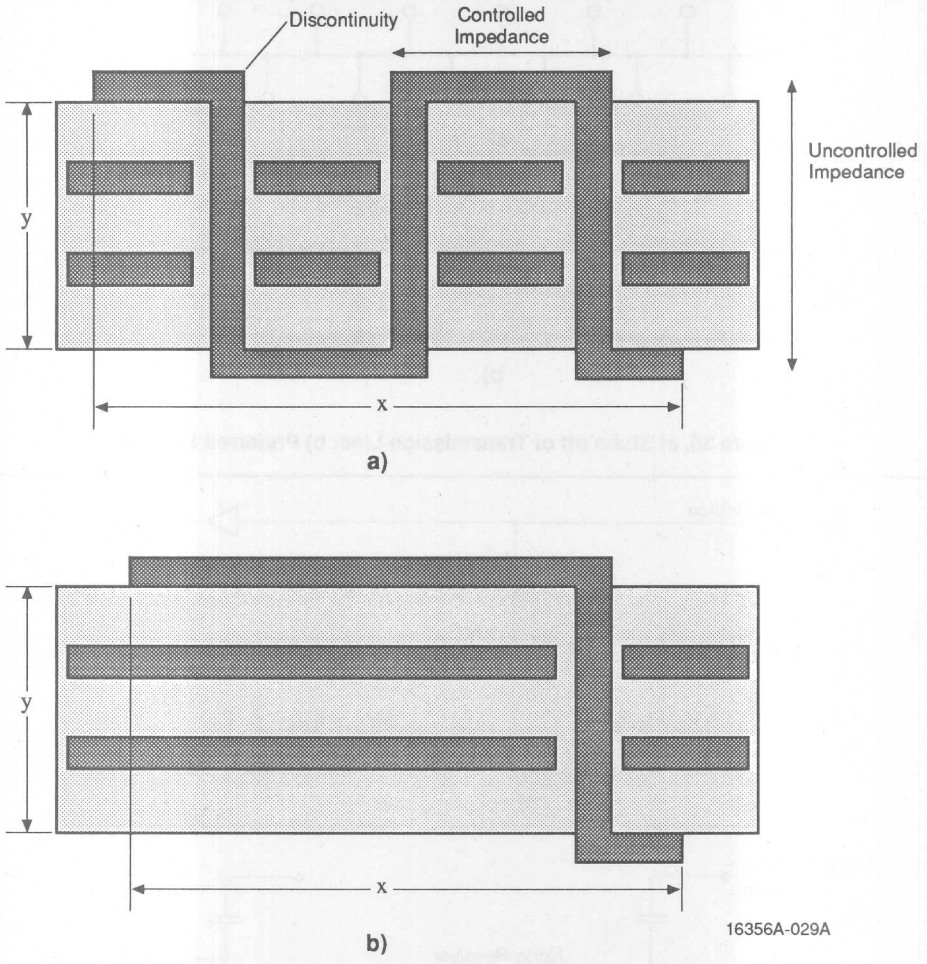


Figure 29. a) Excessive Number of Vias; b) Preferred Solution

Note that changing from an outer layer to an inside layer (or vice versa) generates an impedance change, since the design effectively is changed from stripline to microstrip (or vice versa). While it is theoretically possible to change geometries to compensate and keep impedances the same, it is very difficult to do so in production. The best results are obtained if outside signals remain outside, and inside signals remain inside.

2. Do Not Use Stubs or Ts

When laying out the signal lines, it is often convenient to run stubs or Ts to the devices, similar to Figure 30a. Stubs and Ts can be noise sources. If long enough, they are transmission lines with the main line as the source and are subject to the same type of reflections.

The signal lines should avoid long stubs and Ts. As long as the stubs are very short, a single line can be used with a single termination at the end, although Z_0 must then be derated to account for the distributed load. Given the example in Figure 30a, if the stubs are too long, the signal line could be made into two signal lines, as shown in Figure 30b. Both are transmission lines and require terminating; however, this is preferable to terminating each long stub individually.

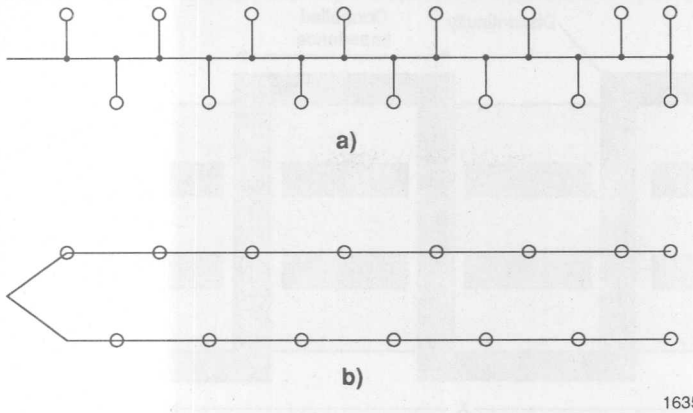


Figure 30. a) Stubs off of Transmission Line; b) Preferred Solution

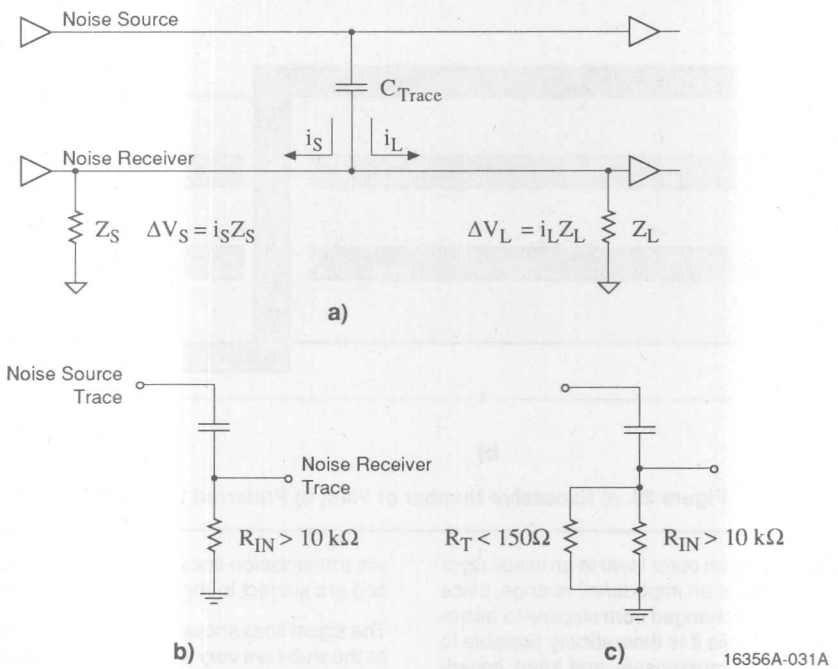


Figure 31. a) Capacitive Crosstalk; b) Equivalent Circuit; c) Solution

3. Crosstalk

Crosstalk is the unwanted coupling of signals between traces. It is either capacitive or inductive. Crosstalk can be handled effectively by following a few simple rules.

3.1 Capacitive Crosstalk

Capacitive crosstalk refers to the capacitive coupling of signals between signal lines. It occurs when the lines are close to each other for some distance.

The circuit representation in Figure 31 shows two signal lines, called the noise source and the noise receiver. Because of capacitance between the lines, noise on the source can be coupled onto the receiving line. This occurs in the form of current injected into the receiving line. In a transmission line, the current sees Z_0 in both directions, and propagates both ways, until it can be dissipated across the source and load. The voltage spike this causes on the line is determined by Z_0. When the current

pulse gets to Z_S and Z_L, it dissipates across these resistors with a voltage proportional to the impedance. If there is an impedance mismatch at the source or load, reflections occur. In the case of an unterminated load, the voltage spike across Z_L can be very large. Terminating the load can significantly reduce the voltage noise seen at the input of the next device.

Capacitive crosstalk can also be reduced by separating the traces. The farther apart the signal traces are, the less the capacitance, and the smaller the crosstalk.

Space constraints on the board may put limits on how far apart the signal lines can be placed. An alternate approach is to put a ground trace between adjacent-signal lines, as shown in Figure 32. The signal is now coupled to ground, not to the adjacent-signal line.

Note that the ground trace must be a solid ground. If it is only connected to the ground plane at the trace ends, the trace has a relatively high impedance. For good grounding, the ground trace should be connected to the ground plane with taps separated a quarter wavelength ($\lambda/4$) of the highest frequency component of the signal.

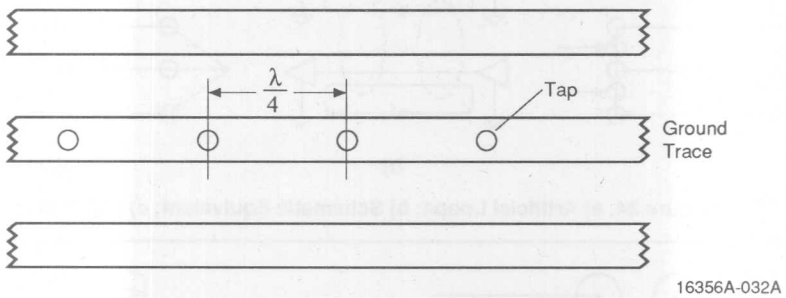


Figure 32. Isolating Traces with a Ground Trace

The wavelength is the distance the signal travels in a single period or:

$$\lambda = vel * Period$$

$$= \frac{1}{t_{PD}} * \frac{1}{freq}$$

With digital signals, the highest significant frequency harmonic of interest is usually assumed to be $1/\pi t_R$. Consider an example where t_R = 1.25 ns (possible for PAL16R8-4 devices). The upper-frequency component is:

$$f_{MAX} = \frac{1}{1.25\ ns * \pi}$$

$$= 255\ MHz$$

The distributed load delay for our example in section 2 was 4.14 ns/ft. λ is equal to the period divided by t_{PD}.

$$\lambda = \frac{1}{255\ MHz} * \frac{1}{4.14\ \frac{ns}{ft}} * \frac{12\ in}{ft}$$

$$= 11.4\ in$$

$$\lambda/4 = \frac{11.4}{4}$$

$$= 2.8\ in$$

For maximum isolation, the ground trace must have taps to the ground plane no more than 2.8 inches apart.

3.2 Inductive Crosstalk

Inductive crosstalk can be thought of as the coupling of signals between the primary and secondary coils of an unwanted transformer (Figure 33). The transformer windings are the current loops on the board (or system). These can be either artificial loops inadvertently created by inefficient layout (Figure 34a) or natural loops resulting from the combination of the signal path and the signal return path (Figure 34b). Artificial loops are sometimes hard to locate, but can be eliminated as shown in Figure 34c.

The amount of unwanted signal coupled to the load depends on the proximity and size of the loops, as well as the impedance of the affected load. The amount of energy transferred increases as the loops become larger and get closer together. The size of the signal seen at the load, on the secondary loop, increases with the load impedance.

3.2.1 Loop Size and Proximity

The inductance of a loop (L) increases with loop size. When two loops interact, one will have a primary inductance (LP) and the other will have a secondary inductance (LS), as shown in Figure 33b. Because the signal lines are not purposely designed to be transformers, the coupling is loose; however, it can create interference on the secondary loop.

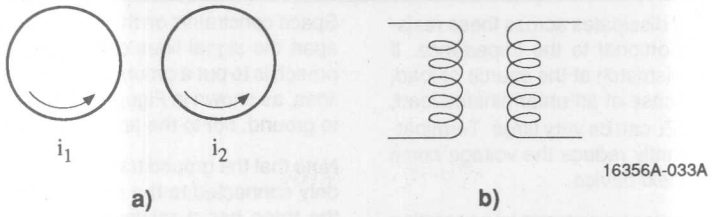


Figure 33. a) Inductive Crosstalk; b) Transformer Equivalent

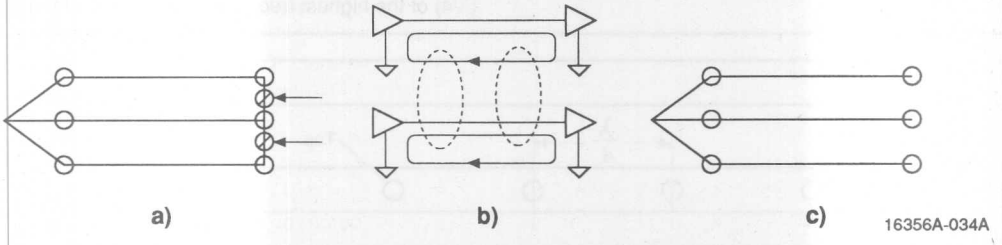


Figure 34. a) Artificial Loops; b) Schematic Equivalent; c) Solution

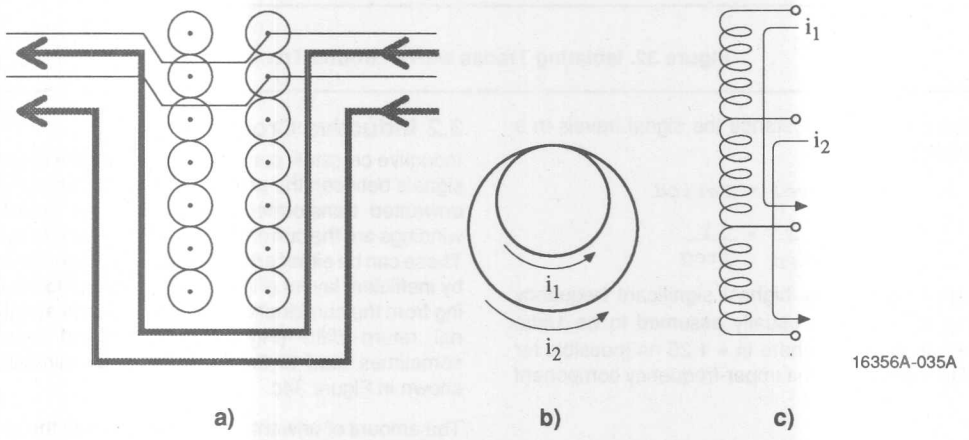


Figure 35. a) Common Return Path; b) Loop; c) Autotransformer Equivalent Circuit

If portions of the return paths of two signal lines coincide, the resulting loops might form an auto-transformer (Figure 35 a and c). An example of this is the VME-backplane example discussed above. Ensuring that each signal has its own return path can eliminate this source of crosstalk.

3.2.2 Load Impedance

If inductive crosstalk comes about due to artificial loops, the solution is to open the loops. Unfortunately, locating the loops can often be a challenge. If the crosstalk is generated by natural signal / return-signal loops, then clearly the loop cannot broken. But by keeping the load impedance low, the effect of the crosstalk can be minimized. Figure 36 shows a simplified schematic representation of a secondary "natural" loop with a load. Here Zs is the intrinsic impedance of the secondary loop. Note the series current (is). Because the impedances are in series, is is the same everywhere in the loop. With a constant is, the voltage drop is largest across the largest impedance. On an unterminated line, this usually is the load at the end of the line; i.e., at the input of the receiving device.

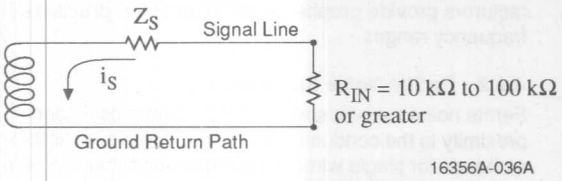


Figure 36. Series Inductive Loop

Large noise signals are most unwanted at the inputs, where noise signals should be minimal. If the maximum signal is developed across the largest impedance, the signal developed at the input can be reduced by terminating the signal line at the receiver end, which reduces R_{IN} to R_T.

R_T is usually in the 30 Ω to 150 Ω range. This reduction in R_{IN} is at least two orders of magnitude. The voltage drop across R_{IN} is reduced accordingly. The exact drop is difficult to predict because it depends on the value of Z_S, which is difficult to determine. But reducing R_{IN} by orders of magnitude should have a significant effect.

3.3 Crosstalk Solutions Summary

The following steps summarize the ways in which the effects of crosstalk can be minimized.

1. The effect of both capacitive and inductive crosstalk increases with load impedance. Thus all lines susceptible to interference due to crosstalk should be terminated at the line impedance.
2. Keeping the signal lines separated reduces the energy that can be capacitively coupled between signal lines.
3. Capacitive coupling can be reduced by separating the signal lines by a ground line. To be effective, the ground trace should be connected to the ground plane every λ/4 inches.
4. For inductive crosstalk, the loop size should be reduced as much as possible. Where possible, loops should be eliminated.
5. For inductive crosstalk, avoid situations where signal return lines share a common path.

4. ELECTRO-MAGNETIC INTERFERENCE (EMI)

EMI is becoming more critical with speed. High-speed devices are naturally more susceptible to interference. They accept fast glitches, which slower devices ignore. Even if the board or system is not susceptible, the FCC in the United States, along with VDE and CCITT in Europe, places severe limitations on the high-frequency noise (both radiated and line noise) that the board can generate.

The designer can reduce EMI through shielding, filtering, eliminating current loops, and reducing device speed where possible. Although shielding is outside the scope of this article, all the other issues are discussed as follows.

4.1 Loops

Current loops are an unavoidable part of every design. They act as antennae. Minimizing the effects of loops on EMI means minimizing the number of loops and the antenna efficiency of the loops. Do not create artificial loops; and keep the natural loops as small as possible.

1. Avoid artificial loops by ensuring that each signal line has only one path between any two points.
2. Use power planes whenever possible. Ground planes automatically result in the smallest natural current loop. When using ground planes, ensure that the signal-return line path is not blocked.

   If power buses are necessary, have the fast-signal lines run either over or next to a power bus.

4.2 Filtering

Filtering is standard for power lines. It can also be used on signal lines, but is recommended only as a last resort, when the source of the signal noise cannot be eliminated.

Three options are available for filtering: bypass capacitors, EMI filters, and ferrite beads. Bypass capacitors are discussed in section 1. EMI filters are commercially available filters; they are available over a wide frequency range. Ferrite beads are ferrite ceramics that add inductance to any wire within their proximity. They are used as high-frequency suppressors.

4.2.1 EMI Filters

EMI filters are commercially manufactured devices designed to attenuate high-frequency noise. They are used primarily to filter out noise in power lines. They act to isolate the power outside the system (referred to as the line) from the power inside the system (referred to as the load). Their effect is bi-directional: they filter out noise going into, and coming out of, the device or board.

EMI filters consist of combinations of inductors and capacitors. In general, the configuration to use depends on the impedance of the nodes to be connected. A capacitor should be connected to a high-impedance node; an inductor should be connected to a low-impedance node. EMI filters are available in variations of the following configurations: feedthrough capacitor, L-Circuit, PI-Circuit, and T-Circuit.

- The feedthrough capacitor's only component is a capacitor (Figure 37a). It is a good choice when the impedances connected to the filter are high. Note that it provides no high-frequency current isolation between nodes.
- The L-Circuit has an inductor on one side of a capacitance (Figure 37b). It works best when the line and load have a large difference in impedance. The inductive element is connected to the lowest impedance.

- The PI-Circuit has an inductor surrounded by two capacitors (Figure 37c). PI filters are best when the line and load impedances are high and when high levels of attenuation are needed.
- The T-filter has inductors on either side of the capacitor in a T fashion (Figure 37d). It is a good choice when both line and load impedances are low.

LC filters are rated according to insertion loss, which is the amount of signal lost due to the insertion of the filter. Insertion loss is usually stated in decibels. Filter manufacturers provide graphs of their filters over prescribed frequency ranges.

4.2.2 Ferrite Noise Suppressors

Ferrite noise suppressors are ferrite ceramics placed in proximity to the conducting material. They are available as beads for single wires and clamps for cables. When using beads, the wire is placed through a hole in the bead (Figure 38a). When using clamps, the ferrite material is clamped around the cable (Figure 38b). Clamps are popular with ribbon cable.

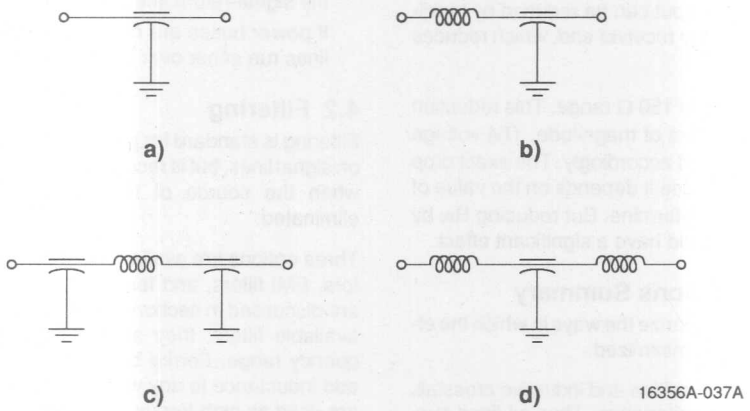


Figure 37. Line-Noise Filters. a) Capacitor; b) LC Filter; c) PI Filter; d) T Filter

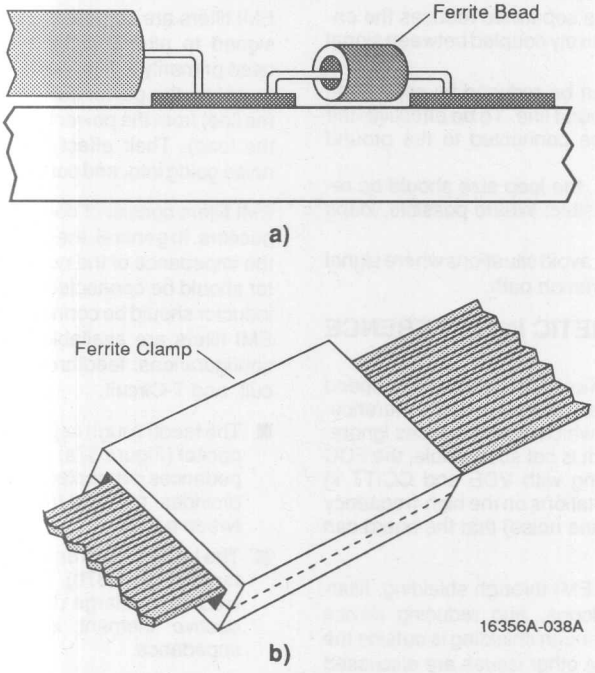


Figure 38. a) Ferrite Bead; b) Ferrite Clamp

Ferrite suppressors work by adding inductance in series with the line (Figure 39). Ferrite manufactures supply graphs similar to those in Figure 40, which shows the added impedance as a function of frequency. The system designer must determine the insertion loss. The formula is:

$$\text{Loss (db)} = 20 \log_{10} \frac{Z_S + Z_L + Z_F}{Z_S + Z_L}$$

where Z_S = Source Impedance
Z_L = Load Impedance
Z_F = Ferrite Impedance

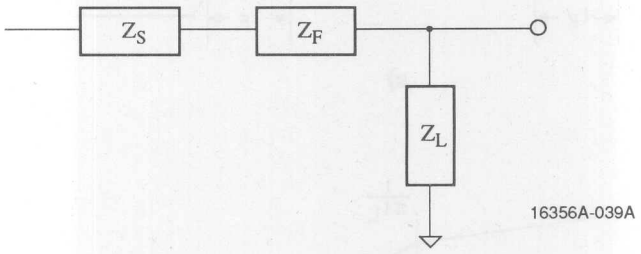


Figure 39. Ferrite Filter Equivalent Circuit

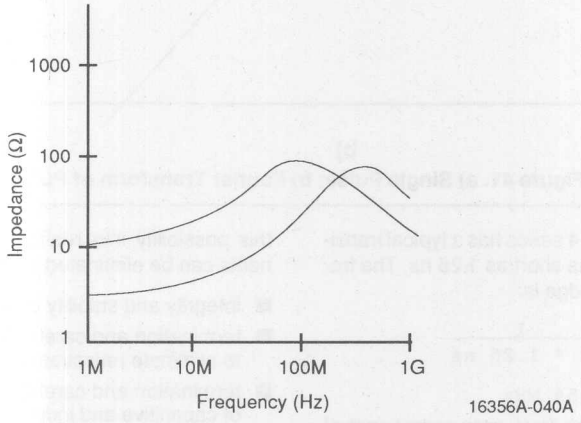


Figure 40. Frequency Response of Ferrite Filter

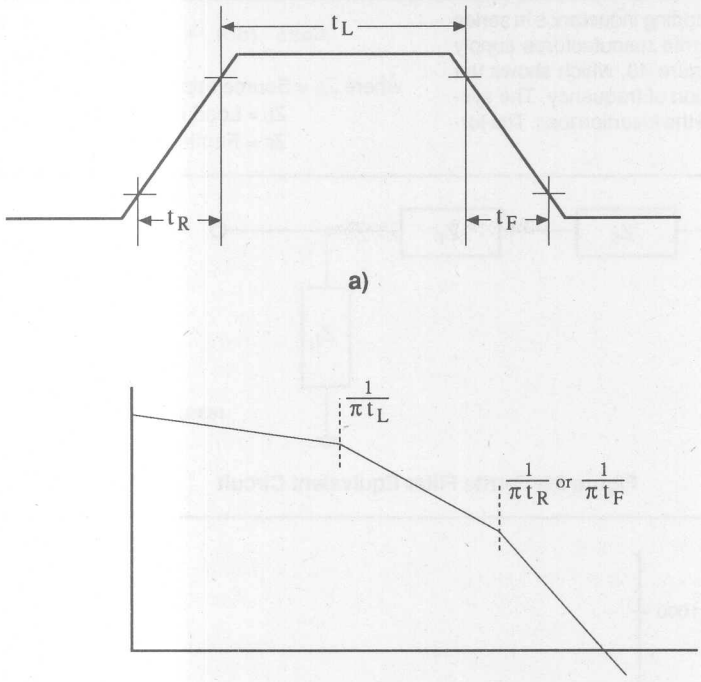
Ferrite suppressors add inductance to the line without adding DC resistance. This makes an ideal choice for line-noise suppressors on the V_{CC} pins of devices.

Because ferrite beads are small and easy to handle, they can sometimes be used in signal lines to suppress high-frequency noise signals. This is not recommended for two reasons: first, it masks the cause of most problems; second because it might affect the edge rates of the signal. However, when the board is already laid out, ferrite beads can be used on noisy signal lines as a last resort.

4.3 Device Speed

The less energy a device generates in a given frequency range, the less noise can be radiated in that range. Faster devices, by definition, have shorter transition times. Because shorter transition times have more energy in the high-frequency range, faster devices can generate more high-frequency noise.

Figure 41a is an outline of the Fourier transform of a square wave (Figure 41b). There are two corners of interest: $1/\pi tL$(this frequency is determined by the period of the signal) and $1/\pi tf$ (determined by the transition time of the signal; this is also the frequency we used in determining the wavelength in the discussion on capacitive coupling). After $1/\pi tf$, the curve drops off very rapidly. For practical purposes, $1/\pi tf$ is the highest significant frequency component of the signal.



16356A-041A

Figure 41. a) Single Pulse; b) Fourier Transform of Pulse

For example, the PAL16R8-4 series has a typical transition time of 2 ns. It can be as short as 1.25 ns. The frequency component of the edge is:

$$f = \frac{1}{\pi * 1.25\ ns}$$

$$= 254\ MHz$$

The output signal has a high-frequency component of 254 MHz, regardless of the clock frequency.

Because of the high-frequency component, the board might require extra filtering and possibly shielding in order to comply with EMI emissions restrictions required by regulatory agencies.

If the system speed requirements are high enough (for example, clock rates over 80 MHz), devices this fast must be used, and the extra effort required to meet compliance is justified. However, if a slower device can meet system requirements, it should be used. By virtue of the longer transition time, the slower device generates less energy at the higher frequencies. In general, try to use devices that are fast enough to meet the system requirements, but no faster.

SUMMARY

While faster technologies provide the theoretical possibility of faster systems, extra care must be taken to turn this possibility into reality. The largest noise components can be eliminated by addressing the following:

- integrity and stability of power and ground;
- termination and careful layout of transmission lines to eliminate reflections;
- termination and careful layout to reduce the effects of capacitive and inductive crosstalk;
- noise suppression for compliance with radiation regulations.

There are many other second-order issues that could be addressed, but that are beyond the scope of the application note. Some references for additional information are listed below.

1. Sherman Lee, Mark McClain, Dave Stoenner. "Am29000 32-Bit Streamlined Instruction Processor Memory Design Handbook," Advanced Micro Devices Inc., Sunnyvale, CA, Appendix A, Memory Array Loading Calculations.
2. William R. Blood Jr. "ECL Systems Design Handbook," Motorola Semiconductor Products Inc., Mesa, AZ, May, 1983 (Fourth Edition) Chapters 3 and 7.
3. Ramo, Whinnery, and Van Duzer, "Fields and Waves in Communications Electronics," John Whilley & Sons, 1965, Chapter 1.

Minimizing Power Consumption with Zero-Power PLDs

Application Note

by Shawn D. Worsell, Senior Applications Engineer

Advanced Micro Devices

Zero-Power Programmable Logic Devices (PLDs) are advanced PAL devices designed with ultra low-power, high-speed, electrically-erasable CMOS technology. ZPAL™ devices provide zero-standby power and high speed for a variety of applications. At 15 µA maximum standby current, Zero-Power devices allow battery powered operation for an extended period of time. Zero-Power CMOS devices can significantly reduce system power consumption by replacing equivalent CMOS and TTL devices.

ZPAL devices are available in the following configurations: the industry-standard 20-pin PALCE16V8Z family and the AMD-patented 24-pin PALCE22V10Z family.

The PALCE16V8Z family is functionally compatible with all CMOS half- and quarter-power PALCE16V8 devices and will directly replace the bipolar PAL16R8 and PAL10H8 series devices with the exception of the PAL16C1.

The PALCE22V10Z family is functionally compatible with all 24-pin 22V10 devices, and it provides user-programmable logic for replacing conventional low-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

POTENTIAL APPLICATIONS

ZPAL devices may be used in any application where a standard 22V10 or 16V8 device would be used. Designs that are currently in a 20V8 will also fit in the 24-pin 22V10 device. In addition, they are ideal for low-frequency or low-duty-cycle environments such as line card and peripheral applications, where low power consumption is a priority. Laptop computers and other battery-operated or backed-up equipment, such as hand-held meters and portable communication units, would benefit from the Zero-Power devices.

The PALCE16V8Z and PALCE22V10Z feature a zero-standby power mode. When none of the inputs switch for an extended period, the device will go into standby mode, shutting down most of its internal circuitry, causing the current consumption to drop to almost zero (15 µA). The outputs will maintain the states held before the device went into the standby mode. When any input switches, the internal circuitry is fully enabled, and power consumption returns to normal.

Since all of the features which cause the device to be a Zero-Power PLD are internal, the 16V8Z and the 22V10Z PAL devices are pin-for-pin and JEDEC-file compatible with existing devices of the same families.

HINTS ON MINIMIZING POWER CONSUMPTION

The quintessential feature of the ZPAL device's current reducing operation is the "sleep mode." When the device is inactive for a period of time, certain portions of the PLD can be disabled or "put to sleep" by the presence of input transition detection circuitry. Any switching delays of about 50 nanoseconds or more, for the entire device, will place the PLD in sleep mode. This means that none of the inputs, including the clock, can be switching in order to utilize the significant power saving features. Therefore, during the design phase, special attention must be given to *every* signal that is being transferred to the device, so that the sleep mode feature may be engaged as much as possible. Refer to Figure 1 for ZPAL device features.

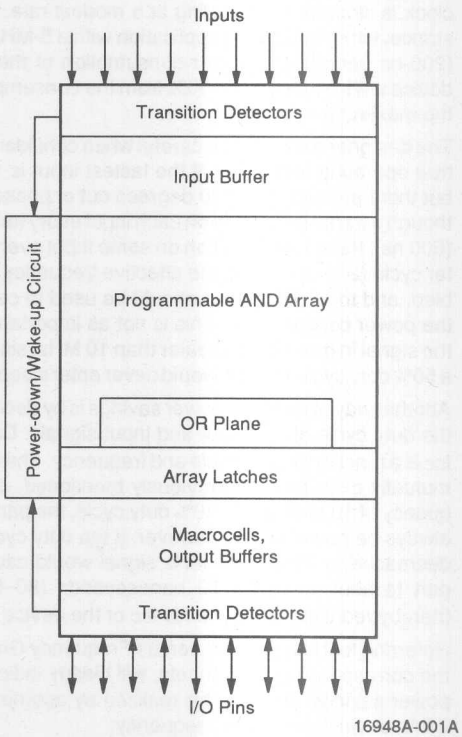


Figure 1. ZPAL Device Features

Publication# 16948 Rev. A Amendment /0
Issue Date: June 1992

As sleep mode is asserted, all outputs will latch to the state they were in when the last input transition occurred. This state will be held as long as the device is asleep.

When an input does experience a transition, the device will "wake up." The wake-up delay associated with the initial transition is included in the determined propagation delay of the device. Therefore, there are no extra system delays to consider when the device utilizes the standby feature, since it quickly returns to full operation. However, if a designer is more interested in high speed, such as a burst mode application, a typical propagation delay would be closer to 5 nanoseconds faster while the device is awake.

The inputs and I/O pins are monitored by an input transition detection circuit. Any transition on any pin, including noise spikes, will disengage the sleep mode. Thus, during the design phase, care should be taken to ensure that *all* circuitry associated with the Zero-Power device is as quiet as possible.

Effects of Frequency

The sleep mode benefits are best realized in combinatorial applications since sequential functions will be powered-up with every edge of the clock. However, significant power savings can still be realized when the clock is stopped or operating at a modest rate. For instance, when used in an application with a 5-MHz clock (200-ns period), the power consumption of the ZPAL device will be reduced by 50% from the consumption at the maximum frequency.

The designer must also be careful when considering the true operating frequency. If the fastest input is 1 MHz, but there are two inputs 90 degrees out of phase, even though a transition occurs on each input every half-cycle (500 ns), there is a transition on some input every quarter cycle (250 ns). Thus, the effective frequency is doubled, and the 2-MHz point should be used to calculate the power consumption. This is not as important when the signal in question is greater than 10 MHz, since with a 50% duty cycle the part would never enter sleep mode.

Another way of realizing power savings is by decreasing the duty cycle of the clock and input signals. Dynamic I_{CC} is a function of duty cycle and frequency. The two are mutually exclusive. As previously mentioned, at a frequency of 10 MHz with a 50% duty cycle, the part would always be powered up. However, if the duty cycle was decreased to 20%, a 10-MHz signal would cause the part to shut down for 30 nanoseconds (80–50 ns), thereby reducing the Dynamic I_{CC} of the device.

Referring to the typical I_{CC} versus Frequency Graphs of the corresponding data sheets, will clearly indicate the power savings that may be realized by optimizing the ZPAL device's operating frequency.

Effects of Product Terms

To further reduce power consumption, unused product terms are permanently disabled during programming. Each product term has a Sense Amp Off (SAOFF) bit, which will be programmed when the corresponding product term is unused, thereby shutting off the sense amp to save power. Note that the SAOFF bit is automatically configured and has no effect on the JEDEC file, so the designer does not even have to think about it. A typical power savings of approximately 300 µA per unused product term will be achieved. Thus, a logic design that utilizes a minimum number of product terms will result in the maximum amount of power savings.

Inverting simplified logic by using DeMorgan's theorem and changing the output polarity is one way that a designer may easily reduce product term requirements. For example, in the equation

$$Z = X+Y$$

the "OR" function denoted by the "+" sign, requires two product terms, one for each variable. However, if both sides of the equation are inverted to become

$$/Z = /(X+Y)$$

using DeMorgan's theorem yields

$$/(X+Y) = /X*/Y$$

Here the "AND" function denoted by the "*" sign does not use the second product term, because one product term is shared by both variables. The resultant equation is now

$$/Z = /X*/Y$$

and by switching the output polarity, the logic behaves the same way as it was originally intended as well as reducing a product term requirement.

The choice of output polarity itself does not save power, but if chosen wisely, it may help to reduce product term usage. It should also be noted, however, that switching output polarity will also invert the Synchronous Preset (SP) and Asynchronous Reset (AR) functions at the output of the register of a 22V10.

I/O Characteristics

The output stage of the Zero-Power PAL devices consist of a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail switching. A P-channel pull-up is better for low-power applications than an N-channel transistor, since P-channel outputs can be driven up to the V_{CC} level. This ensures that the following input buffer draws no current. The same amount of current is available for both high and low outputs with a P-channel pull-up, unlike the unequal, although slightly faster N-channel transistor used in other PLD products.

These devices are capable of driving and being driven by either TTL or CMOS devices. They are compatible with both HC and HCT standard specifications as illustrated in Table 1.

Table 1

Parameter	HC	HCT	ZPAL
V_{IH}	3.15 V	2.0 V	2.0 V
V_{IL}	0.9 V	0.8 V	0.9 V
V_{OL} @ 6 mA	0.33 V	0.33 V	0.33 V
V_{OL} @ 20 µA	0.1 V	0.1 V	0.1 V
V_{OH} @ 6 mA	3.84 V	3.84 V	3.84 V
V_{OH} @ 20 µA	V_{CC} –0.1 V	V_{CC} –0.1 V	V_{CC} –0.1 V

One minor disadvantage of true CMOS outputs is the intrinsic SCR circuit that is developed in the CMOS structure and cannot be eliminated. The SCR has been made as difficult as possible to turn on by using guard rings and carefully laying out all input and output circuits. An excess current of 100 mA would be required on an individual pin to induce "latch-up". However, there is a potential to latch-up a ZPAL device through hot-socket insertion. If there is a possibility of the device or board being instantly powered-up, design care must be taken.

Effects of Reducing I/O Switching

Since each input will draw up to a maximum of 5 mA each time it switches, additional power savings are possible by reducing the number of inputs used. A CMOS transistor pair only draws current when it is switching or floating in an intermediate region, so unused inputs should be externally tied either HIGH or LOW. The number of outputs switching will also affect the amount of current consumption. Therefore, minimizing output switching will also help to reduce the amount of current required.

The potential for ground bounce problems will also be reduced by limiting the number of outputs switching. Built-in slew-rate-limiting circuits will help to slow down the fast CMOS falling edges that contribute to ground bounce. A fall rate of 1.25 V/ns is typical of the faster N-channel pull-down transistor, while a slower rise rate of 1 V/ns can be expected from the P-channel pull-up. If most of the outputs are required to switch simultaneously, it is important to ensure that the ground path on the circuit board has low inductance, and to reduce the loading on the outputs. The lower-lead-inductance PLCC package will also reduce the possibility of ground bounce since the bonding wires are 1/4 the length of a DIP's bond wires.

Effects of Loading

Power dissipation of the outputs is greatly affected by the load. To minimize power dissipation, ZPAL device loads should have no DC components. If termination is required, an AC terminator like the one in Figure 2 should be used to eliminate DC power drain.

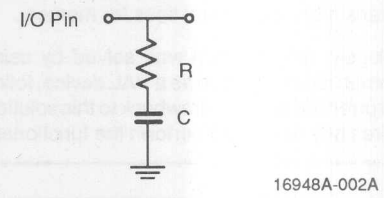


Figure 2. Typical AC Terminator

The capacitance should generally be kept as low as possible since the output stage will go through a process of constantly charging and discharging the capacitor. The formula for current consumption due to loading is

$$i = C_L V s f o$$

where i is the current, C_L is the capacitive load, Vs is the voltage swing, and fo is the frequency at which the output is switching. Therefore, current is consumed every high transition since the capacitor has to recharge.

SUMMARY

ZPAL devices provide zero-standby power and high speed for a variety of applications. Zero-Power CMOS devices can significantly reduce system power consumption by replacing equivalent CMOS and TTL devices. Since all of the features which cause the device to be a Zero-Power PLD are internal, the 16V8Z and the 22V10Z PAL devices may be used in any application where a standard 22V10 or 16V8 device would be used. With a little extra attention given to the particular design involving a Zero-Power PAL device, a designer can realize significant system power savings.

Designing with the PALCE16V8HD

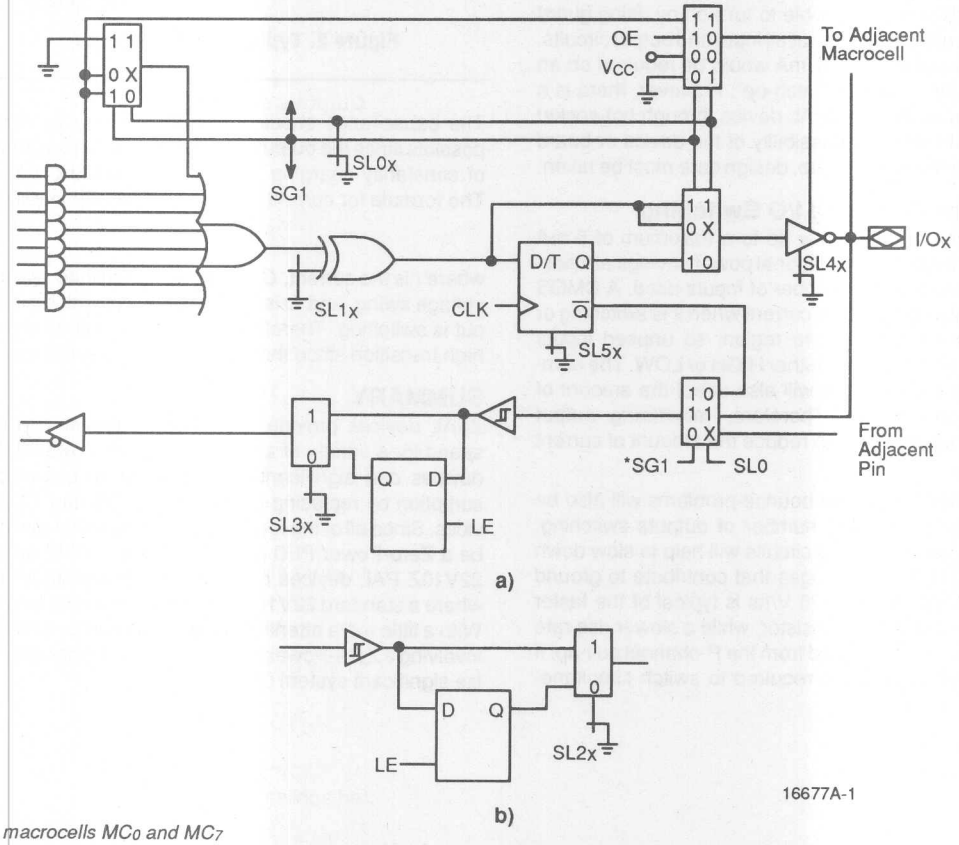
Advanced Micro Devices

Application Note

The PALCE16V8HD is a HIgh Drive PLD that combines the popular PALCE16V8 architecture with 64-mA current drivers. It has application anywhere a reasonably complicated function must control a high-current signal line. Examples of this are control signals for buses such as the VME bus, combination decoder and LED driver, 3 V translator, and control lines for memory.

Previously, this problem was solved by using a programmable device, such as a PAL device, followed by a highcurrent driver. The drawback to this solution is that it requires two devices to perform the functionality of one device. The extra device increases part count and increases total propagation delay.

The PALCE16V8HD is an ideal replacement for the pair of devices. First, it combines the full functionality of a PAL device and 64-mA current sink capability into one device. Second, it provides input latches to store information. Third, it provides the choice of either totem-pole or open-drain output drivers. Finally, it has a minimum of 200-mV hysteresis on all input and I/O pins for increased noise immunity. The macrocell is shown in Figure 1.



**In macrocells MC_0 and MC_7*

SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

Figure 1. a) PALCE16V8HD I/O Macrocell; b) PALCE16V8HD Input Macrocell

Publication# 16677 Rev. A Amendment/0
Issue Date: April 1993

The purpose of this application note is to guide the engineer in using the PALCE16V8HD high drive-current PAL device. What follows is a discussion of its features and hints on how to maximize their benefits.

Input Latches

All inputs to the device (including I/O pins) can be programmed as a transparent latch. The latch enable (LE) signal is pin 4 (pin 5 for PLCC). The latches are transparent when LE is HIGH and latched when LE is LOW.

Input latches provide a convenient way to speed up data transfer while providing storage at the same time. With latches, the new data is available instantaneously, while with registers, the data is not available until the next clock edge. The input-latch setup time is also short because the product-term array is bypassed. The register-setup time is 10 ns, while the latch-setup time is only 4 ns. This last feature makes it possible to capture signals which tend to occur late in the clock cycle.

The PALCE16V8HD is designed so that the transparent latch does not add extra delay to the signal. This makes the PALCE16V8HD faster than the usual PAL device and input latch combination.

Register Configurations

The output registers can be configured as either D-type or T-type flip-flops. The D-type register's Q output is equal to the D input at the rising edge of the clock. The T-type registers output toggles when the corresponding T input is HIGH and maintains the current state when the T input is LOW. The T-type register's action is also determined at the rising edge of the clock signal.

The D-type register has the advantage of simplicity. It is straight forward and the easiest to determine the desired results.

In many applications, such as counters, the T-type flip-flop requires fewer product terms. If the application is large enough, this can mean the difference between fitting or not fitting on the part.

T-type flip-flops tend to reduce the number of product terms required in sequential applications such as counters and state-machines. They are not optimal for all applications. For example, to load data takes two product terms with a T-type flip-flop and only one product term with a D-type flip-flop. Because the PALCE16V8HD can be configured as either type, it has a wider range of application than either one alone.

Note that because there is no global initialization function, designers should be sure that T-type flip-flops have a direct way of being initialized. This can most easily be done by ensuring that there is at least one LOAD product term. A LOAD product term is one that can be activated with no other product term active, and which will have the flip-flop toggle only if the flip-flop state is presently in the state opposite the desired initialized state. An example is shown below.

```
OUT1.T = A*B*OUT1*/OUT2        ;application
                               ;equations
       + /A*/B*/OUT1*
         /OUT2                 ;"
       + INIT_LOW*OUT1         ;toggles to
                               ;LOW if HIGH
       + INIT_HIGH*/OUT1       ;toggles to
                               ;HIGH if LOW
```

Output Driver Configurations

The output macrocells can be independently configured as either totem-pole outputs or open-drain outputs. In the totem-pole configuration the driver has an n-channel pull-down transistor and an n-channel pull-up transistor. The output-LOW voltage is typically 0.3 V and the output-HIGH voltage is typically 3.5 V. In the open-drain configuration, the n-channel pull-up transistor off. The output-LOW voltage is the same as in the totem-pole configuration. The output-HIGH voltage is determined by the termination voltage and the load on the signal line.

Totem-Pole Output Configuration

The totem-pole output driver conforms to TTL specifications. Because the pull-up transistor is n-channel, the output-HIGH voltage is 1 to 1.5 volts below V_{CC}, even under zero-load conditions. If rail-to-rail swings are required, V_{OH} can be raised by terminating the output with a resistor to V_{CC}.

Open-Drain Outputs

The open-drain configuration has two types of applications. The first is as a switch to apply power to devices such as a small lamp or even a small motor. The second is as an active-LOW signal source on a signal line with multiple asynchronous drivers. Because the pull-up transistor is always off, the risk of device damage due to contention is eliminated. If the output structure were totem-pole only, the state of the output would have to be set internally and then the output would be enabled. The open-drain structure eliminates this extra complexity.

An example of asynchronous signals on one line is the bus request for VME buses. For open-drain outputs, the request line simply goes LOW. Simultaneous requests must be handled by an arbiter, but there is no risk of circuit damage due to bus contention.

Output Terminations

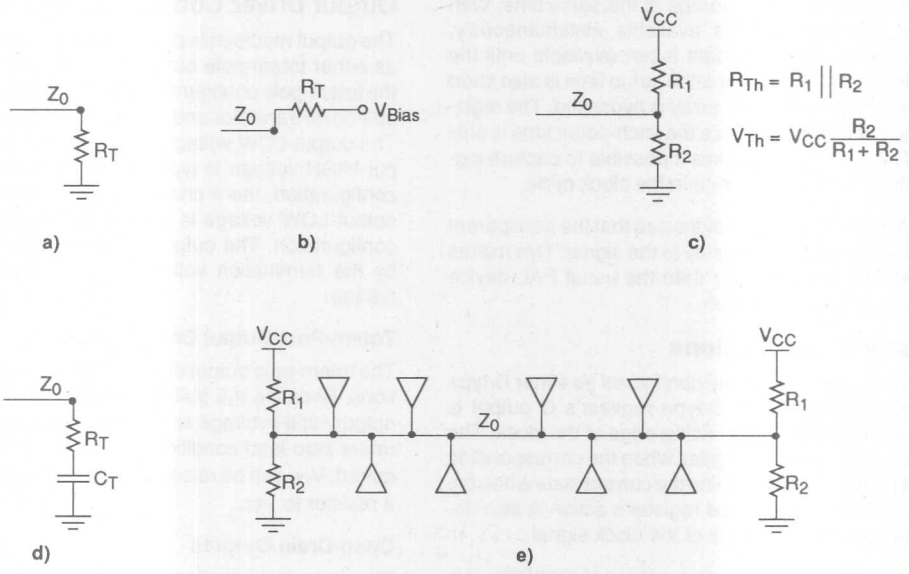
The anticipated applications for the PALCE16V8HD include relatively long signal-line lengths. At the rise and fall times of this device (2 to 3 ns), the signal lines resemble transmission lines. The transmission line's propensity for reflections requires the use of terminating techniques. It is beyond the scope of this article to pre-

sent a detailed discussion of transmission lines, but we will discuss some of the more popular termination techniques that lend themselves well to high-drive devices. Those interested in studying transmission lines in more detail are encouraged to check out the references at the end of this application note.

Terminating Totem-Pole Outputs

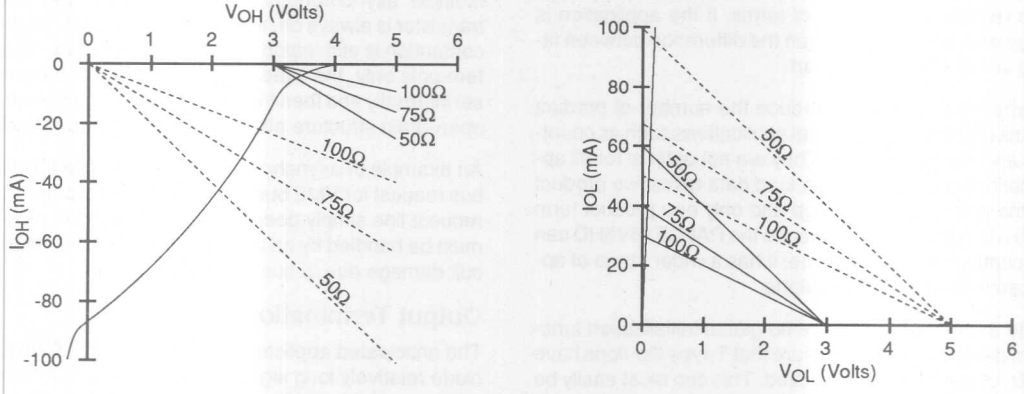
The most effective termination is a resistor at the load end of the signal line that is equal to the line impedance (Figure 2a). Because the input impedance of all PLDs is greater than 10 kΩ, this is effectively an exact match.

Because parallel termination increases the DC load, the output will be degraded for both V_{OH} and V_{OL}. The I/V curves for the device (Figure 3) can be used with a load line to determine the degraded output levels. The dashed lines indicate simple termination to V_{CC} or ground.



16677A-2

Figure 2. Termination Alternatives: a) Parallel; b) Active; c) Thévenin; d) AC; e) Multiple Drivers



16677A-3

Figure 3. Terminating Load Lines: a) HIGH Output; b) LOW Output

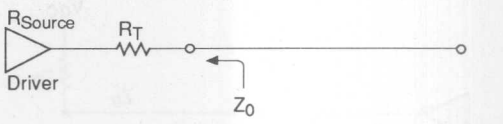
If the degraded output is outside acceptable limits, the terminating resistor can be referenced to a separate power source (Figure 2b). The reference voltage is selected so that output drive currents for both HIGH and LOW levels are within the operating ranges of the device. The solid load lines in Figure 3 show the output degradation when R_T is referenced to 3.0 V. Note that the voltage source must also be chosen to be able to change between sourcing and sinking current at the fast switching speeds of the PALCE16V8HD.

If a reference power supply is not a viable option, it may be replaced with its Thévenin equivalent (Figure 2c). The resistors are chosen so that the parallel combination of R_1 and R_2 is equal to R_T and V_0 is equal V_{REF} when the line is open. The loading effect of a 3-V Thévenin equivalent bias is also indicated by the solid load lines in Figure 3.

Another option is to place a capacitor in series with R_T (Figure 2d). Because the capacitor is a DC open, the termination presents a load equal to Z_0 at the edges of the signal, where termination is needed. At other times the termination presents a negligible load.

If multiple drivers are used on the same signal line, both ends of the line should be terminated as in Figure 2e. Although the AC load is R_T, the DC load is the parallel combination of the loads at both ends of the line. This effectively doubles the DC load. This should be taken into consideration when selecting R_1 and R_2.

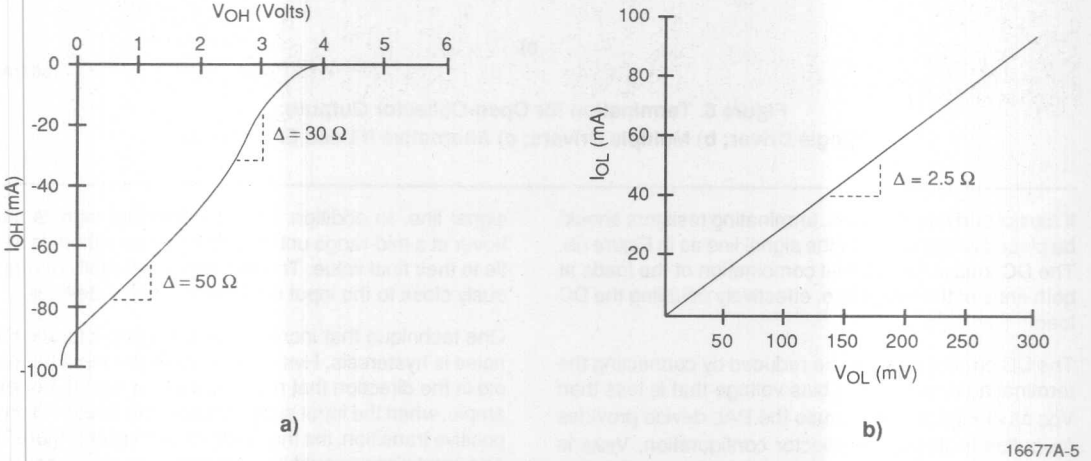
Another technique that reduces DC loading is series termination. Here a resistor is placed in series with the driver and the signal line (Figure 4). R_T is chosen so that it increase the value of the output impedance to match Z_0. The advantage of this technique is that it does not add any load to the output driver. The disadvantage is that the device has different output impedances for HIGH and LOW output; therefore it is impossible to exactly match the device to the signal line for both HIGH and LOW transitions.



16677A-4

Figure 4. Series Termination

The output impedances are shown in Figure 5. Note that the output impedance is 2.5 Ω for a LOW output and 50 Ω for a HIGH output. When using series termination, a compromise value is required for R_T. The value depends on the Z_0 and the amount of ringing the system can tolerate. Because there will always be some ringing, this configuration should be avoided for noise-sensitive signals.



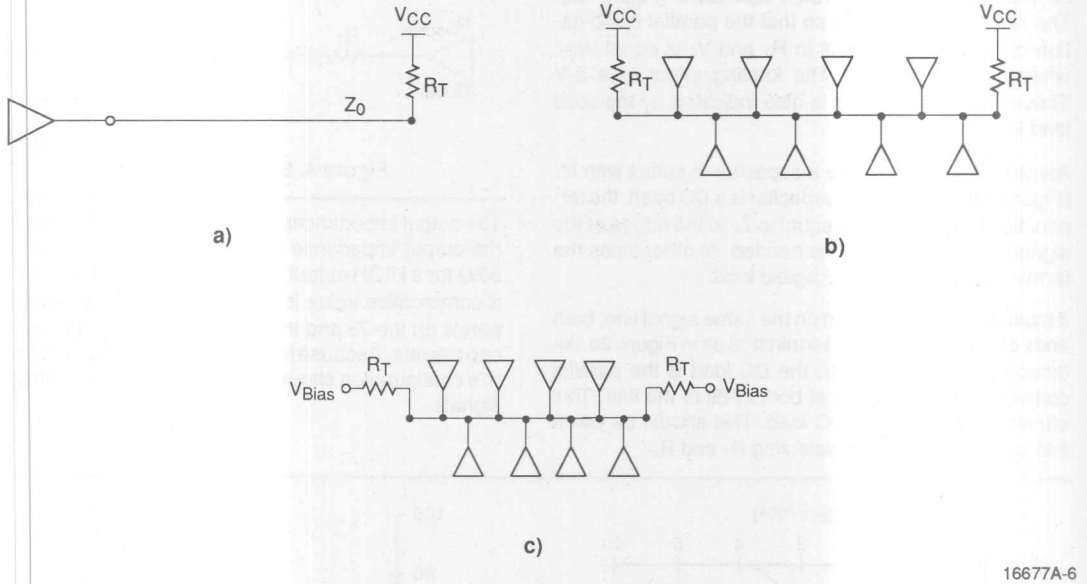
16677A-5

Figure 5. Output Impedances: a) HIGH Output; b) LOW Output

Terminating Open-Drain Outputs

The open-drain configuration is simply a single pull-down transistor with the drain connected to the output. The transistor turns on and off very fast. When the transistor turns on, it provides a low impedance for the load capacitance to discharge into. Therefore, the fall time (t_f) of the output is short, in the range of 2 ns to 3 ns. When the transistor turns off an extremely high impedance is presented to the load. The only discharge path is that provided by the load and any external termination. Therefore, the rise time (t_R) depends on the RC-time constant formed by the line capacitance and the terminating resistance.

The recommended termination scheme is shown in Figure 6a. The value of R_T should be equal to the impedance of the line. This is different from the usual resistor pair termination because the terminator itself must provide the logic HIGH level. R_T is placed at the load end of the line.



16677A-6

Figure 6. Termination for Open-Collector Outputs:
a) Single Driver; b) Multiple Drivers; c) Alternative if Load Exceeds I_{OL}

If multiple drivers are used, terminating resistors should be placed at both ends of the signal line as in Figure 6b. The DC load is the parallel combination of the loads at both ends of the signal line, effectively doubling the DC load.

The DC current load can be reduced by connecting the terminating resistors to a bias voltage that is less than V_{CC} as in Figure 6c. Because the PAL device provides no pullup in the open-collector configuration, V_{BIAS} is V_{OH}; therefore V_{BIAS} must be high enough to ensure a valid logic HIGH to all the device inputs on the signal line.

Hysteresis

Buses tend to operate in a noisy environment. Voltage spikes from crosstalk can be expected on almost every signal line. In addition, series-terminated signals can hover at a mid-range until reflections cause them to settle to their final value. The mid-range is usually dangerously close to the input thresholds of most devices.

One technique that increases the devices tolerance to noise is hysteresis. Hysteresis moves the input threshold in the direction that requires a larger signal. For example, when the input signal crosses the threshold on a positive transition, the threshold moves lower (Figure 7). The input signal would have to move lower to cross the new threshold. Therefore, even a noisy signal will cause a single crossing per transition, not the multiple crossings that might occur without hysteresis.

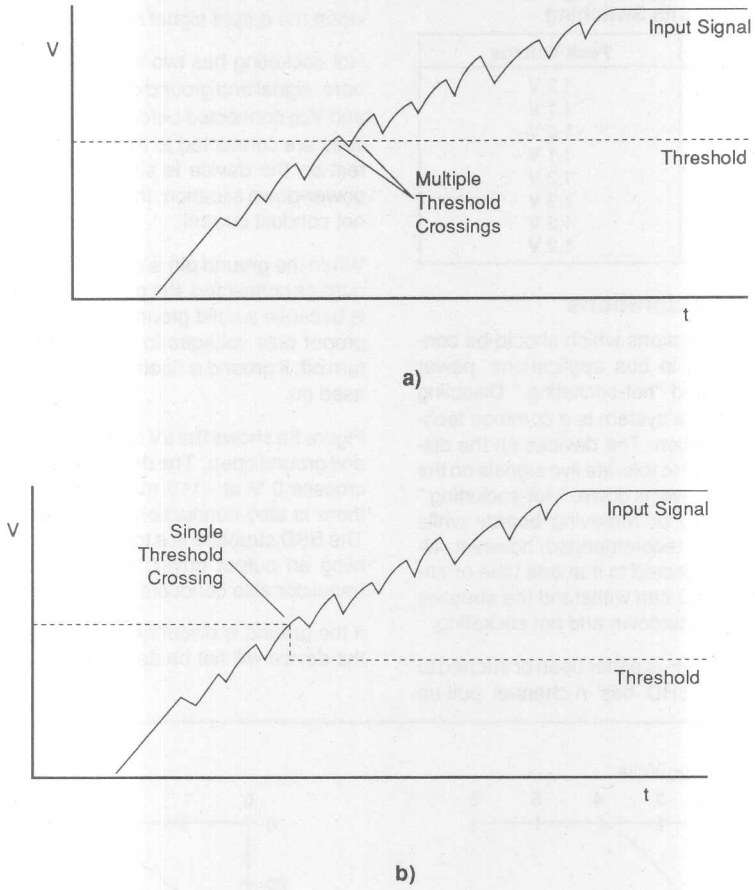


Figure 7. Response to Noisy Inputs:
a) Device with no Input Hysteresis; b) Device with Input Hysteresis

The PALCE16V8HD comes with a minimum of 200 mV hysteresis. Therefore, if the noise occurs when the input signal level is at the exact middle of the threshold range, the device can tolerate 200 mV peak-to-peak of noise before detecting multiple transitions.

Ground Bounce

An issue that is associated with high-current CMOS is ground bounce. This phenomenon is usually first noticed as a pulse or ringing on a LOW output. If these pulses are large enough they can generate false clocking or false data. The design of the PALCE16V8HD takes ground bounce into consideration so that it is minimized.

The PALCE16V8HD has two features which make it resistant to ground bounce: multiple ground pins and slew rate limiting. The multiple ground pins share the switching current. Because there is less current in any one ground pin, there is less energy available to generate ground bounce. Slew rate limiting reduces the current surge in the ground pin. Together these features keep ground bounce down to a tolerable level.

The following table shows ground-bounce data measured under worst-case conditions: all eight macrocells in the registered configuration and seven outputs switching simultaneously. The measured pin is in the LOW state during the test. The test was performed with the following AC test load: 80 Ω to V_{CC}, 160 Ω to ground, and 50 pF to ground.

Note that the maximum transient V_{OL} is 1.3 V, which shows that ground bounce on the PALCE16V8HD is equal to, or better than, ground bounce on devices with only 24-mA drive current capability.

Ground Bounce Peak Voltage with Seven Outputs Switching

LOW Pin #	Peak Voltage
23	1.2 V
22	1.1 V
20	1.0 V
19	1.1 V
16	1.2 V
15	1.3 V
14	1.3 V
13	1.2 V

Power Supply Considerations

There are two special situations which should be considered for devices used in bus applications: power down with live signals and "hot-socketing." Disabling V_{CC} of certain sections of a system is a common technique for power conservation. The devices on the disabled board should be able to tolerate live signals on the input and I/O pins while power is down. "Hot-socketing," the technique of inserting or removing boards while power is applied, is never recommended; however, almost every system is subjected to it at one time or another. The PALCE16V8HD can withstand the stresses brought about by power shutdown and hot socketing.

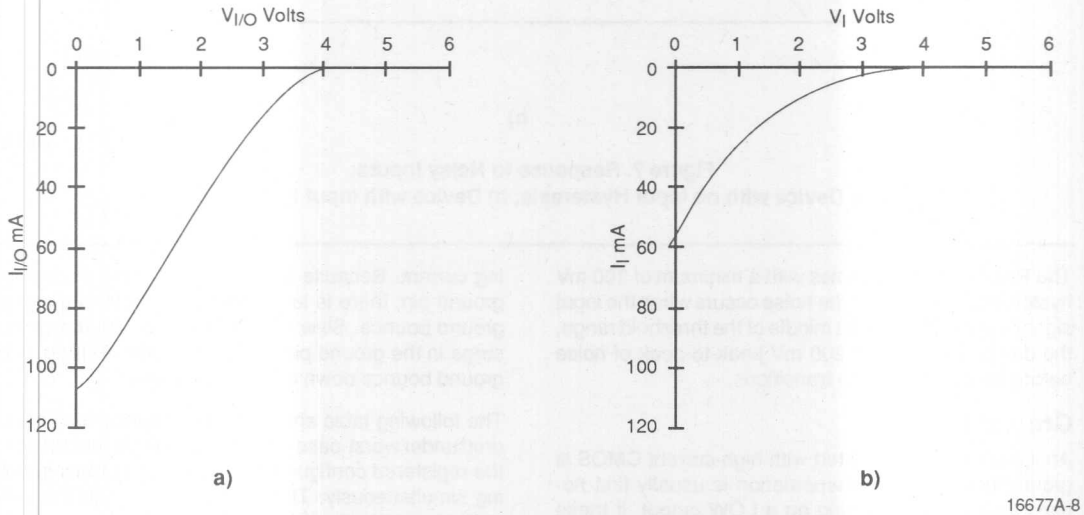
During power shutdown, V_{CC} is either open or shorted to ground. The PALCE16V8HD has n-channel pull-up transistors, which will not conduct or cause latchup when the output signal is higher than V_{CC}.

Hot socketing has two manifestations that concern us here: signal and ground connected before V_{CC}, or signal and V_{CC} connected before ground. If ground and signal lines are connected to the device before V_{CC} is, the effect on the device is similar to that presented by the power-down situation; the device inputs and outputs do not conduct current.

When the ground pin is open with V_{CC} and the inputs or outputs connected, the pull-up transistors conduct. This is because a solid ground is necessary to establish the proper bias voltages to allow the output transistors to turn off. If ground is floating the output transistors are biased on.

Figure 8a shows the I/V curves on an I/O pin with V_{CC} on and ground open. The driver starts to conduct at 4 V and crosses 0 V at –110 mA. It is interesting to note that there is also conduction at the input pins (Figure 8b). The ESD structure is a totem-pole configuration resembling an output driver; therefore, the ESD-protection transistor also conducts when ground floats.

If the ground is disconnected for only a second or two, the device will not be damaged.



16677A-8

Figure 8. I/V Curves when Ground is Disconnected: a) I/O Pin; b) Input

SUMMARY

The PALCE16V8HD incorporates a number of features which make it ideal for applications involving high-current signal lines such as bus control lines.

- There are input latches on every input and I/O pin. The latches allow the earlier capture of data, which effectively shortens the cycle time in many applications. The use of the latch does not add any extra delay. Thus the PALCE16V8HD is faster than the PLD device and external latch combination.
- The PALCE16V8HD macrocell can be programmed as either D-type or T-type flip-flops. The T-type flip-flops can reduce product-term usage in many applications. Larger counters and state-machines can often be built with T-type flip-flops than with D-type flip-flops.
- The output drivers generate fast signals (2-ns to 3-ns rise and fall times). At these edge rates transmission line terminating procedures should be used.
- The drivers can be individually programmed as either totem-pole or open drain. For open-drain outputs, the terminating voltage determines V_{OH}.
- All input pins have a minimum of 200 mV hysteresis. This allows the PALCE16V8HD to operate more robustly in noisy environments such as buses.
- The PALCE16V8HD incorporates slew-rate limiting and multiple grounds. This reduces ground bounce to levels more common in low-power devices.
- The PALCE16V8HD has n-channel pullup transistors. Therefore, it is resistant to latchup caused by signals on input and I/O pins while V_{CC} is off, or by hot-socketing.


IMPORTANT.
NOTES

CHAPTER

6 APPENDICES

Logic Reference Guide 6-3
Signal Polarity 6-25
Glossary 6-30
Worldwide Application Support 6-37


IMPORTANT.
NOTES

INTRODUCTION

Throughout this data book and design guide we have assumed that you have a good working knowledge of logic. Unfortunately, there always comes a time when you are called on to remember something which can only be found in that logic textbook which you threw away years ago.

This section is intended to provide a quick review and reference of the basic principles of digital logic. We will cover three general areas:

- Basic logic elements
- Basic storage elements
- Binary numbers

Throughout the text, we will use the notation that was used throughout this book. If you are unfamiliar with the syntax, you will probably find it easy to understand as you read; if you wish for a more detailed explanation of the symbols, please refer to the Basic Design with PLDs section where they are defined.

As this is a logic reference only, we cannot take on lengthy discussions, nor can we train you in the basic principles of digital logic if you have not previously been trained. In such a case, we must refer you to your favorite logic textbook.

BASIC LOGIC ELEMENTS

In this section, we will discuss the concepts surrounding combinatorial logic functions.

The Three Basic Gates

There are three basic logic gates from which all other combinatorial logic functions can be generated. These functions are *NOT*, *AND*, and *OR*. A truth table indicating these functions is shown in Table 1. Since they can be used to generate any function, they are said to be *functionally complete.*

Table 1. Truth Table for the NOT, AND, and OR Functions

A	B	/A	A*B	A+B
0	0	1	0	0
0	1	1	0	1
1	0	0	0	1
1	1	0	1	1

The standard schematic symbols used to represent these gates are shown in Figure 1.

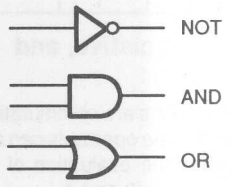
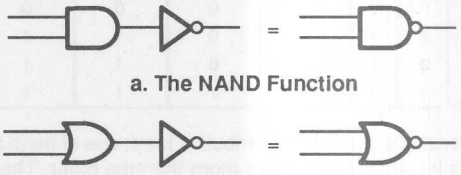


Figure 1. Schematics Symbols for the Three Fundamental Gates

The AND and NOT functions can be combined into the *NAND* function. This is equivalent to an AND gate followed by an inverter, as shown in Figure 2a. Likewise, the OR and NOT gates can be combined into the *NOR* function, as shown in Figure 2b. Each of these gates is functionally complete; any logic function can be expressed solely as a function of NAND or NOR gates.



a. The NAND Function

b. The NOR Function

Figure 2. The NAND and NOR Functions

Precedence of Operators

Logic functions may be created with any combination of the three basic functions. How those functions are expressed affects the evaluation of the function. The normal order of evaluation is:

NOT, AND, OR

Evaluation proceeds in order from left to right.

This order may be altered by inserting parentheses in the function. The contents of the parentheses will always be evaluated before the rest of the expression, from left to right.

Some example functions are evaluated in Table 2.

Table 2. Using Parentheses to Change the Order of Evaluation

A	B	C	D	A*B+/A* C+D	A*B+/A* (C+D)	A*(B+/A)* C+D	A*(B+/A)* (C+D)
0	0	0	0	0	0	0	0
0	1	1	0	1	1	0	0
1	0	0	1	1	0	1	0
1	1	1	1	1	1	1	1

Commutative, Associative, and Distributive Laws

The AND and OR functions are commutative and associative. This means that the operands can appear in any order without affecting the evaluation of the function. This is illustrated in Tables 3 and 4.

Table 3. Commutativity

A	B	A*B	B*A	A+B	B+A
0	0	0	0	0	0
0	1	0	0	1	1
1	0	0	0	1	1
1	1	1	1	1	1

Table 4. Associativity

A	B	C	(A*B)*C	A*(B*C)	(A+B)+C	A+(B+C)
0	0	0	0	0	0	0
0	1	1	0	0	1	1
1	0	1	0	0	1	1
1	1	1	1	1	1	1

There are actually two distributive laws; one of them resembles standard algebra more than the other. These two laws state that:

```
A*(B+C) = (A*B) + (A*C)
A+(B*C) = (A+B) * (A+C)
```

Duality

The two distributive laws give an example of the concept of *duality*. This principle states that:

Any identity will also be true if the following substitutions are made:

* for +
\+ for *
1 for 0
0 for 1

Thus, it is only necessary to prove the first of the distributive laws; the second one will then be true by duality. Note that duality is not required to prove the second law; it can also be proven by truth table or by logic manipulation.

Manipulating Logic

Logic functions may be manipulated by the use of Boolean algebra. The logic functions may be expressed in one of the two canonical forms, or by using a simplified expression.

Canonical Forms

There are two fundamental canonical forms: *sum-of-minterms* and *product-of-maxterms.* The former is by far the most widespread. These are special cases of what are more generally referred to as *sum-of-products* and *product-of-sums* forms. *Minterms* and *maxterms* are products and sums of the variables involved in a function. Each particular combination of noninverted and inverted variables in a product or sum is given a minterm or maxterm number, as shown in Table 5. Within each minterm or maxterm, the individual variables are referred to as *literals.*

For the case of sum-of-minterms form, the expression for a function may be found by ORing the minterms which correspond to the 1's in the function's truth table. Likewise, the product-of-maxterms expression may be found by ANDing the maxterms which correspond to the 0's in the truth table. This is illustrated in Figure 3.

Table 5. Minterms and Maxterms

Table of Minterms for Three Variables

Minterm	Name
/x*/y*/z	m0
/x*/y*z	m1
/x*y*/z	m2
/x*y*z	m3
x*/y*/z	m4
x*/y*z	m5
x*y*/z	m6
x*y*z	m7

Table of Maxterms for Three Variables

Maxterm	Name
x + y + z	M0
x + y +/z	M1
x +/y + z	M2
x +/y + /z	M3
/x + y + z	M4
/x + y + /z	M5
/x + /y + z	M6
/x + /y + /z	M7

Conversion Between Canonical Forms

It is a simple matter to convert between canonical forms. Given a truth table for a function F, there are four different representations that can be used:

- Sum-of-minterms form of F
- Product-of-maxterms form of F
- Sum-of-minterms form of /F
- Product-of-maxterms form of /F

One can convert back and forth between these representations by using the rules shown in Table 6.

A	B	C	D	X	Y	Minterm/ Maxterm Number
0	0	0	0	1	1	0
0	0	0	1	0	1	1
0	0	1	0	1	1	2
0	0	1	1	1	1	3
0	1	0	0	0	1	4
0	1	0	1	1	0	5
0	1	1	0	0	0	6
0	1	1	1	1	1	7
1	0	0	0	1	1	8
1	0	0	1	1	1	9
1	0	1	0	0	0	10
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	0	15

a. Truth Table

```
X = m0+m2+m3+m5+m7+m8+m9
  = Σm (0,2,3,5,7,8,9)

  = /A */B */C */D          ;m0
  + /A */B * C */D          ;m2
  + /A */B * C * D          ;m3
  + /A * B */C * D          ;m5
  + /A * B * C * D          ;m7
  + A */B */C */D           ;m8
  + A */B */C * D           ;m9

Y = m0+m1+m2+m3+m4+m7+m8+m9
  = Σm (0,1,2,3,4,7,8,9)

  = /A */B */C */D          ;m0
  + /A */B */C * D          ;m1
  + /A */B * C */D          ;m2
  + /A */B * C * D          ;m3
  + /A * B */C */D          ;m4
  + /A * B * C * D          ;m7
  + A */B */C */D           ;m8
  + A */B */C * D           ;m9
```

b. The Sum-of-Minterms Expression

```
X = M1*M4*M6*M10*M11*M12*M13*M14*M15
  = ΠM (1,4,6,10,11,12,13,14,15)

  =(A+B+C+/D)               ;M1
  *(A+/B+C+D)               ;M4
  *(A+/B+/C+D)              ;M6
  *(/A+B+/C+D)              ;M10
  *(/A+B+/C+/D)             ;M11
  *(/A+/B+C+D)              ;M12
  *(/A+/B+C+/D)             ;M13
  *(/A+/B+/C+D)             ;M14
  *(/A+/B+/C+/D)            ;M15

Y = M5*M6*M10*M11*M12*M13*M14*M15
  = ΠM (5,6,10,11,12,13,14,15)

  =(A+/B+C+/D)              ;M5
  *(A+/B+/C+D)              ;M6
  *(/A+B+/C+D)              ;M10
  *(/A+B+/C+/D)             ;M11
  *(/A+/B+C+D)              ;M12
  *(/A+/B+C+/D)             ;M13
  *(/A+/B+/C+D)             ;M14
  *(/A+/B+/C+/D)            ;M15
```

c. The Product-of-Maxterms Expression

Figure 3. Finding the Canonical Form from the Truth Table

Table 6. Conversion of Forms Table

Given Form	Desired Form			
	Minterm Expansion of F	Maxterm Expansion of F	Inverted Minterm Expansion of F	Inverted Maxterm Expansion of F
Minterm expansion of F	–	Maxterm numbers are those numbers not in the Minterm list of F	List Minterms not present in F	Maxterm numbers are the same as Minterm numbers of F
Maxterm expansion of F	Minterm numbers are those numbers not on the Maxterm list of F	–	Minterm numbers are the same as Maxterm numbers of F	List Maxterms not present in F

Simplifying Logic

Canonical forms are convenient in that it is easy to derive and convert them. However, the representation is bulky, since all variables must appear in each sum or product. These expressions can be simplified by applying the basic laws and theorems of Boolean algebra.

There are four basic postulates, two of which are the commutative and distributive laws which were discussed above. From these postulates, it is possible to derive nine basic theorems. The postulates and theorems are listed in Table 7.

Table 7. Postulates and Theorems of Boolean Algebra

Postulate 1	(A)	X + FALSE = X
	(B)	X*TRUE = X
Postulate 2	(A)	X + /X = TRUE
	(B)	X * /X = FALSE
Postulate 3	(A)	X + Y = Y + X
	(B)	X*Y = Y*X
Postulate 4	(A)	X * (Y + Z) = (X*Y) + (X*Z)
	(B)	X + (Y*Z) = (X + Y) * (X + X)
Theorem 1	(A)	X + X = X
	(B)	X * X = X
Theorem 2	(A)	X + TRUE = FALSE
	(B)	X*FALSE = FALSE
Theorem 3		/ (/X) = X
Theorem 4	(A)	X + (Y + Z) = (X + Y) + Z
	(B)	X * (Y*Z) = (X*Y) * Z
Theorem 5	(A)	/ (X + Y) = /X * /Y
	(B)	/ (X * Y) = /X + /Y
Theorem 6	(A)	X + (X * Y) = X
	(B)	X * (X + Y) = X
Theorem 7	(A)	(X*Y) + (X*/Y) = X
	(B)	(X + Y) * (X + /Y) = X
Theorem 8	(A)	X + (/X*Y) = X + Y
	(B)	X * (/X + Y) X*Y
Theorem 9	(A)	(X*Y) + (/X*Z) + (Y*Z) = (X*Y) + (/X*Z)
	(B)	(X + Y) * (/X + Z) * (Y + Z) = (X + Y)*(/X + Z)

Notice that each theorem and postulate (with the exception of theorem 3) has two forms. This is a result of the duality principle; once one form of a theorem is established, the dual representation follows immediately. Theorem 3 has no dual because it does not involve any of the elements that have duals (+, *, 1, or 0).

As the logic expression is simplified, it no longer contains minterms (or maxterms), since some of the minterms and literals are being eliminated. What was a sum-of-minterms (product of maxterms) representation is now simplified to a sum-of-products (product of sums).

DeMorgan's Theorem

Once an expression has been simplified, it is no longer possible to invert the function by using Table 6. Inverting simplified logic requires DeMorgan's theorem:

```
/(X*Y) = /X + /Y
/(X + Y) = /X*/Y
```

This is theorem 5 in Table 7.

There is one shortcut which can be used. The effect of inversion can be accomplished by inverting all literals and then using the dual representation. For example, given the expression

```
/(A*/B + A*C + /A*B*D)
```

we can invert to obtain:

```
/A*B + /A*/C + A*/B*/D   ;step one,
                         invert
                         literals

(/A + B)*(/A + /C)*      ;step two,
(A + /B + /D)            take dual
```

This expression must still be simplified to obtain a sum-of-products representation, but this shortcut eliminates some of the early steps.

Karnaugh Maps: Minimizing Logic

Simplifying by hand by using algebraic manipulation can be a tedious and error-prone procedure. When only a few variables are used (generally less than 5 or 6), Karnaugh maps (also called K-maps) provide a simpler graphical means of simplifying logic. K-maps not only allow for logic simplification, but for logic minimization, where an expression has a minimal number of product terms (or sum terms) and literals.

A Karnaugh map consists of a box which has one cell for each minterm. These cells are arranged so that only one literal is inverted when moving from one cell to an adjacent cell. The headings placed by each row and column indicate the polarities of the literals for that row or column. The literals themselves are indicated in the top left corner of the map. An example of a Karnaugh map for three variables is shown in Figure 4.

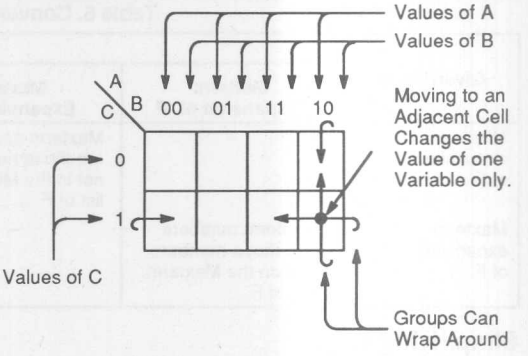


Figure 4. A Karnaugh Map for Three Variables

The truth table for a function is then transferred to the K-map by placing the 1's and 0's in the appropriate cells.

Since each cell differs from its neighbor only in the polarity of one of the literals, 1's in adjacent cells can be combined by theorem 7a, which says that

```
x*y + x*/y = x
```

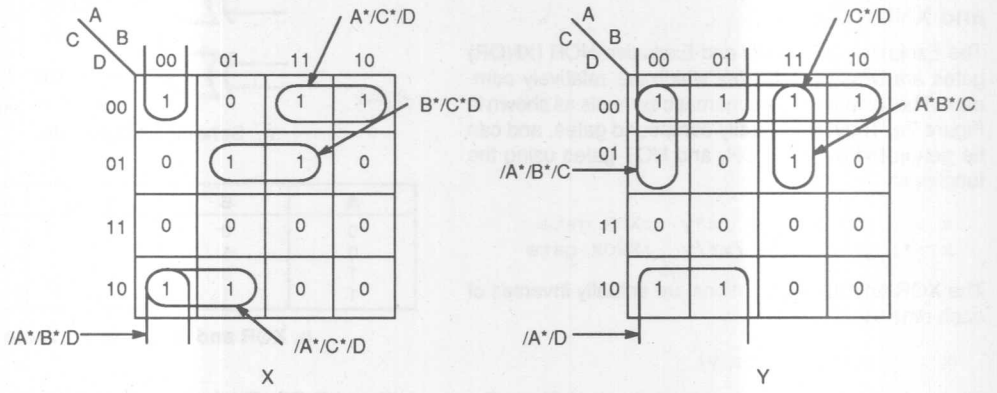
In this manner, two product terms are combined into one. This procedure can conceptually be repeated to allow groupings of two, four, eight, or any group of adjacent cells whose size is a power of two. A cell may appear in more than one group. Just enough groups are found to include all of the 1's. The groups should be as large as possible.

This process provides a minimal sum of products. The product-of-sums form can be obtained by grouping 0's instead of 1's and inverting the header for each cell.

The two functions from Figure 3 have been placed into K-maps in Figure 5. The groups are then used as individual product terms. When reading the product terms from the map, the only literals which will appear in the product term are the ones whose values are constant for each cell in the group. If that value is 1, then the non-inverted form of the literal is used. If the value is 0, then the inverted form of the literal is used.

For active-LOW functions, the same procedure is used, except that the 0's are grouped instead of the 1's. The active-LOW version of the functions from Figure 3 are derived in Figure 6.

Hand simplification and minimization is not needed as frequently today as in the past, since software is now available for handling these logic manipulations. Most software can perform logic simplification and minimization automatically.

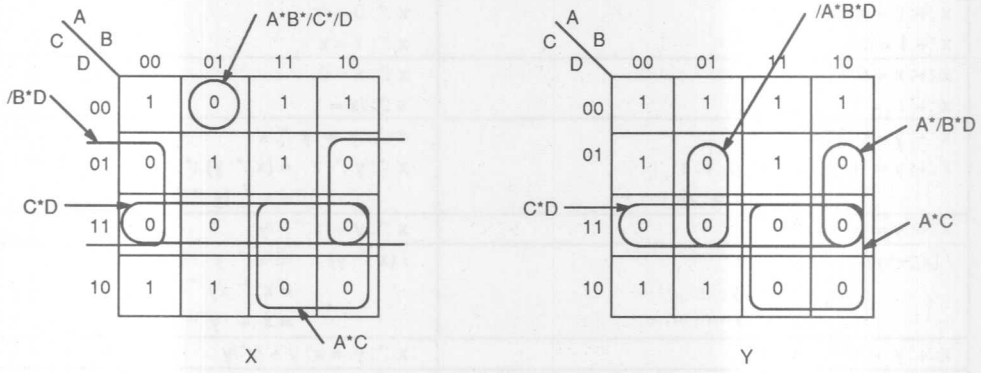


X = /A*/B*/D
+ A*/C*/D
+ B*/C*D
+ /A*C*/D

Y = /A*/D
+ /C*/D
+ /A*/B*/C
+ A*B*/C

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Figure 5. Using a K-map to Minimize the Functions in Figure 3



/X = C*D
+ /B*D
+ A*C
+ /A*B*/C*/D

/Y = C*D
+ A*D
+ /A*B*D
+ A*/B*D

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Figure 6. Finding Inverse Functions

Comparison and Equivalence: the XOR and XNOR Gates

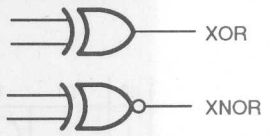
The Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates are two special gates which are relatively common. These gates have schematic symbols as shown in Figure 7a. They are actually compound gates, and can be generated by AND, OR, and NOT gates using the functions:

```
x :+: y = x*/y + /x*y   ;XOR gate
x :*: y = x*y + /x*/y   ;XNOR gate
```

The XOR and XNOR functions are actually inverses of each other; that is,

```
x :+: y = /(x :*: y)
```

The truth tables for these gates are shown in Figure 7b. Note that the XOR function is true if and only if the operands are different. For this reason, it is useful as a comparator. The XNOR function is true if and only if its operands are the same; therefore it is used as an equivalence indicator.



10173D-

a. Schematic Symbols

A	B	A:+:B	A:*:B
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

b. XOR and XNOR Truth Table

Figure 7. The Exclusive-OR and Exclusive-NOR Functions

Some basic properties of the XOR and XNOR functions are listed in Table 8.

Table 8. Properties of the XOR and XNOR Functions

XOR	XNOR
x :+: 0 = x x :+: 1 = /x	x :*: 0 = /x x :*: 1 = x
x :+: x = 0 x :+: /x = 1	x :*: x = 0 x :*: /x = 1
x :+: y = y :+: x x :+: y = :+: z = (x :+: y) :+: z = x :+: (y :+: z)	x :*: y = y :*: x x :*: y :*: z = (x :*: y) :*: z) = x :*: (y :*: z)
x :+: y = /x :+: /y	x :*: y = /x :*: /y
/(x :+: y) = /x :+: y = x :+: /y = x :+: y	/(x :*: y) = /x :*: y = x :*: /y = x :+: y
x :+: y = x* /y + /x*y	x :*: y = x* y + /x*/y
x :+: x* y = x*/y x :+: /x*y = x + y	x :*: x* y = /x + y x :*: /x*y = /x * /y
x* (y :+: z) = (x*y) :+: (x*z) /x*(y :+: z) = (x + y) :+: (x + z)	x + (y :*: z) = (x + y) :*: (x + z) /x + (y :*: z) = (x*y) :*: (x*z)

When deriving equations from a Karnaugh map, XOR and XNOR functions can usually be identified by their characteristic pattern. Exactly what the operands are may or may not be obvious for more complicated functions. Some examples are shown in Figure 8.

The XOR gate can be used as an "UNLESS" operator. In other words, the function, A = X :+: Y can be interpreted as:

"A will have the same value as X UNLESS Y is true."

This can be helpful when trying to derive a logic equation for a function which can be described in words.

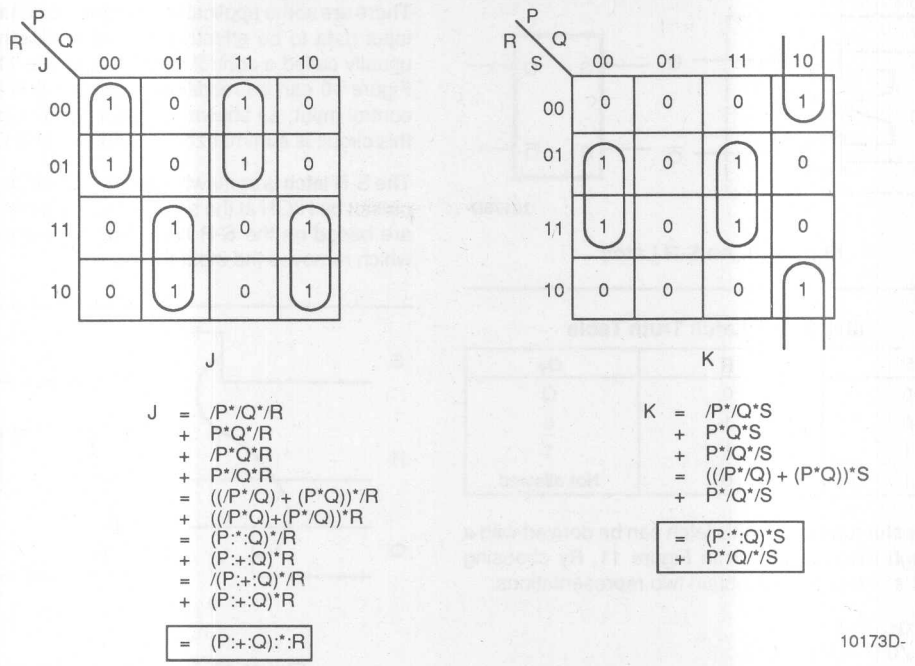


Figure 8. Finding XOR and XNOR Functions in Karnaugh Maps

Basic Storage Elements

Storage elements provide circuits with the capability of remembering past conditions or events. The prototypical storage element is just a pair of cross-coupled NAND gates, as shown in Figure 9. These elements are normally called *flip-flops*.

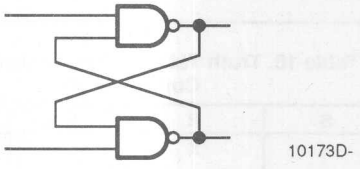


Figure 9. Basic Storage Element

In general, there are two primary classes of flip-flops:

- *Unclocked* flip-flops, or *latches*
- *Clocked* flip-flops

Clocked flip-flops are sometimes referred to as *registers*, although technically speaking, a register is a bank of several flip-flops with a common clock signal.

Flip-flops can also be characterized by their control scheme. There are four types of flip-flops, each of which can be unclocked or clocked:

- S-R
- J-K
- D
- T

The discussion below will be divided between unclocked and clocked flip-flops. Each of the four flip-flop types will be treated for each section.

Unclocked Flip-Flops—Latches

S-R Latches

An S-R latch can be built out of NOR gates as shown in Figure 10, and behaves according to the truth table in Table 9. 'S' stands for 'set' and 'R' stands for 'reset,' as suggested by the truth table.

Note that the latch actually has two outputs, which are complementary. These are referred to as Q and $\overline{Q}$. If both S and R are raised at the same time, then both Q and $\overline{Q}$ will be HIGH; although this is physically possible, it does not make sense if Q and $\overline{Q}$ are to be complementary signals. Thus, this condition is not allowed.

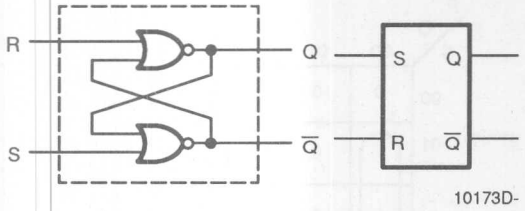


Figure 10. An S-R Latch

Table 9. S-R Latch Truth Table

S	R	Q+
0	0	Q
0	1	0
1	0	1
1	0	Not allowed

The transfer function for this latch can be derived with a Karnaugh map, as shown in Figure 11. By choosing either 1's or 0's, we can obtain two representations:

a. Q+ = S+/R*Q
b. /Q+ = R+/S*/Q

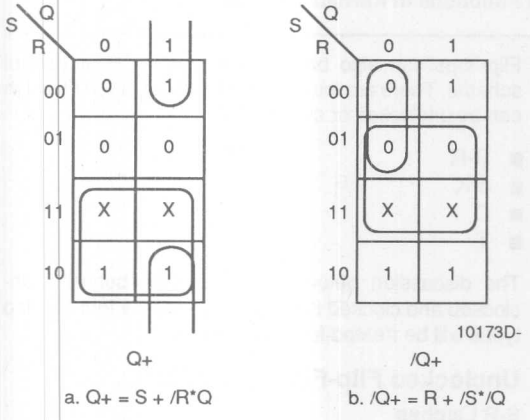


Figure 11. Karnaugh Map for an S-R Latch

Waveforms illustrating the operation of the S-R latch are shown in Figure 12.

There are some applications where it is desirable for the input data to be effective only when another signal—usually called a control signal—is active. The circuit of Figure 10 can be modified to give an S-R latch with a control input, as shown in Figure 13. The operation of this circuit is summarized in Table 10 and Figure 14.

The S-R latch is somewhat restrictive, since both inputs cannot be HIGH at the same time. The other latch types are based on the S-R latch, but have additional logic which removes the input restrictions.

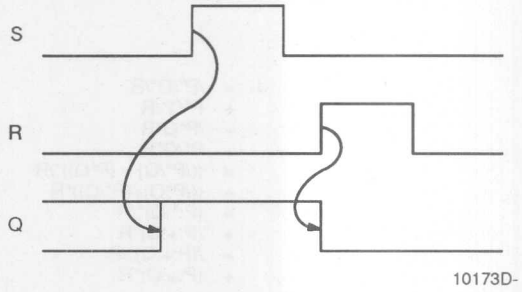


Figure 12. S-R Latch Behavior

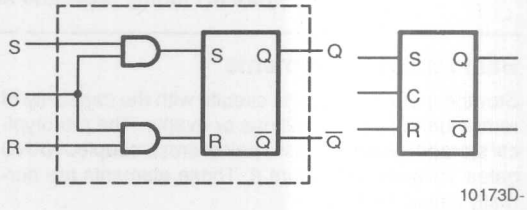


Figure 13. Adding a Control Input to an S-R Latch

Table 10. Truth Table for an S-R Latch with a Control Input

S	R	C	Q+
X	X	0	Q
0	0	1	Q
0	1	1	0
1	0	1	1
1	1	1	Not allowed

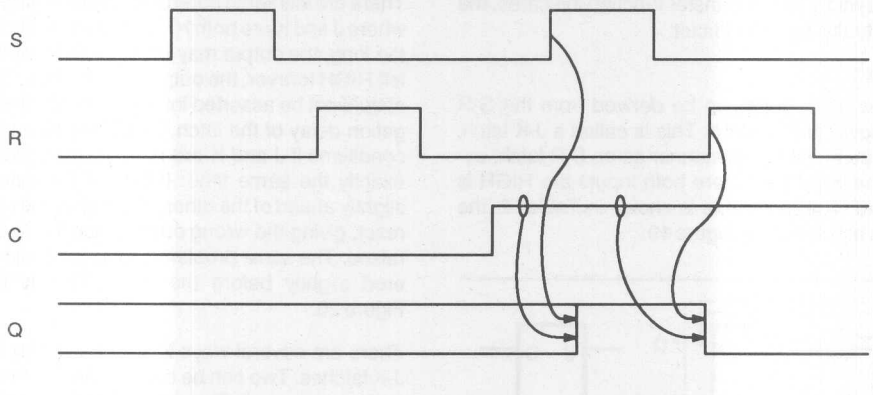


Figure 14. Behavior of an S-R Latch with a Control Input

D-Type Latches (Transparent Latches)

A single-input latch can be formed by adding some logic to the controlled S-R latch in Figure 13; this gives rise to the D-type latch in Figure 15. This latch is often called a *transparent* latch, since data on the input passes right through to the output as long as the control input is HIGH. If the control input is set LOW, then the latch holds whatever data was present when the control went LOW. With this type of latch, the control is usually called a *gate*.

The behavior of the D-type latch is shown in Table 11 and Figure 16.

The basic transfer function for a D-type latch can be derived from the Karnaugh map in Figure 17.

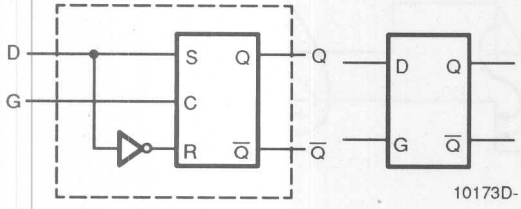


Figure 15. A D-Type (Transparent) Latch

Table 11. Truth Table for a D-Type Latch

D	G	Q+
X	0	Q
0	1	0
1	1	1

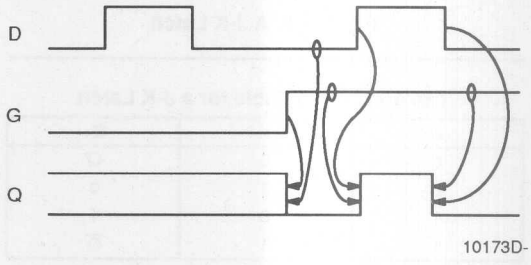
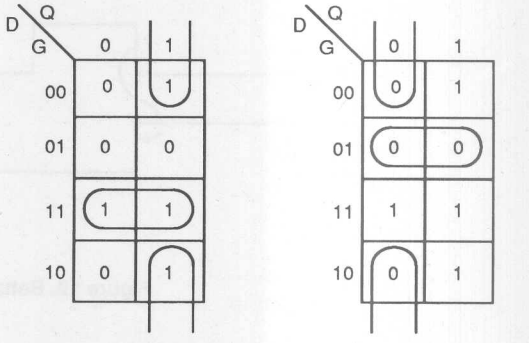


Figure 16. D-Type (Transparent) Latch Behavior

Q+ = D*G + Q*/G

/Q+ = /D*G + /Q*/G



a. Q+ = D*G + D*/G

b. /Q+ = /D*G + /Q*/G

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Figure 17. Karnaugh Maps for a D-Type Latch

If realized exactly as the transfer function indicates, the result is actually a glitchy circuit.

J-K Latches

Another two-input latch can be derived from the S-R latch as shown in Figure 18. This is called a J-K latch, and operates in the same manner as an S-R latch, except that the condition where both inputs are HIGH is now allowed. The truth table is shown in Table 12; the waveforms are shown in Figure 19.

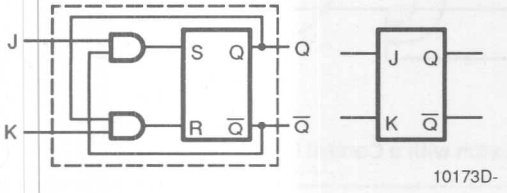


Figure 18. A J-K Latch

Table 12. Truth Table for a J-K Latch

J	K	Q+
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

There are still some potential problems here for the case where J and K are both HIGH. If J and K are left HIGH for too long, the output may change more than one time; if left HIGH forever, the output will oscillate. Thus, J and K should not be asserted for a time longer than the propagation delay of the latch. There are also potential race conditions if J and K are not asserted and removed at exactly the same time. If one of the inputs is raised slightly ahead of the other, it may give the output time to react, giving the wrong output once the second input is raised. The same problem can occur if one input is lowered slightly before the other. This is illustrated in Figure 20.

There are several ways to derive transfer functions for J-K latches. Two can be derived directly from Karnaugh maps, as shown in Figure 21; the others are not as obvious, and make use of the XOR gate described before. The basic transfer functions are listed in Table 13.

Table 13. Transfer Functions for a J-K Latch

Q+ = J * /Q + /K*Q	/Q+ = /J* /Q + K*Q
Q+ = Q :+: (J* /Q + K*Q)	/Q+ = /Q :+: (J*/Q + K*Q)
Q+ = /Q :+: (/J*/Q + /K*Q)	/Q+ = Q :+: (/J*/Q + /K*Q)

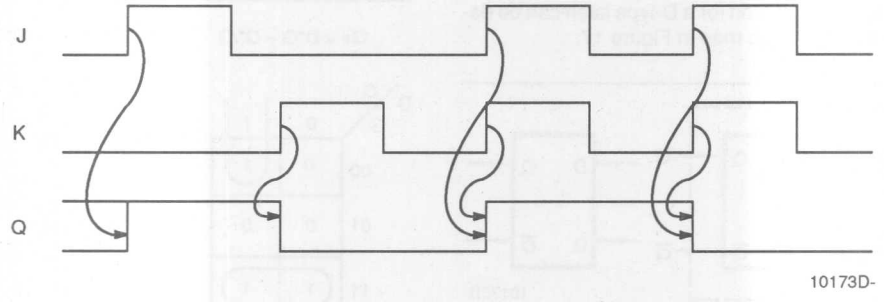


Figure 19. Behavior of a J-K Latch

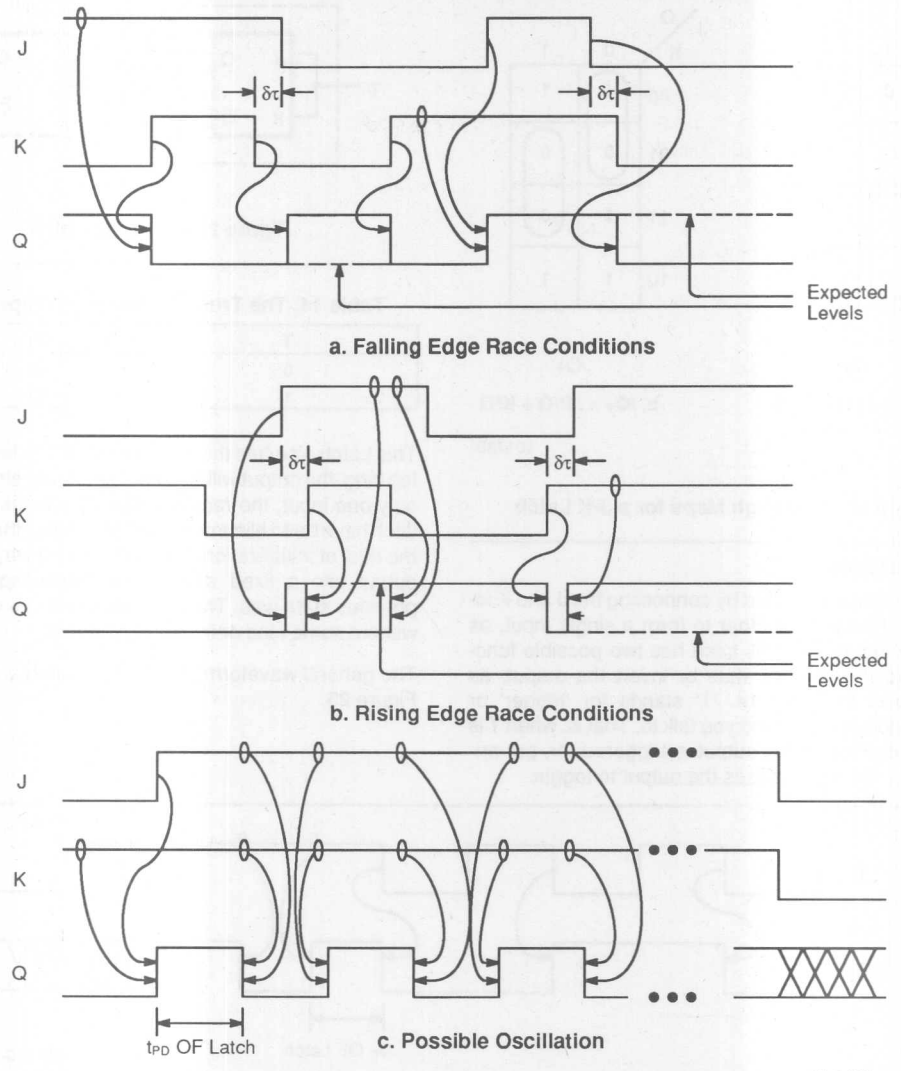
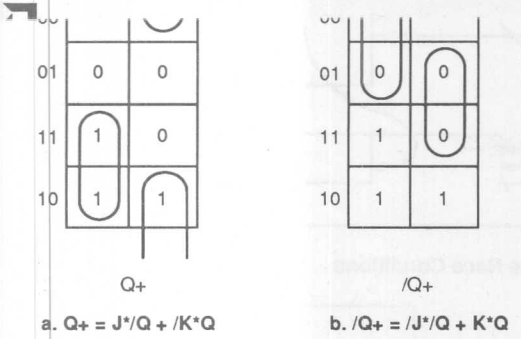


Figure 20. Hazards Inherent in a J-K Latch



a. Q+ = J*/Q + /K*Q

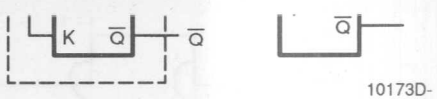
b. /Q+ = /J*/Q + K*Q

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Figure 21. Karnaugh Maps for a J-K Latch

T-Type Latches

T-type latches are formed by connecting the J and K inputs of a J-K latch together to form a single input, as shown in Figure 22. This latch has two possible functions: hold the present state or invert the output, as summarized in Table 14. 'T' stands for 'trigger' or 'toggle' depending on who you talk to. That is, when T is HIGH, a change at the output is triggered; or, put another way, raising T causes the output to toggle.



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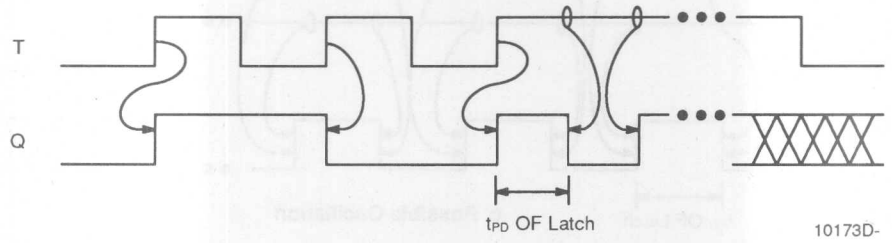
Figure 22. A T-Type Latch

Table 14. The Truth Table for a T-Type Latch

T	Q+
0	Q
1	/Q

This Latch also has the problem that if T is left HIGH for too long, the output will oscillate. However, since there is only one input, the race condition problems of the J-K latch have been eliminated. Unfortunately, this comes at the cost of initialization. There is now no way to get the output into a fixed state without knowing what the previous state was. Thus, this device is not very useful without some kind of initialization circuit.

The general waveforms for a T-type latch are shown in Figure 23.



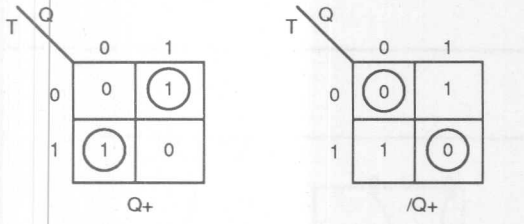
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Figure 23. Behavior of a T-Type Latch

From the Karnaugh map in Figure 24, we can generate the following transfer functions:

```
Q+ = T*/Q          /Q+ = T*Q
   + /T*Q               + /T*/Q

Q+ = Q:+:T         /Q+ = /Q :+: T
Q+ = /Q:+: /T      /Q+ = Q :+: /T
```



a. Q+ = T*/Q + /T*Q

b. /Q+ = T*Q + /T*/Q

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Figure 24. Karnaugh Maps for a T-Type Latch

Clocked Flip-Flops

Latches can be modified by adding a *clock* input. The purpose of the clock is to delay any output changes until the clock signal changes. Whereas latch control inputs (such as the gate) are *level-sensitive,* clock inputs are generally *edge-sensitive (*or *edge-triggered),* meaning that output transitions can occur only when a clock transition is detected. A device is classified as positive edge-triggered or negative edge-triggered, depending on whether it responds to the rising or falling edge of the clock signal, respectively. The behavior to a clocked S-R flip-flop is illustrated in Figure 25.

The clock provides two basic advantages. It removes the hazards inherent in the J-K and T flip-flops, since all inputs will have settled by the time the clock edge arrives, and only one transition is possible for each clock edge. The clock also allows the design of synchronous systems, where all signals are coordinated with other signals. The entire system is then regulated by the clock.

The basic behavior of the four flip-flops types does not change with the addition of a clock; the output changes are merely made to wait for the clock edge. Thus, the basic transfer equations for most of the flip-flops are the same. We can indicate the clocked nature of the flip-flops by using the "registered" assignment ':=' instead of '='.

D-Type Flip-Flops

This is the only flip-flop type whose basic transfer characteristic changes, because the clock input replaces the gate input. Thus the transfer equations become:

```
Q+:= D/Q+ := /D
```

That is, whatever data appears on the input will be transferred to the output after the next clock edge. The input is not changed in any way.

The simplicity of this flip-flop makes it the most widely used flip-flop. However, functions are sometimes more conveniently expressed using J-K flip-flops, or using T-type flip-flops. If we replace the D signal with the transfer function for one of the other flip-flop types, we can then emulate that flip-flop type in the D-type flip-flop. This is equivalent to taking a latch and placing a clocked D-type flip-flop after the latch output for synchronization. Figure 26 illustrates how each flip-flop can be emulated in a D-type flip-flop. The standard schematic symbols for the flip-flop types are also shown.

Table 15 summarizes the transfer functions for all of the flip-flop types. These functions can directly be used to emulate a particular flip-flop type in a D-type flip-flop. This can be particularly useful since D-type flip-flops are available in most registered PLDs.

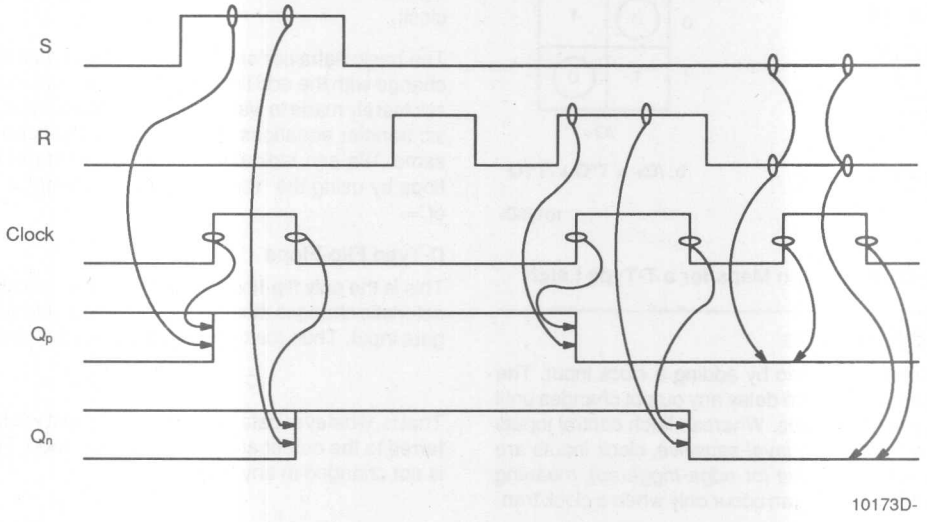


Figure 25. Behavior of a Clocked S-R Flip-Flop for Positive (Qp) and Negative (Qn) Edge-Triggered S-R Flip-Flops

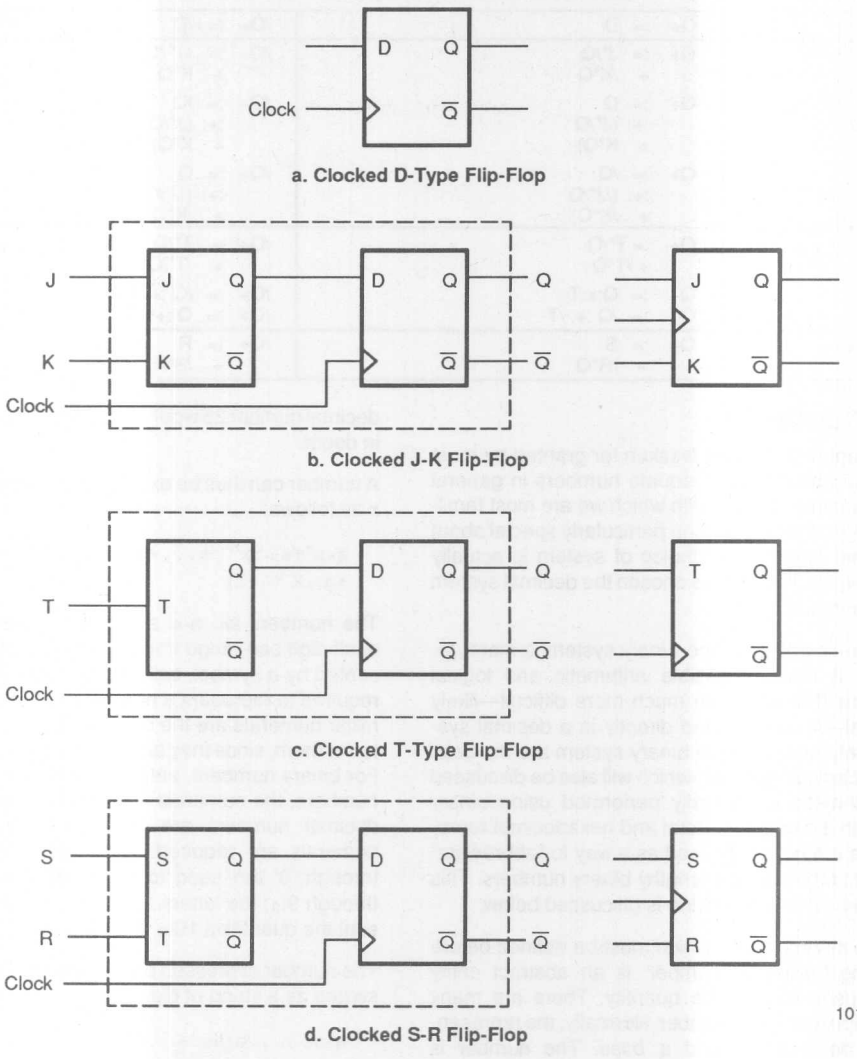


Figure 26. Clocked Flip-Flops. All can be Emulated with a D-Type Flip-Flop

Table 15. Clocked Flip-Flop Transfer Functions

D-Type	Q+ := D	/Q+ := /D
J-K-Type	Q+ := J*/Q + /K*Q Q+ := Q :+: (J*/Q + K*Q) Q+ := /Q :+: (/J*/Q + /K*Q)	/Q+ := /J* /Q + K*Q /Q+ := /Q :+: (J*/Q + K*Q) /Q+ := Q :+: (/J*/Q + /K*Q)
T-Type	Q+ := T*/Q + /T*Q Q+ := Q:+:T Q+ := /Q :+: /T	/Q+: = T*/Q + /T*/Q /Q+ := /Q :+: T /Q+ := Q :+: /T
S-R-Type	Q+ := S + /R*Q	/Q+ := R + /S*/Q

Binary Numbers

The concept of *a number is* taken for granted by most people. And most people equate numbers in general with the *decimal* system, with which we are most familiar. However, there is nothing particularly special about the decimal system; the choice of system is actually rather arbitrary. History has chosen the decimal system for most humans.

For electronic systems, the *binary* system is more appropriate. It makes possible arithmetic and logical calculations that would be much more difficult—likely impractical—if implemented directly in a decimal system. Closely related to the binary system are the *octal* and *hexadecimal* systems, which will also be discussed here. Arithmetic is normally performed using binary numbers in a computer. Octal and hexadecimal representations are generally used as a way to "abbreviate" what might otherwise be lengthy binary numbers. This will be seen when conversion is discussed below.

There are several terms which must be defined before proceeding further. A *number* is an abstract entity which is used to describe quantity. There are many ways of representing a number. Normally, the representation is designed around a *base*. The number is expressed as a sum of multiples of the powers of the base. The decimal system is a base-10 system, meaning that 10 is used as the base. The binary system is base-2; the octal system is base-8; and the hexadecimal system is base-16. The binary, octal, and hexadecimal systems are closely related because 8 and 16 are both powers of 2. When different bases are being used, a number will often be followed by its base in subscript, to indicate exactly what the base is. For example, the decimal number 25 would be written 25_{10} if its base were in doubt.

A number can thus be expressed in terms of some base x as follows:

$$a_n x^n + a_{n-1} x^{n-1} + \ldots + a_1 x^1 + a_0 x^0 + a_{-1} x^{-1} + \ldots + a_{-m} X^{-m} \quad (1)$$

The numbers $a_n \ldots a_{-m}$ are called *digits*. The value of each digit can range from 0 to x–1. Each digit is represented by a symbol, called a *numeral*. X numerals are required to represent a number in base x. The most familiar numerals are the symbols '0,' '1,'...'9.' There are ten of them, since they are used for the decimal system. For binary numbers, only '0' and '1' are used; for octal numbers, the numerals '0' through '7' are used. Hexadecimal numbers are more difficult, since sixteen numerals are required. Therefore, the numerals '0' through '9' are used to represent the quantities 0_{10} through 9_{10}; the letters A through F are used to represent the quantities 10_{10} through 15_{10}.

The number expressed by equation 1 is normally represented as a string of digits:

$$a_n a_{n-1} \ldots a_1 a_0 . a_{-1} \ldots a_{-m}$$

The digits representing negative powers of the base are separated from those representing non-negative powers by *a point*. In the decimal system, this is referred to as a *decimal point;* in the binary system, it is referred to as a *binary point*.

There are two basic classes of manipulation which will be discussed: conversions between bases and arithmetic within a base.

Converting Between Bases

Base-2 <–> Base-10

Converting a binary number to a decimal number is accomplished by using equation 1 directly.

Example:

Converting 110100.011_2 to decimal:

$$\begin{aligned} Y &= 110100.011 \\ &= 1\bullet2^5 + 1\bullet2^4 + 0\bullet2^3 + 1\bullet2^2 + 0\bullet2^1 + 0\bullet2^0 + 0\bullet2^{-1} + \\ &\quad 1\bullet2^{-2} + 1\bullet2^{-3} \\ &= 32 + 16 + 4 + .25 + .125 \\ &= 52.375 \end{aligned}$$

When converting whole numbers from decimal to binary, the decimal number is repeatedly divided by 2. Integer division is used, so the quotients are "rounded down" to the next integer. The remainders form the digits of the number. The least significant digit is the first one calculated.

Example:

Converting 61_{10} to binary:

61/2 = 30	remainder = 1	LSB
30/2 = 15	remainder = 0	
15/2 = 7	remainder = 1	
7/2 = 3	remainder = 1	
3/2 = 1	remainder = 1	
1/2 = 0	remainder = 1	MSB

$61_{10} = 111101_2$

When converting a decimal fraction into a binary fraction, the decimal number is multiplied by 2. This results in a whole number and a fraction. The whole number is a digit; the procedure is repeated on the new fraction. This procedure is repeated until the fractional portion is zero. If the procedure does not terminate, then the result is a repeating fraction. The first digit calculated is the most significant digit.

Example:

Converting $.1625_{10}$ to binary:

0.1625•2 = 0.3250	whole portion = 0	MSB
0.3250•2 = 0.65	whole portion = 0	
0.65•2 = 1.3	whole portion = 1	
0.3•2 = 0.6	whole portion = 0	
0.6•2 = 1.2	whole portion = 1	
0.2•2 = 0.4	whole portion = 0	
0.4•2 = 0.8	whole portion = 0	
0.8•2 = 1.6	whole portion = 1	
0.6•2 = 1.2	whole portion = 1	

Here we see that the fraction will repeat, since we have already multiplied 0.6 earlier. Thus

$0.1625_{10} = 0.00101001100110011..._2$

For mixed numbers, it is necessary to calculate the whole and fractional portions separately. Thus, for example, we know that

$61.1625_{10} = 111101.0010100110011..._2$

These are actually general procedures which can be used to convert a decimal number into any base, and vice versa.

Examples:

1. Converting 321.54_8 to decimal:

$$\begin{aligned} Y &= 3\bullet8^2 + 2\bullet8^1 + 1\bullet8^0 + 5\bullet8^{-1} + 4\bullet8^{-2} \\ &= 192 + 16 + 1 + .625 + .0625 \\ &= 209.6875 \end{aligned}$$

$321.54_8 = 209.6875_{10}$

2. Converting 106.10375_{10} to octal:

106/8 = 13	remainder = 2	LSB
13/8 = 1	remainder = 5	
1/8 = 0	remainder = 1	MSB

Thus, the whole portion is 151_8.

0.10375•8 = 0.83	whole portion = 0	MSB
0.83•8 = 6.64	whole portion = 6	
0.64•8 = 5.12	whole portion = 5	
0.12•8 = 0.96	whole portion = 0	
0.96•8 = 7.68	whole portion = 7	
0.68•8 = 5.44	whole portion = 5	

At this point we have enough significant digits. We could continue either until the procedure terminated, or until the pattern started repeating. However, those last digits are not likely to be significant. Thus, we can approximate by saying that...

$106.10375_{10} = 152.065075_8$

3. Converting $31F.A2_{16}$ to decimal:

$$\begin{aligned} Y &= 31F.A2_{16} \\ &= 3\bullet16^2 + 1\bullet16^1 + 15\bullet16^0 + 10\bullet16^{-1} + 2\bullet16^{-2} \\ &= 768 + 16 + 15 + 0.625 + 0.0078125 \\ &= 799.6328125 \end{aligned}$$

$31F.A2_{16} = 799.6328125_{10}$

4. Converting 7689.100854_{10} to hexadecimal:

7689/16 = 480	remainder = 9	LSB
480/16 = 30	remainder = 0	
30/16 = 1	remainder = E	
1/16 = 0	remainder = 1	MSB

0.618624•16 = 13.097984 whole portion = D
0.097984•16 = 1.567744 whole portion = 1
0.567744•16 = 9.083904 whole portion = 9
0.083904•16 = 1.342464 whole portion = 1

Again, we likely have enough digits at this point. The exact fraction could be either very long or a long repeating pattern. For our purposes, we can approximate the overall result as:

$7689.100854_{10} = 1E09.19D191_{16}$

Binary <–> Octal, Hexadecimal

Converting between the binary-related systems is very easy. The procedure consists of dividing the binary digits into groups, and replacing each group with an appropriate digit. For this reason, octal and hexadecimal numbers are often used to shorten long binary numbers.

To convert from binary to octal, group the digits by three, starting on each side of the binary point, and then convert each group of three digits into its corresponding octal digit. Leading and trailing zeroes may have to be added to the left of the whole portion and the right of the fractional portion, respectively, to make complete groups of three binary digits.

Example:

Converting $1011010110101.001001101_2$ to octal:

Divide into groups of three digits:

011	011	010	110	101	.	001	001	101
3	3	2	6	5	.	1	1	5

Thus $1011010110101.001001101_2 = 33265.115_8$

To convert from binary to hexadecimal, the digits are divided into groups of four digits, and then given their corresponding hexadecimal digits. Again, leading and/or trailing zeroes may be needed.

Example:

Converting $100101011101100.110110001_2$ to hexadecimal:

Divide into groups of four digits:

0100	1010	1110	1100	.	1101	1000	1000
4	A	E	C	.	D	8	8

Thus $100101011101100.110110001_2 = 4AEC.D88_{16}$

To convert from octal or hexadecimal to binary, merely expand each digit into its corresponding binary representation.

7	3	2	4	.	3	4
111	011	010	100	.	011	100

Thus $7324.34_8 = 111011010100.0111_2$

2. Convert $1A2.3F5_{16}$ to binary:

1	A	2	.	3	F	5
0001	1010	0010	.	0011	1111	0101

Thus $1A2.3F5_{16} = 110100010.001111110101_2$

Binary Arithmetic

Positive binary arithmetic is very simple, and completely analogous to decimal arithmetic. However, if we are restricted to positive numbers, then we are also restricted to addition. We need a means of representing negative numbers. Using a dash '–' is unacceptable for representation in a computer. There are two general schemes which can be used. In binary systems, they are referred to as *1s complement* and *2s complement* representation, although they can be generalized for any base system as *diminished-radix complement* and *radix complement* representation.

One's Complement Representation

The one's complement of a binary number can be calculated by inverting all of the bits of the number. Fractions are handled exactly the same way, although this is convenient only for fixed-point arithmetic. Floating-point arithmetic requires other methods, which will not be discussed here.

Example:

Finding the one's complement of 110111.0101:

110111.0101
001000.1010 (Inverting each bit)

Thus, the one's complement of 110111.0101 is 001000.1010.

The sign of a number is determined by the most significant bit. If the MSB is 0 the number is positive; if the MSB is 1, then the number is negative. Zero is represented by all bits being zero. However, one normally thinks of zero as being its own complement. But if we take the one's complement of zero,

0000
1111

we see that 1111 is another representation of zero. Thus, in an eight-bit representation, positive numbers range from 00000001 to 01111111; negative numbers range from 10000000 to 11111110. Note that there are just as many negative numbers as positive numbers.

This eight-bit code allows us to represent the numbers from –127 to +127.

When performing addition with one's complement numbers, it is important to watch for overflow results. Whenever an overflow occurs, a correction must be made by adding 1 to the result.

In some cases, the results of an operation will not be meaningful, since the intended result cannot be represented. For instance, in the eight-bit system above, adding 127 to 127 will give a meaningless result, since 254 cannot be represented in this system. Thus, the operation must be evaluated to ensure that the result is meaningful.

Examples:

All examples will use 4-bit systems. Thus, the range of representable numbers is from –7 to +7.

Add 3 + 2:

0011	3	
+ 0010	+ 2	
0101	5	result meaningful

Add 7 + 7 (14 cannot be represented):

0111	7	
+ 0111	+ 7	
1110	–1	result meaningless

Subtract 3 from 7:

0111	7	
+ 1100	+ –3	
10011		overflow – add 1, discard overflow bit
+1		
0100	4	

Subtract 5 from 2:

0010	2	
+ 1010	+ –5	
1100	–3	result meaningful

Subtract 6 from –5 (–11 cannot be represented):

1010	–5	
+ 1001	+ –6	
10011		overflow – add 1, discard overflow bit
+1		
0100	4	result meaningless

Subtract 5.25 from 3.5 (fixed point; requires 6 bits):

0011.10	3.5	
+ 1010.10	+ –5.25	
1110.00	–1.75	result meaningful

Subtract 7 from 7:

0111	7	
+ 1000	+ –7	
1111	0	one of the representations of 0

The advantage of one's complement code is the fact that it is easy to compute the complement. However, the fact that there are two representations for zero is a problem. In addition, the results of subtraction frequently have to be adjusted for overflow by adding 1.

Two's Complement Representation

The two's complement of a binary number is more difficult to calculate. It is generated by taking the one's complement, and then adding 1. Any overflow is discarded. Fractions are again handled in the same way, although 1 is added to the least significant bit.

Example:

Finding the two's complement of 110111.0101:

```
  110111.0101
  001000.1010      (take one's
+        +1        complement)
-----------
  001000.1011
```

Thus, the two's complement of 110111.0101 is 001000.1011.

The sign of a number is again determined by the most significant bit. If the MSB is 0 the number is positive; if the MSB is 1, then the number is negative. Zero is represented by all bits being zero. In this case, if we take the two's complement of zero, we get:

```
  0000
  1111
+  +1
------  (overflow is discarded)
  0000
```

giving only one representation for zero.

Thus, in an eight-bit representation, positive numbers range from 00000001 to 01111111; negative numbers range from 10000000 to 11111111. This means that there is one more negative number than there are positive numbers. So this eight-bit code allows us to represent the numbers from –128 to +127.

Addition is handled in the same fashion as with one's complement code, except that when an overflow occurs, the overflow bit is disregarded. No correction must be made to the results.

After any operation, one must still make sure that the results are meaningful.

Examples:

Add 3 + 2:

```
   0011      3
+  0010   +  2
------    ---
   0101      5    result meaningful
```

Add 7 + 7 (14 cannot be represented):

```
   0111      7
+  0111   +  7
------    ---
   1110     –2    result meaningless
```

Subtract 3 from 7:

```
   0111      7
+  1101   +  –3
------    ---
  10100      4    overflow – discard
                  overflow bit
```

Subtract 5 from 2:

```
   0010      2
+  1011   +  –5
------    ---
   1101     –3    result meaningful
```

Subtract 6 from –5 (–11 cannot be represented):

```
   1011     –5
+  1010   +  –6
------    ---
  10101      5    overflow – discard
                  overflow bit result
                  meaningless
```

Subtract 5.25 from 3.5 (fixed point; requires 6 bits):

```
  0011.10     3.5
+ 1010.11   + –5.25
--------    ------
  1110.01    –1.75    result meaningful
```

Subtract 7 from 7:

```
   0111      7
+  1001   +  –7
------    ---
  10000      0    overflow – disregard
                  overflow bit
```

The benefits of two's complement lie in the fact that there is only one representation for zero, and the fact that the results of operations never need adjusting due to overflow. The disadvantage is the fact that it is harder to generate the two's complement of a number.

Signal Polarity



The polarity of signals, simple as it seems, turns out to be a potentially confusing issue. With such phrases as positive and negative logic, active HIGH, and active LOW, and with one person saying "asserted," another saying "active," and another saying "enabled," all of which may or may not be well defined, it is very difficult to explain the relationships between signals. This can also make the generation of the design file more difficult.

In an attempt to sidestep the ambiguities in the language, this discussion contains tables instead of vague descriptions. The tables list the various possibilities. If you know what you want, you should be able to find how to specify your equations from the tables. The issues of input signal polarity, output signal polarity, and feedback signal polarity are treated separately.

Input Pin Polarity

Table 1 shows the relationships between the input pin names and the use of the input in a Boolean equation. As an example of how this table can be used, if you have a signal called /A on your schematic, and you wish for the output to go HIGH when both /A and B are HIGH, then from the second row of Table 1, declare the pins as /A and B in the design file, and use the equation:

```
X = /A*B
```

The basic function A*B has been used throughout for the purpose of illustration. The same procedure holds regardless of the waveforms being used or generated.

Output Pin Polarity

The issue of output polarity is slightly more complicated because of the issue of active-HIGH and active-LOW outputs. The possibilities are shown in Table 2. As an example, if a signal X is to go LOW only when inputs A and B are HIGH, and this function is to be implemented in an active-HIGH device, then from the third row of Table 2, declare the output pin as X in the design file, and use the equation:

```
X = /(A*B)
```

Feedback Polarity

Using feedback combines some of the polarity issues of inputs with some of the polarity issues of outputs. It is more difficult to use a simple example for this type of circuit. In Table 3, an output is assumed to be fed back to itself. The basic principles can be extended to any output feeding back to any other output. The waveform shows the output level that is considered to be "TRUE," or "active."

As an example, if the equation for a pin /X has to contain the inverse of the output, the output signal is to be active when HIGH, and an active-LOW device is to be used, then from the sixth row of Table 3, declare the output pin as /X in the design file, and specify the Boolean expression as:

```
/X := f (A, X)
```

meaning that the Boolean equation uses X as an input term.

Table 1. Input Pin Polarity

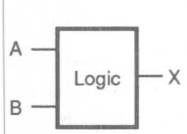
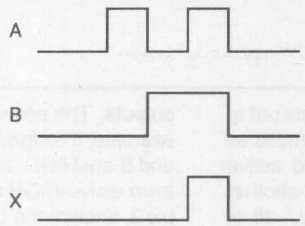
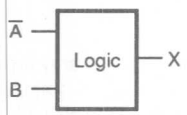
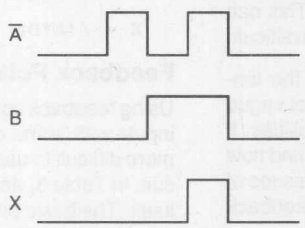
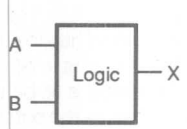
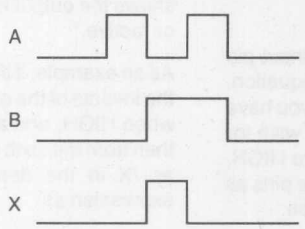
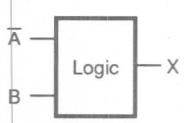
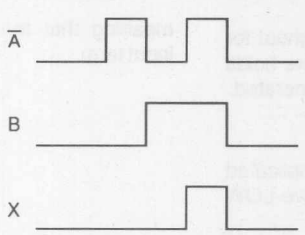
Schematic	Desired Waveform	Input Pin Definition	Boolean Equation
		A, B	X = A*B
		/A, B	X = /A*B
		A, B	X = /A*B
		/A, B	X = A*B

Table 2. Output Pin Polarity

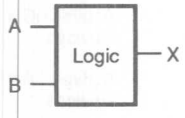
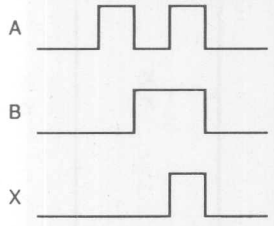
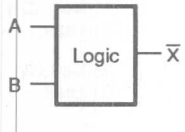
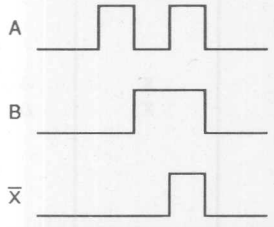
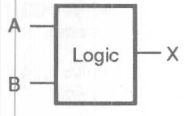
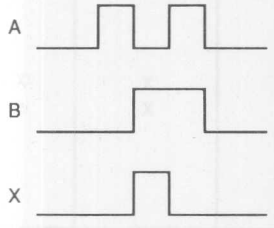
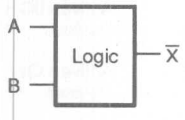
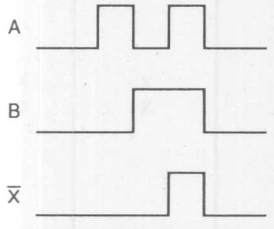
Schematic	Desired Waveform	Output Pin Definition	Boolean Equation	Device Restriction
		X X	X = A*B /X = /(A*B)	Active-HIGH Devices Active-LOW Devices
		/X /X	/X = A*B X = /(A*B)	Active-HIGH Devices Active-LOW Devices
		X X	X = /(A*B) /X = A*B	Active-HIGH Devices Active-LOW Devices
		/X /X	/X = /(A*B) X = A*B	Active-HIGH Devices Active-LOW Devices

Table 3. Feedback Signal Polarity

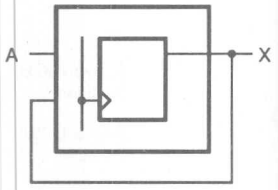
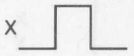
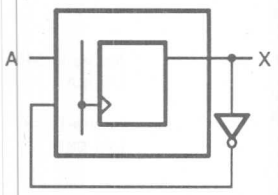
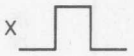
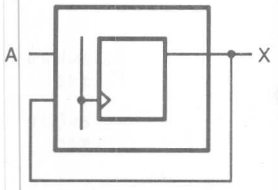
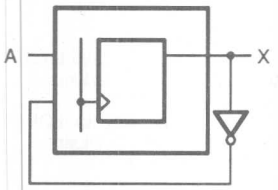
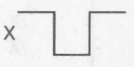
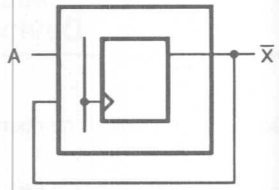
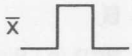
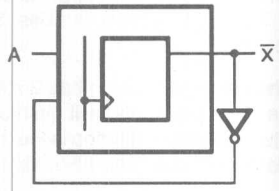
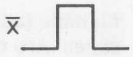
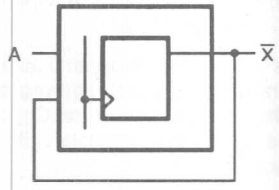
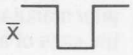
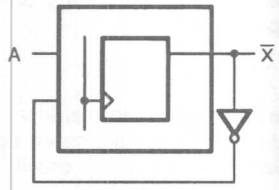
Schematic	Desired Waveform	Output Pin Definition	Boolean Equation	Device Restriction
		X X	X = f(A,X) /X = /f(A,X)	Active-HIGH Devices Active-LOW Devices
		X X	X = f(A,/X) /X = /f(A,/X)	Active-HIGH Devices Active-LOW Devices
		X X	X = /f(A,X) /X = f(A,X)	Active-HIGH Devices Active-LOW Devices
		X X	X = /f(A,/X) /X = f(A,/X)	Active-HIGH Devices Active-LOW Devices

Table 3. Feedback Signal Polarity (continued)

Schematic	Desired Waveform	Output Pin Definition	Boolean Equation	Device Restriction
		/X /X	/X = f(A,/X) X = /f(A,/X)	Active-HIGH Devices Active-LOW Devices
		/X /X	/X = f(A,X) X = /f(A,/X)	Active-HIGH Devices Active-LOW Devices
		/X /X	/X = /f(A,/X) X = f(A,/X)	Active-HIGH Devices Active-LOW Devices
		/X /X	/X = /f(A,X) X = f(A,/X)	Active-HIGH Devices Active-LOW Devices

Glossary

10KH (adj.) A family of ECL devices. Circuits are temperature compensated. See also: ECL, 100K, temperature compensation.

100K (adj.) A family of ECL devices. Circuits are both temperature and voltage compensated. They have lower power dissipation and higher speed than their 10KH counterparts. See also: ECL, temperature compensation, voltage compensation, power dissipation, 10KH.

A

active high (adj.) See polarity.

active low (adj.) See polarity.

ALS (adj.) Advanced Low-power Schottky TTL family. Characterized as a lower power version of the AS family, and actually faster and lower power than the LS family. See also: AS, LS, TTL, Schottky TTL.

AND 1. (adj.) One of the three elementary logic functions. Result of the AND operation is true if and only if all operands are true. 2. (v.t.) To perform the AND operation.

AS (adj.) Advanced Schottky TTL family. High-speed versions of the standard Schottky TTL family. Generally use oxide isolated technology for very high speed. See also: Schottky TTL, TTL, oxide isolation.

assertive high (adj.) Same as "active high". See polarity.

assertive low (adj.) Same as "active low". See polarity.

astable (adj.) Describes a system which has no stable state. Such a system will oscillate. Astable circuits can be used to generate timing and synchronizing clock signals. See also: bistable, monostable.

asynchronous 1. (adj.) Describes a sequential logic system wherein operations are not synchronized to a common clock. 2. (adj.) Describes signals whose behavior and timing are completely unrelated to a particular clock. Such signals can either be random or based on another clock which has a different frequency. 3. (adj.) Describes a communication protocol whereby the timing of various operations is not determined by a system clock, but rather by events whose relationships are known, but whose exact timing cannot be precisely predicted. See also: sequential, clock, synchronous.

B

BCD (n.) Binary Coded Decimal. Decimal numbers in 4-bit binary.

binary (adj.) Having only two possible states, which can be variously called on/off, I/O, true/false, high/low, etc.

bipolar (adj.) One of the two basic types of transistor. In logic design, used for TTL, ECL, and I^2L families. See also: TTL, ECL, I^2L, MOS.

bistable (adj.) Describes a system which has 2 stable states. Any other state is unstable, and will eventually change to one of the stable states. A flip-flop is the most common electronic bistable circuit. See also: flip-flop, astable, monostable.

bit 1. (n.) Binary Digit. One unit of binary information 2. (n.) A measure of the storage capacity of a memory chip. See also: binary.

blank (adj.) Describes the state of a programmable cell after manufacturing, and before any programming, or, in the case of an erasable device, after erasure. Opposite of "programmed". See also: programmable cell, programmed, program, erase.

buffer (n.) A logic gate which performs the logic identify function; i.e., the input is passed through unchanged. Used to isolate various parts of a system, or to provide voyage or current amplification.

C

chip (n.) A single piece of semiconductor material which contains an integrated circuit. Sometimes called a die if not in a package. See also: integrated circuit, die, package.

clock 1. (adj.) A signal used to synchronize the operation of a system. 2.(adj.) An input to a clocked flip-flop. The flip-flop will not change state until an appropriate pulse appears at the clock input. 3. (n.) A circuit which generates a clock signal. 4. (v.t.) To pulse the clock signal or the clock input of a clocked flip-flop. See also: flip-flop, clocked flip-flop.

clocked flip-flop (n.) A flip-flop that does not change state until a clock signal is received. See also: flip-flop, unclocked flip-flop, clock.

CMOS (n., adj.) Complementary MOS. A type of circuit which makes use of both N-channel and P-channel

MOS transistors. Many CMOS logic circuits consume no power when not actually switching. See also: MOS, NMOS, PMOS, standby power.

combinational (adj.) See combinatorial.

combinatorial (adj.) Refers to a logic circuit which implements logic functions of present input signals only. Also called combinational. See also: sequential.

complement 1. (adj). Refers to a signal which is identical to some reference signal, except that it is of opposite polarity. Opposite of "true". 2. (v.t.) To invert. See also: true, polarity, invert.

complementary (adj.) Refers to logic device outputs which implement identical logic functions, but with opposite polarities. Used on some PLDs and ECL devices. See also: polarity, PLD, ECL.

D

decimal (adj.) Based on the number 10.

die (n.; plural: dice) Same as a chip, particularly before being placed in a package. See also: chip, package.

digit (n.) Any number from 0 to 9.

DIP (n.) Dual In-line Package. The most common integrated circuit package. It is rectangular in shape, with widths ranging from .300 inch to .900 inch, and has vertical leads along the length. See also: integrated circuit, package.

disable 1. (v.t.) To turn off a three-state output. 2. (v.t.) To inhibit another function, such as "disabling the clock". See also: three-state, enable.

download 1. (v.t.) To pass data from one machine to a less complex machine. 2. (n.) The act of downloading data. See also: upload.

E

ECL (n., adj.) Emitter Coupled Logic family. An extremely high-speed family of bipolar logic and memory devices. See also: bipolar.

EE cell (E^2 cell) (n.) A floating gate cell which can be both programmed and erased with electrical signals.

EEPROM (n.) Electrically Erasable Programmable Read-Only Memory. A nonvolatile read-only memory device which can be erased and reprogrammed, both with special electrical signals. See also: program, erase, EPROM, PROM, ROM, RAM, nonvolatile.

enable 1. (v.t.) To turn on a three-state output. 2. (adj.) By itself, usually refers to a pin which is used to enable a three-state output. Also called "output enable". 3. (adj.) Used with other function names, indicates a qualifier or inhibitor of the function. For example, "clock enable" is a function which qualifies the clock function. 4. (v.t.) To allow a signal which has been disabled to function; for example, "enabling the clock" removes any restraint which may disable the clock signal. See also: three-state, disable.

EPROM (n.) Erasable Programmable Read-Only Memory. A non-volatile read-only memory device which can be erased and reprogrammed. Erasure is accomplished by exposing the die to ultraviolet light for a period of time. Die must be packaged in a windowed package to allow erasure. See also: program, erase, EEPROM, PROM, ROM, RAM, non-volatile, windowed package.

erase 1. (v.t.) To return a programmed device to its blank state. Opposite of "program". 2. (v.t.) To return an individual programmable cell to its blank state. See also: blank, programmable cell, program.

ESD (n.) Electrostatic Discharge. The natural physical event of the transferring of electrical charges. If uncontrolled, ESD can destroy or degrade both CMOS and bipolar semiconductor devices with inadequate on-chip protection circuitry and/or insufficient packaging and handling protection. See also: ESDS Device, CMOS, bipolar.

ESDS Device (n.) Electrostatic Discharge Sensitive Device. A device which is sensitive to damage at certain levels of ESD. Three classes exist at ESD levels of up to 1999 V, to 3999 V and above 4000 V. See also: ESD.

F

finite state machine (FSM) (n.) A machine which can be in one of a finite number of states. Often used for logic circuits which sequence through various states. Such a circuit is referred to as sequential. See also: sequential.

flip-flop (n.) A bistable digital circuit. The simplest variety is called an S-R flip-flop. Other types are J-K,T, and D-type. May be unclocked or clocked. See also: bistable, unclocked flip-flop, clocked flip-flop.

floating gate (n.) A gate on an MOS transistor which is not connected to anything. Used to store charge; forms the basis of UV cells and EE cells. See also: MOS, gate, UV cell, EE cell.

FPGA 1. (n.) Field Programmable Gate Array. A high-density PLD with multiple levels of logic and programmable interconnect. 2. (n.) Field Programmable Gate Array. An array of logic gates whose configuration can be programmed by the customer. The gates are often NAND gates, but can also be NOR gates. See also: gate, program, NAND, NOR.

FPLA (n.) Field Programmable Logic Array. See PLA.

FPLS (n.) Field Programmable Logic Sequencer. A programmable logic device which is intended for sequencing or state machine applications. See also: finite state machine.

functionally complete (adj.) Refers to a logic operation or group of operations from which any complex logic function can be built. The NAND and NOR operators are functionally complete. See also: NAND, NOR.

fuse (n.) As used in programmable logic, usually refers to a lateral metal link fuse. See also: lateral fuse.

fuse map (n.) A graphic representation of the contents of a PLD. The state of each connection (fuse or other programmable cell) is represented, usually with "X" indicating an intact connection, and "-" indicating an open connection. See also: PLD, programmable cell.

G

gate 1. (n.) A fundamental logic element. The elementary gates provide NOT, AND, and OR logic functions. 2. (n.) The control terminal of a gated D-type latch. See also: latch, gated latch.

gate array (n.) A logic device which consists of an array of logic gates (usually NAND) which can be interconnected during fabrication. A custom metallization pattern is used to configure the desired functions. See also: gate, NAND, metallization.

gate equivalency (n.) A rough measure of the complexity of a digital logic integrated circuit. Indicates the approximate number of discrete logic gates that would be needed to implement the same function. See also: gate.

gated latch (n.) Generally refers to an unclocked D-type flip-flop which has a control signal called a gate. When the gate is "open", the flip-flop output follows the data input. When the gate is "closed", the output holds its current state. Also called a transparent latch. See also: flip-flop, unclocked flip-flop, gate, latch.

H

HAL® device (n.) Hard Array Logic device. A version of a PAL device which is configured during fabrication with a custom metallization pattern. HAL is a registered trademark of Advanced Micro Devices. See also: PAL device, metallization.

I

I^2L (IIL) (n., adj.) Integrated Injection Logic. A less common bipolar logic design technique which, when used, is found primarily in portions of LSI and VLSI circuits. See also: bipolar, LSI, VLSI.

Integrated circuit (n.) An electronic device which has many transistors and other semiconductor components integrated onto one piece of silicon. Often abbreviated IC.

Invert (v.t.) To perform the logical NOT function on a digital signal. To reverse the polarity of a digital signal. See also: polarity, NOT.

Inverter (n.) A logic gate which performs logical inversion, or the NOT operation. See also: gate, NOT.

I/0 (Input/Output) 1. (n.) The methods and equipment used to pass information into and/or out of a system or device. 2. (adj.) On a programmable logic device, a pin which can function as an input and/or an output.

J

JEDEC 1. (n.) Joint Electronic Device Engineering Council. A council which creates, approves, arbitrates, and/or oversees industry standards for electronic devices. 2. (adj.) In programmable logic, refers to a computer file containing information about the programming of a device. The file format is a JEDEC-approved standard. Used for downloading to programmers. See also: program, programmer, download.

junction isolation (n.) A bipolar integrated circuit fabrication technique which uses P-N functions to isolate transistors. This is the original integrated circuit technology, and is being supplanted by oxide isolation in places where speed is critical. See also: oxide isolation, bipolar.

K

Karnaugh map (K-map) (n.) A graphic tool for minimizing sum-of-products or product-of-sums logic functions. Useful for up to six logic variables. See also: sum-of-products, product-of-sums.

L

latch 1. (n.) A type of flip-flop. Means different things to different people. In general, an unclocked flip-flop. Sometimes used to refer specifically to a gated D-type flip-flop. 2. (v.t.) To capture a signal in a latch. See also: flip-flop, unclocked flip-flop, gate, gated latch.

latch up (v.t.) To enter the latch-up condition. See also: latch-up.

latch-up (n.) A condition in which a circuit draws uncontrolled amounts of current, and certain voltages are forced, or "latched-up" to some level. Used especially in reference to CMOS devices, which can latch up if the operating conditions are violated. See also: CMOS, latch up.

lateral fuse (n.) A thin metal link which is disconnected when programmed. Connected in the blank state, disconnected in the programmed state. Usually just called a "fuse". See also: program, programmed, blank.

LCC (n.) Leadless Chip Carrier. A ceramic integrated circuit package having no leads. Connection is made to metal contacts which are flush with the package. See also: integrated circuit, lead, package.

lead (n.) [lēd] A metal conductor which provides a connection from the inside of an integrated circuit package to the outside world for soldering or other mounting techniques. See also: integrated circuit.

logic array (n.) Generally an array of programmable cells which attach inputs to logic gates of a specified type. See also: program, gate, programmable cell.

logic simulation (n.) A means whereby a logic design can be evaluated on a computer before actually being built. The computer simulates the behavior of the components to predict the behavior of the overall circuit.

LS (adj.) Low-power Schottky TTL family. Lower power version of the standard Schottky TTL family. See also: TTL, Schottky TTL.

LSI (adj.) Large-Scale Integration. A rough measure of the complexity of a digital circuit. Characterized as having 100–5000 gate equivalents for logic chips, or 1 K–16 K bits for memory chips. See also: gate equivalent, bit, VLSI, SSI, MSI.

M

macrocell (n.) Typically the output cell of a PLD, containing a flip-flop and path multiplexers.

maxterm (n.) A sum in the canonical product-of-sums form. Each maxterm contains every input variable, in either true or complemented form. See also: product-of-sums, true, complement.

metallization (n.) The process of connecting the various elements of an integrated circuit or printed circuit board by placing a layer of metal over the entire wafer or board, and then selectively etching away unwanted metal. A photolithographic mask defines the pattern of connections. See also: integrated circuit, wafer, printed circuit board.

minterm (n.) A product in the canonical sum-of-products form. Each minterm contains every input variable, either in true or complemented form. See also: sum-of-products, true, complement.

monolithic (adj.) In the electronics industry, refers to a circuit which has been integrated onto one semiconductor chip. Integrated circuits are monolithic by definition. See also: integrated circuit.

monostable (adj.) Describes a system which has 1 stable state. Any other state is unstable, and will eventually change to the stable state. The most common monostable circuit is a "one-shot". See also: bistable, astable.

MOS (n., adj.) Metal-Oxide-Semiconductor transistor. One of the two basic types of transistor. In logic design, used for NMOS, PMOS, and CMOS families. See also: NMOS, PMOS, CMOS, bipolar.

MSI (adj.) Medium-Scale Integration. A rough measure of the complexity of a digital logic circuit. Characterized as having 10–100 gate equivalents. See also: gate equivalent, SSI, LSI, VLSI.

N

NAND (adj.) Not AND. A commonly used logic gate which is equivalent to an AND gate followed by an inverter. The NAND logic operation is functionally complete.See also: gate, inverter, functionally complete, AND.

negative logic (n.) A physical implementation of logic wherein a low voltage level represents a logic 1, or "true", and a high voltage level represents a logic 0, or "false". See also: positive logic, polarity.

NMOS (n., adj.) N-channel MOS. A type of circuit which makes exclusive use of N-channel MOS transistors. See also: MOS, PMOS, CMOS.

non-volatile (adj.) Refers to memory devices which do not lose their contents when power is removed. See also: volatile.

NOR (adj.) Not OR. A logic gate which is equivalent to an OR gate followed by an inverter. The NOR logic operation is functionally complete. See also: gate, inverter, functionally complete, OR.

NOT (adj.) One of the three elementary logic functions. Unary operation whose result is true if and only if the operand is false.

O

OR 1. (adj.) One of the three elementary logic functions. Result of the OR operation is false if and only if all operands are false. 2. (v.t.) To perform the OR operation.

OTP (adj.) One-Time Programmable. Refers to programmable devices which are UV-erasable, but which are not packaged in windowed packages. As a result, there is no way to erase the device, making it programmable only once. See also: program, erase, UV-erasable, windowed package.

oxide isolation (n.) A bipolar integrated circuit fabrication technique which uses silicon oxide to isolate transistors. This results in higher speed and density. See also: junction isolation, bipolar.

P

package (n.) The encasement which protects a die and provides convenient electrical contact to the die. Materials used are generally ceramic or plastic compounds. There are a variety of shapes and sizes. See also: die.

PAL® device (n.) Programmable Array Logic device. A PLD which implements logic via a programmable AND logic array driving a fixed OR logic array. PAL is a registered trademark of Advanced Micro Devices. See also: program, logic array, sum-of-products, PLD, AND, OR.

PLA (n.) Programmable Logic Array. A programmable logic device which implements sum-of-products logic via a programmable AND logic array driving a programmable OR logic array. See also: program, logic array, sum-of-products, AND, OR.

PLCC (n.) Plastic Leaded Chip Carrier. A molded plastic integrated circuit package with leads shaped like a "J" (J-leads). Intended for surface mounting. See also: integrated circuit, lead, surface mounting, package.

PLD (n.) Programmable Logic Device. Generic term for a logic device whose function can be configured by the customer after purchase. See also: program.

PMOS (n., adj.) P-channel MOS. A type of circuit which makes exclusive use of P-channel MOS transistors. See also: MOS, NMOS, CMOS.

polarity (n.) Specifies the sense of "active" and "inactive", or "true" and "false" in a digital signal. "Active high" represents "true" as a high signal; "active low" represents "true" as a low signal.

positive logic (n.) A physical implementation of logic wherein a high voltage level represents a logic 1, or "true", and a low voltage level represents a logic 0, or "false". See also: negative logic, polarity.

power dissipation (n.) The amount of electrical power used by a device. Calculated as the product of the operating voltage and current. Measured in watts (W) or milliwatts (mW), as appropriate. Sometimes incorrectly used to refer to the operating current only.

printed circuit board (PC board, PCB) (n.) A board for assembling electrical components. Component connections are made by metal traces which have been fabricated through a metallization process. See also: trace, metallization.

product-of-sums (POS) (adj.) A representation of a logic function where the input signals are individually inverted (if necessary), then ORed together to form sums which are ANDed together. Any combinatorial logic function can be represented in product-of-sums form. See also: sum-of-products, combinatorial, AND, OR.

product term (pterm, p-term) (n.) An AND gate in a PLD which implements sum-of-products logic. See also: sum-of-products, PLD, AND, gate.

product term sharing (n.) See product term steering.

product term steering (n.) A means whereby product terms in a PAL device can be routed to one of two device outputs, instead of being dedicated only to one output. Sometimes called "product term sharing". See also: product term, PAL device.

program 1. (v.t.) As used in programmable logic, to configure a blank device so that it can perform some desired function. Applies to memory and logic devices. Opposite of "erase". 2. (v.t.) To change an individual programmable cell from a blank state to a programmed state. See also: blank, programmable cell, programmed, erase.

programmable cell (n.) Any of a variety of cells which can be altered by applying certain electrical signals. Various types are lateral and vertical fuses, UV cells, E^2 cells, and even RAM cells. All but RAM cells are non-volatile. See also: lateral fuse, vertical fuse, UV cell, E^2 cell, RAM cell, non-volatile, volatile.

programmed (adj.) Describes the state of a programmable cell or device after programming. Opposite "blank".

programmer (n.) A device or machine used for configuring, or "programming", PLDs or PROMs. See also: program, PLD, PROM.

PROM (n.) Programmable Read-Only Memory. A non-volatile memory device whose contents are programmed by the customer. Once programmed, it cannot be erased. Also functions as a PLD with a fixed AND logic array which drives a programmable OR logic array. See also: program, erase, EEPROM, EPROM, ROM, RAM, non-volatile, AND, OR, logic array.

R

RAM (n.) Random-Access Memory. Sometimes called read/write memory. A type of memory device which can be written to and read at any time. Such memory is volatile. Actually a misnomer, since most types of memories can be accessed randomly. The distinguishing feature is the fact that RAM is designed specifically to be written to in normal usage. See also: ROM, volatile.

RAM cell (n.) A cell which is used make one bit of volatile memory in a RAM. Can also form the basis of a programmable logic connectivity array. See also: RAM, volatile.

ROM (n.) Read-Only Memory. A nonvolatile memory device which has its contents defined when manufactured. No changes can be made to the memory contents. See also: PROM, EPROM, EEPROM, RAM, nonvolatile.

S

Schottky TTL (adj.) Family of TTL devices which make use of Schottky diodes for higher speed. See also: TTL.

security fuse (n.) A PLD feature which allows a user to "secure" the PLD after programming. This prevents subsequent copying of the contents of the PLD. See also: PLD, program.

semicustom (adj.) Refers to a circuit which has been partially designed by the device vendor, and partially designed, or configured, by the customer. Primary types are PLDs, gate arrays, and standard cell circuits. See also: PLD, gate array, standard cell.

sequential (adj.) Refers to a logic circuit whose operation depends both on present input signals and previous operations, or states. Requires some kind of memory (usually flip-flops) for remembering past states. See also: flip-flop, combinatorial.

SSI (adj.) Small Scale Integration. A rough measure of the complexity of a digital logic circuit. Characterized as having less than 10 gate equivalents. See also: gate equivalent, MSI, LSI, VLSI.

standard cell (n.) A method of designing semicustom or full custom circuits whereby predefined cells are brought together to provide the specified function. Unlike gate arrays, all fabrication steps are customized, instead of just the metallization step. See also: semicustom, gate array, metallization.

standby power (n.) The power consumed by a device when none of the device inputs are switching. Usually used in reference to CMOS devices, many of which consume practically no standby power. See also: CMOS.

sum-of-products (SOP) (adj.) A representation of a logic function where the input signals are individually inverted (if necessary), then ANDed together to form products which are ORed together. Any combinatorial logic function can be represented in sum-of-products form. See also: product-of-sums, combinatorial, AND, OR.

surface mounting (n.) A printed circuit board assembly technique whereby the integrated circuit packages are placed on the board with no leads protruding through to the other side. Packages can thus be mounted on both sides of the board. See also: printed circuit board, lead, through-hole mounting.

synchronous 1. (adj.) Describes a sequential logic system wherein all operations are synchronized to a common clock. 2. (adj.) Describes signals whose behavior and timing are synchronized to a clock. 3. (adj.) Describes a communication protocol whereby the timing of various operations is determined by a system clock. See also: sequential, clock, asynchronous.

T

temperature compensation (n.) A circuit feature which allows some electrical characteristics to remain relatively constant with some variation in operating temperature.

three-state (adj.) A type of logic device output which can be in one of three-states: HIGH, LOW, and OFF, or High-Z (high impedance). When enabled (on), performs as a normal binary output. When disabled (off), acts as an open pin. See also: enable, disable, binary.

through-hole mounting (n.) A printed circuit board assembly technique whereby the leads of the various components extend through holes in the board. These leads are then soldered from the opposite side of the board. See also: printed circuit board, lead, surface mounting.

trace 1. (n.) During logic simulation, the behavior of a signal or group of signals. The results can sometimes be stored in a "trace file" on disk for later analysis. 2. (n.) A thin layer of metal on a printed circuit board which provides connections between components. Performs the function of a wire. See also: logic simulation, printed circuit board.

transparent latch (n.) See gated latch.

TRI-STATE® (adj.) See three-state. TRI-STATE is a registered trademark of National Semiconductor Corp.

true (adj.) Refers to a signal which is identical to some reference signal, with the same polarity. Opposite of "complement". See also: complement, polarity.

TTL (adj.) Transistor-Transistor Logic family. The most widely used family of bipolar logic devices. The name refers to the particular circuit design technique used. See also: bipolar.

U

unclocked flip-flop (n.) A flip-flop that changes state as soon as the appropriate controls are applied.See also: flip-flop, clocked flip-flop.

upload 1. (v.t.) To pass data from one machine to a more complex machine. 2. (n.) The act of uploading data. See also: download.

UV cell (n.) A floating gate cell which can be erased by exposure to ultraviolet (UV) light. See also: floating gate, erase.

UV-erasable (adj.) Refers to devices or programmable cells which can be erased when exposed to ultraviolet (UV) light for a period of time. See also: programmable cell, erase.

V

vertical fuse (n.) A transistor arranged such that the emitter and base are shorted together when programmed. Disconnected in the blank state, connected in the programmed state. See also: program, programmed, blank.

VLSI (adj.) Very Large Scale Integration. A rough measure of the complexity of a digital circuit. Characterized as having 5000 or more gate equivalents for logic chips, or 16K or more bits for memory chips. See also: gate equivalent, bit, SSI, MSI, LSI.

volatile (adj.) Refers to memory devices which lose their contents when power is removed. See also: nonvolatile.

voltage compensation (n.) A circuit feature which allows some electrical characteristics to remain relatively constant with some variation in the supply voltage.

W

wafer (n.) A round slice of very pure silicon which is used in the fabrication of integrated circuits. Several circuits can be built on one wafer. See also: integrated circuit.

windowed package (n.) A package which has a quartz window in the lid directly over the die. This makes it possible to expose the die to ultraviolet light for erasing the device.See also: erase, die, package.

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